phyCORE®-i.MX 7

Hardware Manual

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SOM PCB. No.: **1458.3**

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Conventions, Abbreviations and Acronyms

This hardware manual describes the PCM-061 System on Module, also referred to as phyCORE-i.MX7. The manual specifies the phyCORE-i.MX7's design and function. Precise specifications for the NXP i.MX7 microcontrollers can be found in NXP's i.MX7 Data Sheet and Technical Reference Manual.

NOTE:
The BSP delivered with the phyCORE-i.MX7 usually includes drivers and/or software for controlling all components such as interfaces, memory, etc.. Therefore programming close to hardware at register level is not necessary in most cases. For this reason, this manual contains no detailed description of the controller's registers, or information relevant for software development. Please refer to the i.MX7 Reference Manual if such information is required.

Conventions

The conventions used in this manual are as follows:

- Signals that are preceded by an "n", "/", or “#” character (e.g.: nRD, /RD, or #RD), or that have a dash on top of the signal name (e.g.: RD) are designated as active low signals. That is, their active state is when they are driven low, or are driving low.
- A "0" indicates a logic zero or low-level signal, while a "1" represents a logic one or high-level signal.
- The hex-numbers given for addresses of I^2C devices always represent the 7 MSB of the address byte. The correct value of the LSB which depends on the desired command (read (1), or write (0)) must be added to get the complete address byte. E.g. given address in this manual 0x41 => complete address byte = 0x83 to read from the device and 0x82 to write to the device.
- Tables which describe jumper settings show the default position in **bold text**
- Text in blue italic indicates a hyperlink within, or external to the document. Click these links to quickly jump to the applicable URL, part, chapter, table, or figure.
- References made to the phyCORE-Connector always refer to the high density Samtec connectors on the undersides of the phyCORE-i.MX7

Abbreviations and Acronyms

Many acronyms and abbreviations are used throughout this manual. Use the table below to navigate unfamiliar terms used in this document.

Table 1. Abbreviations and Acronyms used in this Manual

Abbreviation	Definition
BSP	Board Support Package - Software delivered with the Development Kit including an operating system (Linux) preinstalled on the module and Development Tools.
CB	Carrier Board - Used in reference to the phyCORE-i.MX7 Development Kit Carrier Board.
EMI	Electromagnetic interference
GPIO	General purpose input and output
J	Solder jumper - These types of jumpers require solder equipment to remove and place
PCB	Printed circuit board
PMIC	Power management IC
POR	Power-on reset
RTC	Real-time clock
SMT	Surface mount technology
SOM	System on Module - Used in reference to the PCM-061 / phyCORE-i.MX7 System on Module
VBAT	SOM standby voltage input

Different types of signals are brought out at the phyCORE-Connector. The following table lists the abbreviations used to specify each type of signal.

Table 2. Types of Signals

Type of Signal	Description	Abbr.
Power	Supply voltage	PWR
Ref-Voltage	Reference voltage	REF
USB-Power	USB voltage	USB
Input	Digital input	IN
Output	Digital output	OUT
Input with pull up	Input with pull-up, must only be connected to GND (jumper or open-collector output).	IPU
Input / output	Bidirectional input / output	IO
5V Input with pulldown	5V tolerant input with pull-down	5V_PD
5V Input with pull-up	5V tolerant input with pull-up	5V_PU
3.3V Input with Pull-up	3.3V tolerant input with pull-up	3V3_PU
3.3V Input with pull-down	3.3V tolerant input with pull-down	3V3_PD
LVDS	Differential line pairs 100 Ohm LVDS	LVDS
Differential 90 Ohm	Differential line pairs 90 Ohm	DIFF90
Differential 100 Ohm	Differential line pairs 100 Ohm	DIFF100
Analog	Analog input or output	Analog

Preface

This phyCORE-i.MX7 Hardware Manual describes the System on Module's design and functions. Precise specifications for the NXP i.MX7 processor can be found in the processor datasheet and/or technical reference manual (TRM).

Ordering Information

The part numbering of the phyCORE-i.MX7 has the following structure[1]:

PCM-061-0000000C.Ax

Option	DDR3
0	256MB
1	512MB
2	1GB
3	2GB

Option	eMMC/NAND
0	No NAND/eMMC
1	4GB eMMC
2	8GB eMMC
3	16GB eMMC
4	32GB eMMC
5	256MB NAND

Option	QSPI NOR
0	None
1	16MB

Option	Controller
0	MCIMX7D7DVK10 SC DualCore (CAN)
1	MCIMX7D3EVK10 SC DualCore
2	MCIMX7S5EVK08 SC Solo Core (CAN)

Option	EEPROM
0	None
1	4KB

Option	Ethernet PHY
0	None
1	10/100/1000 PHY

Option	Ext. RTC
0	None
1	Yes

Option	Processor Temp
E	-20 - 105 C
C	0 - 95C

Notes:

- i.MX7Dual with CAN is only available in Commercial Temperature

[1] This structure shows the ordering options available as of the printing of this manual. Additional ordering options may have been added. Please contact our sales team to check current availability, inventory, and lead-time.

Declaration of Electro Magnetic Conformity of the PHYTEC phyCORE-i.MX7 System On Module

PHYTEC System on Modules (SOMs) are designed for installation in electrical appliances or, combined with the PHYTEC Carrier Board, can be used as dedicated Evaluation Boards (for use as a test and prototype platform for hardware/software development) in laboratory environments.

CAUTION:
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

NOTE:
Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The phyCORE-i.MX7 is one of a series of PHYTEC System on Modules that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports a variety of 8-/16- and 32-bit controllers in two ways:

1. As the basis for Rapid Development Kits which serve as a reference and evaluation platform.
2. As insert-ready, fully functional phyCORE OEM modules, which can be embedded directly into the user's peripheral hardware design.

Implementation of an OEM-able SOM subassembly as the "core" of your embedded design allows you to focus on hardware peripherals and firmware without expending resources to "re-invent" microcontroller circuitry. Furthermore, much of the value of the phyCORE module lies in its layout and test.

Production-ready Board Support Packages (BSPs) and Design Services for our hardware further reduce development time and expenses. Take advantage of PHYTEC products to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks. For more information go to: http://phytec.com/contact/

Product Change Management

In addition to our HW and SW offerings, the buyer will receive a free obsolescence maintenance service for the HW provided when purchasing a PHYTEC SOM.

Our Product Change Management Team of developers is continuously processing all incoming PCN's (Product Change Notifications) from vendors and distributors concerning parts which are being used in our products. Possible impacts to the functionality of our products, due to changes of functionality or obsolesce of a certain part, are evaluated in order to take the right measures in purchasing or within our HW/SW design.

Our general philosophy here is: We never discontinue a product as long as there is demand for it. Therefore, a set of methods has been established to fulfill our philosophy:

Avoidance Strategies

- Avoid changes by evaluating longevity of a parts during design-in phase.
- Ensure availability of equivalent second source parts.
- Maintain close contact with part vendors for awareness of roadmap strategies.

Change Management in Case of Functional Changes

- Avoid impacts on Product functionality by choosing equivalent replacement parts.
- Avoid impacts on Product functionality by compensating changes through HW redesign or backward compatibility

SW Maintenance

- Provide early change notifications concerning functional relevant changes of our Products.

Change Management in Rare Event of an Obsolete and Non-Replaceable Part

- Ensure long term availability by stocking parts through last time buy management, according to product forecasts.
- Offer long term frame contract to customers.

We refrain from providing detailed, part-specific information within this manual, which is subject to changes, due to ongoing part maintenance for our products.

1 Introduction

The phyCORE-i.MX7 belongs to PHYTEC's phyCORE System on Module family. The phyCORE SOMs represent the continuous development of PHYTEC System on Module technology. Like its mini-, micro- and nanoMODULE predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware development.

Independent research indicates that approximately 70% of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments. The phyCORE board design features an increased pin package that allows dedication of approximately 20% of all connector pins on the phyCORE boards to ground. This improves EMI and EMC characteristics, making it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD components and laser-drilled microvias are implemented, providing phyCORE users with access to this cutting-edge miniaturization technology for integration into their own design.

The phyCORE-i.MX7 is a subminiature (41 mm x 50 mm) insert-ready System on Module populated with the NXP i.MX7 microcontroller. Its universal design enables its insertion in a wide range of embedded applications. All controller signals and ports extend from the controller to high-density pitch (0.5 mm) connectors aligning two sides of the board, allowing it to be inserted like a "big chip" into a target application.

Precise specifications for the controller populating the board can be found in the applicable controller Technical Reference Manual or datasheet. The descriptions in this manual are based on the NXP i.MX7. A description of compatible microcontroller derivative functions is not included, as such functions are not relevant for the basic functioning of the phyCORE-i.MX7.

The phyCORE-i.MX7 offers the following features:

- Insert-ready, sub-miniature (41 mm x 50 mm) System on Module (SOM) subassembly in low EMI design, achieved through advanced SMD technology
- Populated with the NXP i.MX7 microcontroller (12 x 12 mm, 0.4 mm Pitch BGA)
- Single or Dual ARM® Cortex™-A7 at max. 1 GHz clock frequency
- ARM® Cortex™-M4 at max. 266MHz
- On-board power management IC with integrated RTC
- Ultra-low power off-chip RTC
- Boot from SD, eMMC, NAND Flash, or QSPI Flash
- Up to 2 GB DDR3/3L
- Up to 8 GB NAND or 128 GB eMMC
- 4 KB EEPROM
- 16 MB QSPI NOR
- 2x HighSpeed USB 2.0 OTG with integrated HS USB PHY
- High-Speed USB 2.0 host with integrated HSIC (High-Speed Inter-Chip USB PHY)
- 1x gigabit Ethernet interface with on SOM Ethernet PHY allowing for direct connection to an Ethernet network
- 1x gigabit Ethernet interface at TTL-level; available at the phyCORE connector
- 4x I^2C
- 24-bit parallel LCD Display

- 6x UART[2]
- 2x eCSPI[2]
- 3x SDIO/SD/MMC
- 2x CAN
- PCI Express 2.0 (1 Lane)
- MIPI CSI (2 Lane)
- MIPI DSI (2 Lane)
- 4x ADC
- 3x Tamper
- 3x PWM[2]
- 1x SAI[2]
- 1x QSPI
- Keypad (3x3)[2]
- JTAG
- GPIO

[2] Highly multiplexed. All ports may not be available at once depending on use case.

1.1 Block Diagram

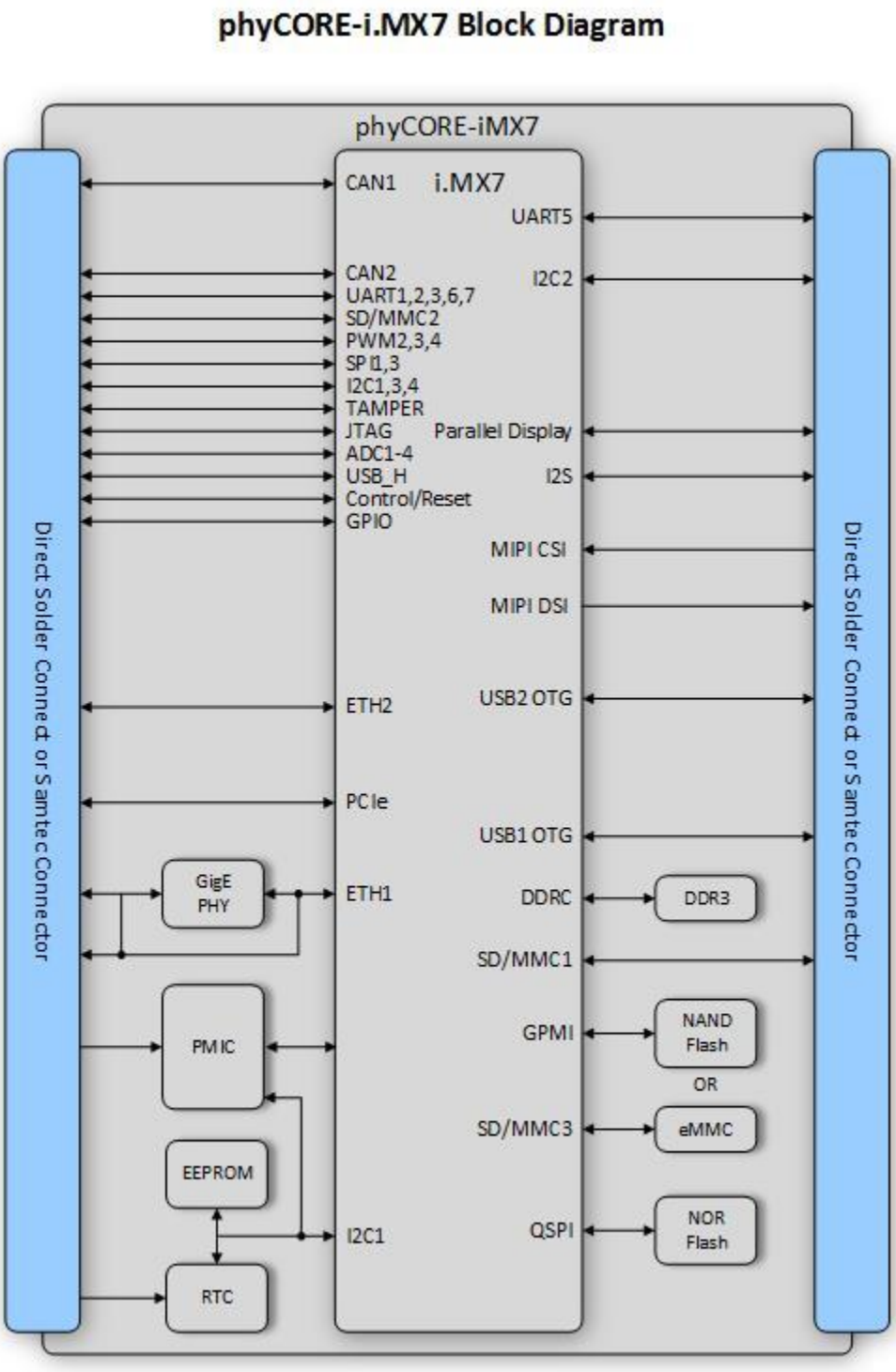

Figure 1. phyCORE-i.MX7 Block Diagram

1.2 Component Placement Diagram

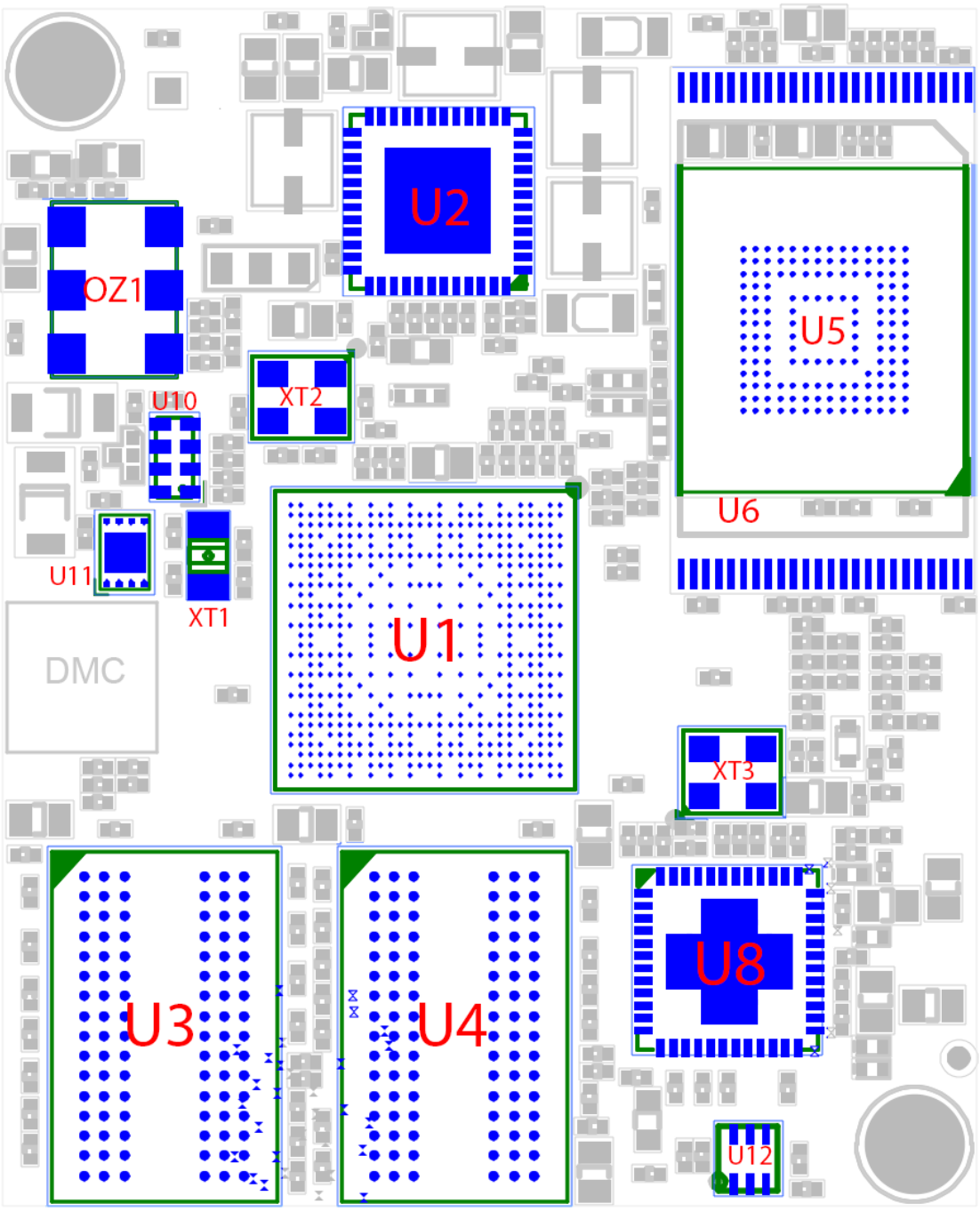

Figure 2. phyCORE-i.MX7 Component Placement (top view)[3]

[3] Detailed component placement diagrams with all reference designators are available through our website

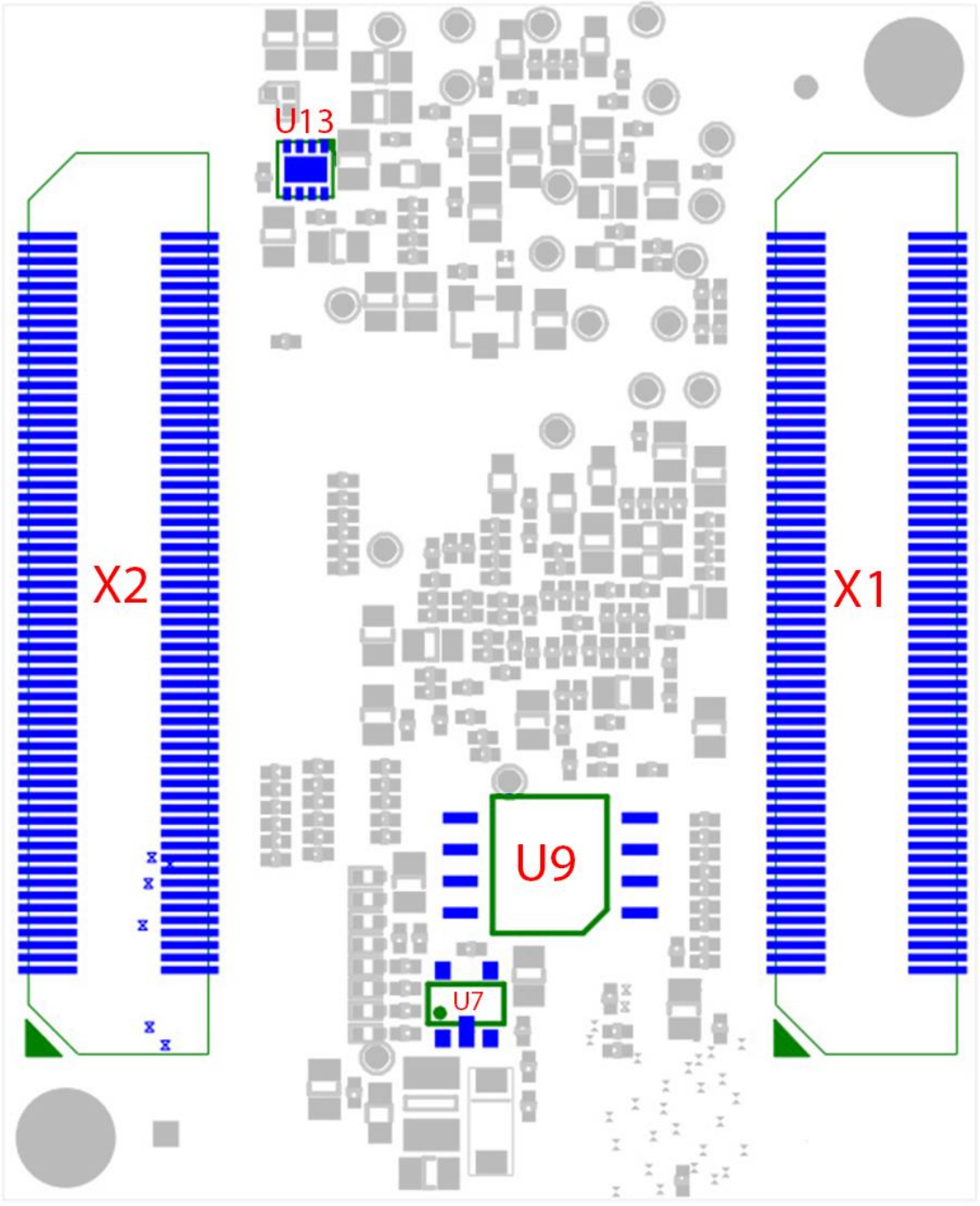

Figure 3. phyCORE-i.MX7 Component Placement (bottom view)[3]

2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

All controller signals extend to surface mount technology (SMT) connectors (0.5 mm) lining two sides of the module (referred to as the phyCORE-Connector). This allows the phyCORE-i.MX7 to be inserted into any target application like a "big chip".

The numbering scheme for the phyCORE-Connector is based on a two-dimensional matrix in which column positions are identified by a letter and row position by a number. Pin A1, for example, is located in the lower right hand corner of the matrix looking down through the top of the SOM. The pin numbering values decrease moving down on the board. Lettering of the pin connector columns progresses alphabetically from right to left for each connector (refer to Figure 4).

The numbered matrix can be aligned with the phyCORE-i.MX7 (viewed from above; phyCORE-Connector pointing down) or with the socket of the corresponding phyCORE Carrier Board/user target circuitry. The lower right-hand corner of the numbered matrix (pin A1) is thus covered with the corner of the phyCORE-i.MX7 marked with a triangle. The numbering scheme is always in relation to the PCB as viewed from above, even if all connector contacts extend to the bottom of the module.

The following figure illustrates the numbered matrix system. It shows a phyCORE-i.MX7 with SMT phyCORE Connectors on its underside (defined with dotted lines) as it would be mounted on a Carrier Board. In order to facilitate understanding of the pin assignment scheme, the diagram presents a cross-view of the phyCORE-module showing these phyCORE-Connectors mounted on the underside of the module’s PCB.

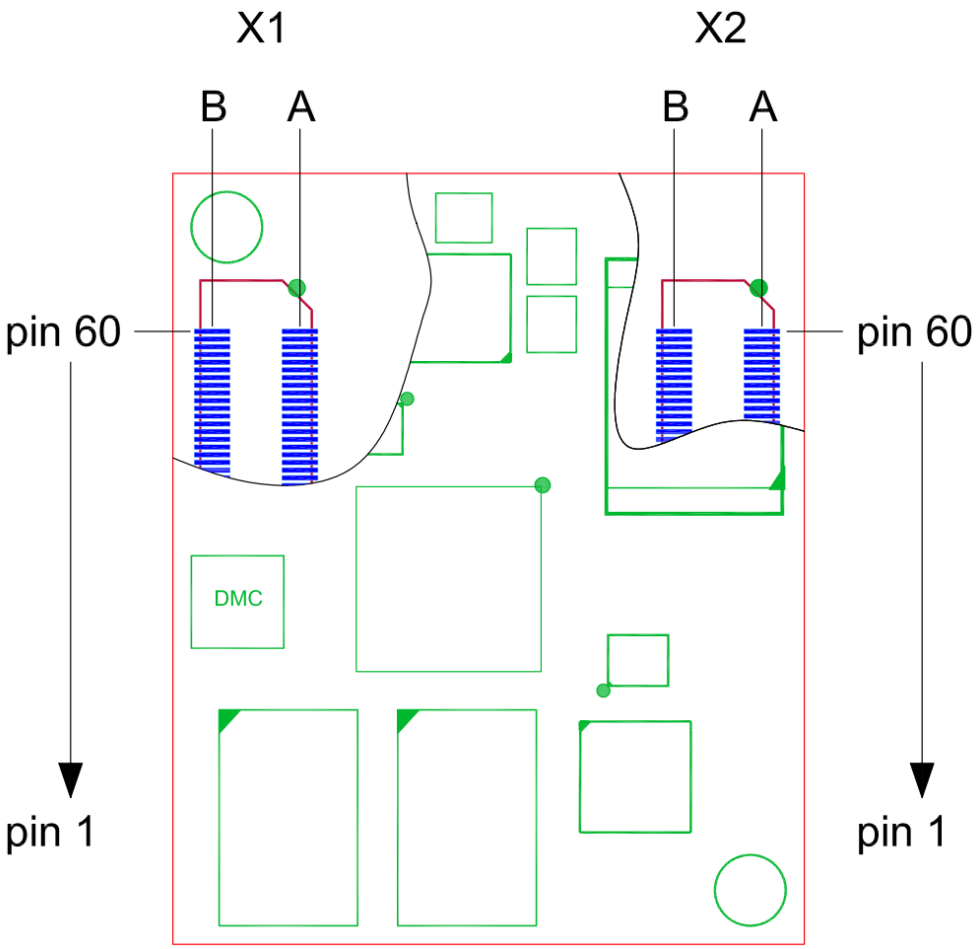

Figure 4. Pinout of the phyCORE-Connector (top view, with cross section insert)

Table 3 provides an overview of the pinout of the phyCORE-Connector with signal names and descriptions specific to the phyCORE-i.MX7. It also provides the appropriate signal level interface voltages listed in the Level column, along with the signal direction.

CAUTION:
Most of the controller pins have multiple multiplexed functions. Because most of these pins are connected directly to the phyCORE-Connector the functions are also available at the connector. Signal names and descriptions in Table 3, however, are in regard to the specification of the phyCORE-i.MX7 and the functions defined therein. Please refer to the i.MX7 datasheet, or the schematic to learn about alternative functions. In order to utilize a specific pin's alternative function the corresponding registers must be configured within the appropriate driver of the BSP. To support all features of the phyCORE-i.MX7 Carrier Board a few changes have been made in the BSP delivered with the module.

The NXP i.MX7 is a multi-voltage operated microcontroller and as such special attention should be paid to the interface voltage levels to avoid unintentional damage to the microcontroller and other on-board components. Please refer to the NXP i.MX7 Reference Manual for details on the functions and features of controller signals and port pins.

Table 3. phyCORE-Connector (X1, X2) Pin-Out Description

X1, Column A				
Pin #	**Signal**	**Type**	**Level**	**Description**
A1	X_I2C1_SCL	IO	3.3V	I²C bus 1 clock
A2	X_I2C1_SDA	IO	3.3V	I²C bus 1 data
A3	X_I2C2_SCL	IO	3.3V	I²C bus 2 clock
A4	X_I2C2_SDA	IO	3.3V	I²C bus 2 data
A5	X_I2C3_SCL	IO	3.3V	I²C bus 3 clock
A6	X_I2C3_SDA	IO	3.3V	I²C bus 3 data
A7	GND	-	-	Ground
A8	X_JTAG_TMS	IN	3.3V	JTAG Test Mode Select
A9	X_JTAG_TDO	OUT	3.3V	JTAG Test Data Out
A10	X_JTAG_TDI	IN	3.3V	JTAG Test Data In
A11	X_JTAG_TCK	IN	3.3V	JTAG Test Clock
A12	X_JTAG_TRST_B	IN	3.3V	JTAG Test Reset
A13	X_SNVS_TAMPER0	IN	1.8V	Tamper Detection Pin 0
A14	X_SNVS_TAMPER1	IN	1.8V	Tamper Detection Pin 1
A15	GND	-	-	Ground
A16	X_CAN1_RX	IN	3.3V	CAN1 Receive
A17	X_CAN1_TX	OUT	3.3V	CAN1 Transmit
A18	X_CAN2_RX	IN	3.3V	CAN2 Receive
A19	X_CAN2_TX	OUT	3.3V	CAN2 Transmit
A20	GND	-	-	Ground
A21	X_UART6_RX	IN	3.3V	UART6 Receive
A22	X_UART6_TX	OUT	3.3V	UART6 Transmit
A23	X_UART5_RX	IN	3.3V	UART5 Receive
A24	X_UART5_TX	OUT	3.3V	UART5 Transmit
A25	GND	-	-	Ground
A26	X_NAND_CE1_B	OUT	3.3V	NAND Chip Enable 1
A27	X_NAND_CE0_B	OUT	3.3V	NAND Chip Enable 0
A28	X_NAND_DQS	IO	3.3V	NAND DQS Signal
A29	X_NAND_READY_B	IO	3.3V	NAND Ready Signal
A30	X_NAND_CE2_B	OUT	3.3V	NAND Chip Enable 2
A31	X_NAND_CE3_B	OUT	3.3V	NAND Chip Enable 3
A32	GND	-	-	Ground
A33	X_ADC_IN0	Analog	1.8V	Analog to Digital Converter Input Bit 0
A34	X_ADC_IN1	Analog	1.8V	Analog to Digital Converter Input Bit 1
A35	X_ADC_IN2	Analog	1.8V	Analog to Digital Converter Input Bit 2
A36	X_ADC_IN3	Analog	1.8V	Analog to Digital Converter Input Bit 3
A37	GND	-	-	Ground
A38	X_GPIO2_30	IO	3.3V	i.MX7 GPIO2_30
A39	X_GPIO2_10	IO	3.3V	i.MX7 GPIO2_10
A40	X_I2C4_SCL	IO	3.3V	I²C bus 4 clock
A41	X_I2C4_SDA	IO	3.3V	I²C bus 4 data
A42	X_GPIO2_11	IO	3.3V	i.MX7 GPIO2_11
A43	X_PWM3	OUT	3.3V	Pulse Width Modulation 3
A44	GND	-	-	Ground
A45	X_SD1_RESET_B	IO	3.3V	SD/MMC1 Reset

X1, Column A				
Pin #	**Signal**	**Type**	**Level**	**Description**
A46	X_SD1_CD_B	IN	3.3V	SD/MMC1 Card Detect
A47	X_SD1_WP	IN	3.3V	SD/MMC1 Write Protect
A48	X_SD1_CLK	IO	3.3V	SD/MMC1 Clock
A49	X_SD1_CMD	IO	3.3V	SD/MMC1 Command
A50	GND	-	-	Ground
A51	X_SD1_DATA0	IO	3.3V	SD/MMC1 Data 0
A52	X_SD1_DATA1	IO	3.3V	SD/MMC1 Data 1
A53	X_SD1_DATA2	IO	3.3V	SD/MMC1 Data 2
A54	X_SD1_DATA3	IO	3.3V	SD/MMC1 Data 3
A55	GND	-	-	Ground
A56	VCC_SOM	PWR	3.3V	3.3V Input Power
A57	VCC_SOM	PWR	3.3V	3.3V Input Power
A58	VCC_SOM	PWR	3.3V	3.3V Input Power
A59	VCC_SOM	PWR	3.3V	3.3V Input Power
A60	GND	-	-	Ground

X1, Column B				
Pin #	**Signal**	**Type**	**Level**	**Description**
B1	X_GPIO2_12	IO	3.3V	i.MX7 GPIO2_12
B2	X_GPIO2_13	IO	3.3V	i.MX7 GPIO2_13
B3	X_GPIO2_14	IO	3.3V	i.MX7 GPIO2_14
B4	X_GPIO2_15	IO	3.3V	i.MX7 GPIO2_15
B5	GND	-	-	Ground
B6	X_MX7_ONOFF	IN	3V	i.MX7 ON/OFF Input (*Drive using an open drain output*)
B7	X_3V3MEM_EN	OUT	3.3V	External 3.3V Sequencing Output
B8	X_PMIC_PWRON	IN	3V	PMIC PWRON Input
B9	X_POR_B	OUT	3.3V	Power On Reset
B10	GND	-	-	Ground
B11	X_GPIO1_09	IO	3.3V	i.MX7 GPI1_09
B12	X_SNVS_TAMPER2	IN	1.8V	Tamper Detection Pin 2
B13	SW2_1V8	PWR	1.8V	1.8V Output
B14	GND	-	-	Ground
B15	X_UART1_RX	IN	3.3V	UART1 Receive
B16	X_UART1_TX	OUT	3.3V	UART1 Transmit
B17	X_UART2_RX	IN	3.3V	UART2 Receive
B18	X_UART2_TX	OUT	3.3V	UART2 Transmit
B19	X_UART3_RX	IN	3.3V	UART3 Receive
B20	X_UART3_TX	OUT	3.3V	UART3 Transmit
B21	GND	-	-	Ground
B22	X_PCIE_RX_N	DIFF100	-	PCIe Differential Negative Receive
B23	X_PCIE_RX_P	DIFF100	-	PCIe Differential Positive Receive
B24	GND	-	-	Ground
B25	X_PCIE_TX_P	DIFF100	-	PCIe Differential Positive Transmit
B26	X_PCIE_TX_N	DIFF100	-	PCIe Differential Negative Transmit
B27	GND	-	-	Ground
B28	X_PCIE_REFCLK_P	DIFF100	-	PCIe Differential Positive Reference Clock

X1, Column B				
Pin #	**Signal**	**Type**	**Level**	**Description**
B29	X_PCIE_REFCLK_N	DIFF100	-	PCIe Differential Negative Reference Clock
B30	GND	-	-	Ground
B31	X_NAND_WP_B	OUT	3.3V	NAND Wait Polarity
B32	X_SD2_CD_B	IN	1.8V/3.3V[4]	SD/MMC2 Card Detect
B33	X_SD2_WP	IN	1.8V/3.3V[4]	SD/MMC2 Write Protect
B34	X_SD2_RESET_B	IO	1.8V/3.3V[4]	SD/MMC2 Reset
B35	GND	-	-	Ground
B36	X_SD2_CLK	IO	1.8V/3.3V[4]	SD/MMC2 Clock
B37	X_SD2_CMD	IO	1.8V/3.3V[4]	SD/MMC2 Command
B38	X_SD2_DATA0	IO	1.8V/3.3V[4]	SD/MMC2 Data 0
B39	X_SD2_DATA1	IO	1.8V/3.3V[4]	SD/MMC2 Data 1
B40	X_SD2_DATA2	IO	1.8V/3.3V[4]	SD/MMC2 Data 2
B41	X_SD2_DATA3	IO	1.8V/3.3V[4]	SD/MMC2 Data 3
B42	GND	-	-	Ground
B43	X_SPI1_SCLK	IO	1.8V/3.3V[4]	SPI1 Clock
B44	X_SPI1_MISO	IO	1.8V/3.3V[4]	SPI1 Master In Slave Out
B45	X_SPI1_MOSI	IO	1.8V/3.3V[4]	SPI1 Master Out Slave In
B46	X_SPI1_SS0	IO	1.8V/3.3V[4]	SPI1 Slave Select 0
B47	X_nWDOG_RST	OUT	3.3V	Active Low Soft Reset Signal
B48	GND	-	-	Ground
B49	X_UART7_RX	IN	1.8V/3.3V[4]	UART7 Receive
B50	X_UART7_RTS	OUT	1.8V/3.3V[4]	UART7 Request to Send
B51	X_UART7_TX	OUT	1.8V/3.3V[4]	UART7 Transmit
B52	X_UART7_CTS	IN	1.8V/3.3V[4]	UART7 Clear to Send
B53	X_BOOT_MODE1	IN	3.3V	Boot Type Select 1
B54	X_BOOT_MODE0	IN	3.3V	Boot Type Select 0
B55	GND	-	-	Ground
B56	VLDO2_1V5	PWR	1.5V	1.5V Output
B57	VBAT	PWR	3V	Battery Input Power
B58	VCC_SOM	PWR	3.3V	3.3V Input Power
B59	No Connect	-	-	For Internal Use Only
B60	No Connect	-	-	For Internal Use Only

[4] Voltage reference level determined by jumper population. Refer to the following 'Jumpers' section for further details.

X2, Column A				
Pin #	**Signal**	**Type**	**Level**	**Description**
A1	GND	-	-	Ground
A2	X_LCD1_DATA21_BOOT21	IO	3.3V	LCD1 Display Data 21 / BOOT 21 Signal
A3	X_LCD1_DATA14_BOOT14	IO	3.3V	LCD1 Display Data 14 / BOOT 14 Signal
A4	X_LCD1_ENABLE	OUT	3.3V	LCD1 Display Enable
A5	X_LCD1_DATA12_BOOT12	IO	3.3V	LCD1 Display Data 12 / BOOT 12 Signal
A6	GND	-	-	Ground
A7	X_LCD1_DATA11_BOOT11	IO	3.3V	LCD1 Display Data 11 / BOOT 11 Signal
A8	X_LCD1_DATA13_BOOT13	IO	3.3V	LCD1 Display Data 13 / BOOT 13 Signal
A9	X_LCD1_DATA19_BOOT19	IO	3.3V	LCD1 Display Data 19 / BOOT 19 Signal
A10	X_LCD1_DATA18_BOOT18	IO	3.3V	LCD1 Display Data 18 / BOOT 18 Signal
A11	GND	-	-	Ground
A12	X_LCD1_DATA16_BOOT16	IO	3.3V	LCD1 Display Data 16 / BOOT 16 Signal
A13	X_LCD1_DATA20_BOOT20	IO	3.3V	LCD1 Display Data 20 / BOOT 20 Signal
A14	X_LCD1_DATA15_BOOT15	IO	3.3V	LCD1 Display Data 15 / BOOT 15 Signal
A15	X_LCD1_DATA10_BOOT10	IO	3.3V	LCD1 Display Data 10 / BOOT 10 Signal
A16	GND	-	-	Ground
A17	X_LCD1_HSYNC	IO	3.3V	LCD1 Horizontal Sync
A18	X_LCD1_VSYNC	IO	3.3V	LCD1 Vertical Sync
A19	X_LCD1_DATA17_BOOT17	IO	3.3V	LCD1 Display Data 17 / BOOT 17 Signal
A20	X_LCD1_DATA23_BOOT23	IO	3.3V	LCD1 Display Data 23 / BOOT 23 Signal
A21	X_LCD1_DATA1_BOOT1	IO	3.3V	LCD1 Display Data 1 / BOOT 1 Signal
A22	X_LCD1_DATA22_BOOT22	IO	3.3V	LCD1 Display Data 22 / BOOT 22 Signal
A23	GND	-	-	Ground
A24	X_LCD1_DATA2_BOOT2	IO	3.3V	LCD1 Display Data 2 / BOOT 2 Signal
A25	X_LCD1_DATA5_BOOT5	IO	3.3V	LCD1 Display Data 5 / BOOT 5 Signal
A26	X_LCD1_DATA4_BOOT4	IO	3.3V	LCD1 Display Data 4 / BOOT 4 Signal
A27	X_LCD1_DATA3_BOOT3	IO	3.3V	LCD1 Display Data 3 / BOOT 3 Signal
A28	GND	-	-	Ground
A29	X_LCD1_DATA0_BOOT0	IO	3.3V	LCD1 Display Data 0 / BOOT 0 Signal
A30	X_LCD1_RESET	OUT	3.3V	LCD1 Reset
A31	X_LCD1_CLK	OUT	3.3V	LCD1 Clock
A32	X_LCD1_DATA8_BOOT8	IO	3.3V	LCD1 Display Data 8 / BOOT 8 Signal
A33	GND	-	-	Ground
A34	X_LCD1_DATA9_BOOT9	IO	3.3V	LCD1 Display Data 9 / BOOT 9 Signal
A35	X_LCD1_DATA6_BOOT6	IO	3.3V	LCD1 Display Data 6 / BOOT 6 Signal
A36	X_LCD1_DATA7_BOOT7	IO	3.3V	LCD1 Display Data 7 / BOOT 7 Signal
A37	X_PWM2	OUT	3.3V	Pulse Width Modulation 4
A38	GND	-	-	Ground
A39	X_RGMII2_RX0	IN	3.3V	RGMII2 Receive Data 0
A40	X_RGMII2_RX1	IN	3.3V	RGMII2 Receive Data 1
A41	X_RGMII2_RX2	IN	3.3V	RGMII2 Receive Data 2
A42	X_RGMII2_RX3	IN	3.3V	RGMII2 Receive Data 3
A43	GND	-	-	Ground
A44	X_RGMII2_RX_CTL	IN	3.3V	RGMII2 Receive Control
A45	X_RGMII2_RXC	IN	3.3V	RGMII2 Receive Clock
A46	X_RGMII2_TX_CTL	OUT	3.3V	RGMII2 Transmit Control
A47	X_RGMII2_TXC	OUT	3.3V	RGMII2 Transmit Clock

X2, Column A				
Pin #	**Signal**	**Type**	**Level**	**Description**
A48	GND	-	-	Ground
A49	X_RGMII2_TX0	OUT	3.3V	RGMII2 Transmit Data 0
A50	X_RGMII2_TX1	OUT	3.3V	RGMII2 Transmit Data 1
A51	X_RGMII2_TX2	OUT	3.3V	RGMII2 Transmit Data 2
A52	X_RGMII2_TX3	OUT	3.3V	RGMII2 Transmit Data 3
A53	GND	-	-	Ground
A54	X_MDIO_D	IO	3.3V	Ethernet MDIO Data
A55	X_MDIO_MCLK	OUT	3.3V	Ethernet MDIO Clock
A56	X_ETH1_LED1	IO	3.3V	ETH1 Configuration Input and Speed LED Output
A57	X_ETH1_LED2	IO	3.3V	ETH1 Configuration Input and Link LED Output
A58	GND	-	-	Ground
A59	X_SAI1_RXD0	IN	3.3V	SAI1 Receive Data 0
A60	X_SAI1_TX_BCLK	OUT	3.3V	SAI1 Transmit Bit Clock

X2, Column B				
Pin #	**Signal**	**Type**	**Level**	**Description**
B1	X_ETH1_D-/RGMII1_RX0	IN	3.3V	ETH1 Differential Negative D / RGMII1 Receive Data 0
B2	X_ETH1_D+/RGMII1_RX1	IN	3.3V	ETH1 Differential Positive D / RGMII1 Receive Data 1
B3	X_ETH1_C-/RGMII1_RX2	IN	3.3V	ETH1 Differential Negative C / RGMII1 Receive Data 2
B4	X_ETH1_C+/RGMII1_RX3	IN	3.3V	ETH1 Differential Positive C / RGMII1 Receive Data 3
B5	GND	-	-	Ground
B6	X_ETH1_B-/RGMII1_TX0	OUT	3.3V	ETH1 Differential Negative B / RGMII1 Transmit Data 0
B7	X_ETH1_B+/RGMII1_TX1	OUT	3.3V	ETH1 Differential Positive B / RGMII1 Transmit Data 1
B8	X_ETH1_A-/RGMII1_TX2	OUT	3.3V	ETH1 Differential Negative A / RGMII1 Transmit Data 2
B9	X_ETH1_A+/RGMII1_TX3	OUT	3.3V	ETH1 Differential Positive B / RGMII1 Transmit Data 3
B10	GND	-	-	Ground
B11	X_RGMII1_TXC	OUT	3.3V	RGMII1 Transmit Clock
B12	X_RGMII1_TX_CTL	OUT	3.3V	RGMII1 Transmit Control
B13	X_RGMII1_RXC	IN	3.3V	RGMII1 Receive Clock
B14	X_RGMII1_RX_CTL	IN	3.3V	RGMII1 Receive Control
B15	GND	-	-	Ground
B16	X_MIPI_DSI_D0_N	DIFF100	-	DSI Differential Data 0 Negative
B17	X_MIPI_DSI_D0_P	DIFF100	-	DSI Differential Data 0 Positive
B18	GND	-	-	Ground
B19	X_MIPI_DSI_CLK_P	DIFF100	-	DSI Differential Clock Positive
B20	X_MIPI_DSI_CLK_N	DIFF100	-	DSI Differential Clock Negative
B21	GND	-	-	Ground
B22	X_MIPI_DSI_D1_N	DIFF100	-	DSI Differential Data 1 Negative
B23	X_MIPI_DSI_D1_P	DIFF100	-	DSI Differential Data 1 Positive
B24	GND	-	-	Ground
B25	X_MIPI_CSI_D0_P	DIFF100	-	CSI Differential Data 0 Positive
B26	X_MIPI_CSI_D0_N	DIFF100	-	CSI Differential Data 0 Negative
B27	GND	-	-	Ground
B28	X_MIPI_CSI_CLK_N	DIFF100	-	CSI Differential Clock Negative
B29	X_MIPI_CSI_CLK_P	DIFF100	-	CSI Differential Clock Positive
B30	GND	-	-	Ground

X2, Column B				
Pin #	**Signal**	**Type**	**Level**	**Description**
B31	X_MIPI_CSI_D1_N	DIFF100	-	CSI Differential Data 1 Negative
B32	X_MIPI_CSI_D1_P	DIFF100	-	CSI Differential Data 1 Positive
B33	GND	-	-	Ground
B34	X_USB_H_DATA	IO	3.3V	USB HSIC Data Signal
B35	X_USB_H_STROBE	IO	3.3V	USB HSIC Strobe Signal
B36	GND	-	-	Ground
B37	X_USB_OTG2_DP	DIFF100	3.3V	USB2 Differential Data Positive
B38	X_USB_OTG2_DN	DIFF100	3.3V	USB2 Differential Data Negative
B39	GND	-	-	Ground
B40	X_USB_OTG1_DP	DIFF100	3.3V	USB1 Differential Data Positive
B41	X_USB_OTG1_DN	DIFF100	3.3V	USB1 Differential Data Negative
B42	GND	-	-	Ground
B43	X_USB_OTG1_ID	IN	3.3V	USB1 ID Signal
B44	X_USB_OTG1_VBUS	PWR	5V	USB1 Power
B45	X_USB_OTG2_ID	IN	3.3V	USB2 ID Signal
B46	X_USB_OTG2_VBUS	PWR	5V	USB Power
B47	GND	-	-	Ground
B48	X_USB_OTG2_OC	IN	3.3V	USB2 Overcurrent Detection
B49	X_USB_OTG2_PWR	OUT	3.3V	USB2 Control Signal to Enable VBUS Power
B50	X_USB_OTG1_OC	IN	3.3V	USB1 Overcurrent Detection
B51	X_USB_OTG1_PWR	OUT	3.3V	USB1 Control Signal to Enable VBUS Power
B52	GND	-	-	Ground
B53	X_SPI3_MISO	IO	3.3V	SPI3 Master In Slave Out
B54	X_SPI3_MOSI	IO	3.3V	SPI3 Master Out Slave In
B55	X_SPI3_SCLK	IO	3.3V	SPI3 Clock
B56	X_SPI3_SS0	IO	3.3V	SPI3 Slave Select 0
B57	GND	-	-	Ground
B58	X_SAI1_TX_SYNC	OUT	3.3V	SAI1 Transmit Sync
B59	X_SAI1_TXD0	OUT	3.3V	SAI1 Transmit Data 0
B60	X_SAI1_MCLK	IO	3.3V	SAI1 Master Clock

3 Jumpers

The phyCORE-i.MX7 provides 18 solder jumpers for configuration purposes. These jumpers have been installed in their default configurations prior to delivery.

If manual jumper modification is required, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

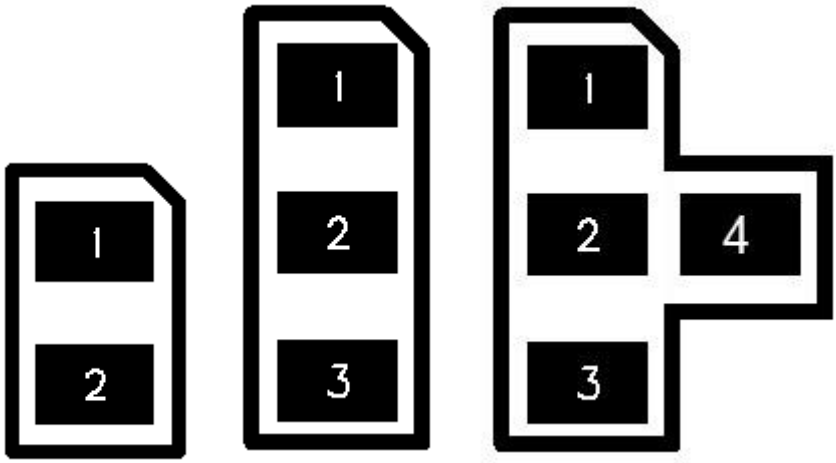

Figure 5. Jumper Numbering Schemes

The bold items in Table 4 below represent the default configuration for each jumper. The table also describes the function of each jumper as well as each alternative position. Note that each solder jumper on the phyCORE-i.MX7 should be populated with a 0-ohm 0402 resistor.

Table 4. Jumper Descriptions and Settings

Jumper	Setting	Description
J1 - J12	**Open**	**Route RGMII1 signals only to the Ethernet PHY.**
	Closed	Route RGMII1 signals out to the phyCORE connector.
J21	**1+2**	**SPI1 and UART7 operate at 1.8V.**
	2+3	SPI1 and UART7 operate at 3.3V.
J22	**1+2**	**SD3 operates at 1.8V.**
	2+3	SD3 operate at 3.3V. required for NAND population.
J23	**1+2**	**SD2 operates at 1.8V.**
	2+3	SD2 operate at 3.3V.
J24	**1+2**	**External RTC interrupt is routed to a GPIO2_04 (EPDC1_DATA04) at the processor.**
	2+3	External RTC interrupt is routed to the X_MX7_ONOFF signal to be used as a 'wake' signal.
	2+4	External RTC interrupt is routed to the PMIC PWRON pin to be used to trigger a PMIC power on event.
J25	**1+2**	**SD3 clock is routed to eMMC.**
	2+3	SD3 clock is routed to NAND.
J26	**1+2**	**SD3 strobe signal is routed to eMMC.**
	2+3	SD3 strobe signal is routed to NAND.

4 Power

The SOM has two input voltage rails and two output rails that are accessible externally via the phyCORE-Connectors. The input rails consist of the main input power, VCC_SOM, and the battery backup power, VBAT. The SOM then generates and provides both the VLDO2_1V5 rail and the SW2_1V8 rail as outputs.

The SW2_1V8 output rail is provided for sequencing external power as needed for interfacing with the various 1.8V signals. Note that SW2_1V8 is NOT intended for directly supplying devices and circuits externally. Various internal functions of the SOM are powered via SW2_1V8, so introducing an additional external load may have negative impacts on the performance of the SOM. Drawing excessive current may cause brown out conditions or potentially introduce noise. Please note the recommended maximum load current when sequencing with SW2_1V8 (refer to

Table 13).

NOTE:
It is possible to supply external devices and circuits via SW2_1V8, but caution must be taken. The power consumption of the SOM will depend on the use case and which 1.8V interfaces are implemented. If the risks are acknowledged and understood, then SW2_1V8 can supply external devices as long as the maximum current limits are adhered to. Refer to the PMIC and i.MX7 reference documentation for further information.

The recommended operating conditions of these external rails are provided in

Table 13. These power rails will be discussed in greater detail in the following sections of this chapter.

CAUTION:
As a general design rule, we recommend connecting all 3.3V input pins to your power supply and at least a matching number of ground (GND) pins. For the best EMI performance, it is recommended to connect ALL ground pins at the phyCORE-Connector (X1, X2) to a solid ground plane. At the very least a matching number of ground pins to power pins should be made, in addition to using the ground pins surrounding signals used in application circuitry. Please refer to Table 3 for the locations of all ground pins on the phyCORE-Connector.

The following sections of this chapter describe the power design of the phyCORE-i.MX7 in further detail.

4.1 Primary System Power (VCC_SOM)

The phyCORE-i.MX7 operates from a voltage supply with a nominal value of +3.3V. The PMIC and On-board switching regulators generate the voltage supplies required by the i.MX7 processor and on-board components from the 3.3V supplied to the SOM.

The phyCORE-i.MX7 requires a +3.3V (+-5%) / 3A supply at the phyCORE-connector pins X1-A56, A57, A58, A59 to guarantee enough power under all operating conditions. Your particular operating conditions may vary and require less power (refer to

Table 13). The phyBOARD-Zeta platform provides a shunt resistor as an access point for measuring the SOM current.

Connect all 3.3V input pins to your power supply and at least the matching number of GND pins.

4.2 Power Mode Management

The phyCORE-i.MX7 provides an X_MX7_ONOFF signal that allows the control of the transitions between the various power modes of the i.MX7. This signal, which is de-bounced and pulled up internally, may be connected to a switch on a baseboard to provide a mechanical means of driving the signal low. If the X_MX7_ONOFF button is driven low briefly when

the processor is in an SNVS or low power mode, the i.MX7 will transition to the RUN mode. When a 'long' press occurs on X_MX7_ONOFF in the RUN mode, the processor will transition back to the SNVS mode. The technical reference manual can be referenced for further details regarding the various power modes.

4.3 Power Management IC (U2)

The phyCORE-i.MX7 provides an on-board Power Management IC (PMIC), NXP PF3000, at position U2 to generate the voltages required by the processor and on-board components.

Figure 6 presents a graphical depiction of the SOM powering scheme.

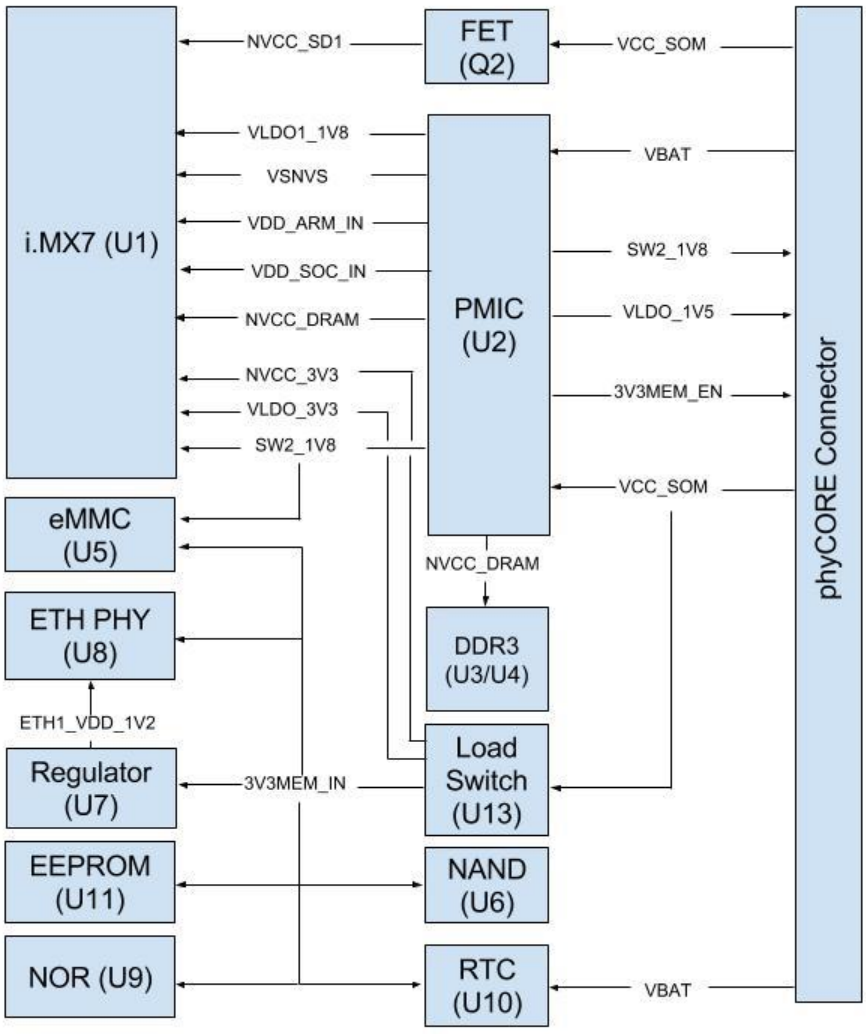

Figure 6. Power Supply Diagram

4.3.1 Power Domains

As stated before, the SOM has two input voltage rails and two output rails. The VCC_SOM input rail provides power to the PMIC, which then generates other voltage rails on the SOM. A load switch IC at U13 is used to generate the 3.3V rails used on the phyCORE-i.MX7 (VLDO3_3V3, NVCC_3V3, and 3V3MEM_IN) from VCC_SOM. This load switch is enabled by the PMIC to ensure proper power sequencing for all on-board supplies. VCC_SOM is also switched to supply the SD1 power rail NVCC_SD1 through a FET enabled by the PMIC. Refer to Table 5 below for descriptions of all of the external power supplies at the phyCORE connector.

The following tables summarize the relationships between the voltage rails and the devices on the phyCORE-i.MX7.

Table 5. External Supply Voltages

Signal	Description	Direction	Function
VCC_SOM	3.3V system power supply	IN	PMIC Power Supply
VBAT	3.0V RTC battery supply	IN	Backup power for RTC U19
VLDO2_1V5	1.5V power supply	OUT	Power rail for Mini-PCIe on Carrier Board
SW2_1V8	1.8V power supply	OUT	Reference output for sequencing

Table 6. Internal Voltage Rails

Device	Device Output	Schematic Signal	Voltage	Function
PMIC U3	VLDO1	VLDO1_1V8	1.8	i.MX7 LPSR Domain Supply
	VLDO2	VLDO2_1V5	1.5	i.MX7 Carrier Board Mini-PCIe Supply
	VSNVS	VSNVS	3.0	i.MX7 SNVS Domain Supply
	SW1A	VDD_ARM_IN	1.1	i.MX7 Core Supply Voltage
	SW1B	VDD_SOC_IN	1.0	i.MX7 Core Supply Voltage
	SW2	SW2_1V8 / NVCC_1V8	1.8	ADC Supply / Supply for NVCC_SD2 and NVCC_SD3 / i.MX7 power for analog domain and LDOs
	SW3	SW3_1V35 / NVCC_DRAM	1.35	DDR Supply Voltage
Load Switch U13	VOUT	VCC_3V3_S3	3.3	Multiple component voltage supply
Switching FET Q2	VOUT	VCC_3V3_S4	3.3	SD1 VCC

4.3.2 Power Management

The PMIC provides an input signal to control the power state of the system by generating a turn-on event. This signal is provided as X_PMIC_PWRON, and can be used to bring the PMIC out of OFF and Sleep modes into the ON mode. By default, X_PMIC_PWRON is pulled up to the VSNVS rail on the SOM. Therefore, it is recommended to implement an open-drain output to drive X_PMIC_PWRON externally. Refer to the PMIC datasheet for information on how to configure the PWRON pin.

X_3V3MEM_EN is provided as an output at the phyCORE connector to sequence an external 3.3V power rail to match the timing of VCC_3V3_S3. It is recommended to use a load switch with similar characteristics as U13 on the SOM (TPS22965) so that the external 3.3V rail is sequenced as close as possible to the internal VCC_3V3_S3 rail. This is intended for

sequencing power before the release of POR. It is recommended to use this power sequencing for configuring the boot signals on a carrier board (as these are strapped at the release of POR) and supplying memory devices (i.e. SD card).

4.3.3 External Battery (VBAT)

The SOM provides a VBAT input for applications requiring an ultra-low power RTC that retains time when VCC_SOM is removed. Connect a 3.0 V battery or other supply to the VBAT input at pin X1-B57. VBAT voltage should not exceed the VCC_SOM supply. The RTC will continue to maintain its time down to approximately 1.0V on the VBAT pin.

The VBAT rail also supplies the LICELL pin on the PMIC, allowing for the connection of a coin cell backup battery or super capacitor. If VCC_SOM goes below the V_{IN} threshold of the PMIC or is removed, the VBAT voltage supplied to the LICELL pin will be switched to maintain power for the internal logic and the VSNVS rail. If VBAT is not present or disconnected, then the memory will be cleared and VSNVS will be turned off. To prevent this, the VBAT rail should supply the LICELL pin with a voltage between 1.8V and 3.0V.

For applications that do not require the external RTC backup or PMIC Coin Cell operation, VBAT can be left floating.

5 Real-Time Clock (RTC)

There are two options for an RTC on the phyCORE-i.MX7: the on-chip RTC or an external on-board RTC. If cost is the primary concern, then the on-chip RTC should be considered to minimize external components. However, if power is the primary concern, then consider using the external RTC to reduce power consumption. Typical VBAT power consumption measurements for the RTC configuration options are provided in Table 7. The following sections detail these two RTC options.

Table 7. Typical VBAT Power Consumption

RTC Configuration	I_{VBAT} Typ. (uA)
Internal RTC Powered with External RTC Disconnected	34.99
External RTC Powered and Internal RTC Disconnected	1.32
Internal and External RTCs Powered	36.12

5.1 i.MX7 RTC

The i.MX7 processor includes an integrated RTC. However, the RTC integrated in the i.MX7 uses more power than the external RTC on the SOM. Refer to the technical reference manual for further information.

5.2 External RTC

The SOM provides an ordering option to populate an external RTC at U10 which is connected to the I2C1 bus at address 0x68. The external RTC uses less power than the i.MX7 internal RTC, and can be used when very-low battery power is critical. The external RTC typically uses 350nA at 3V. In order for the external RTC to maintain time when main system power is removed, the VBAT input must be supplied with power. To achieve the lowest power consumption, resistor R172 must be removed to disconnect the PMIC VBAT backup supply. This can be accomplished via hand rework, or for series production this component can be configured to be removed.

Jumper J24 is provided to configure the various interrupt options for the external RTC. By default, J24 is set to 1+2 so that the interrupt is routed to a GPIO at the processor (pad EPDC1_DATA04).

Setting jumper J24 to 2+3 routes the interrupt to the X_MX7_ONOFF signal to be used as a ‘wake’ signal. Implement this configuration for applications that use the RTC interrupt to transition the processor from a low power mode to RUN mode.

The jumper can also be set to 2+4 to route the interrupt to the PMIC PWRON pin to be used to trigger a PMIC power on event. This configuration drives the PWRON input pin at the PMIC, allowing the RTC to bring the PMIC out of OFF and Sleep modes. Use this configuration for applications that require the RTC interrupt to turn on the PMIC.

6 System Configuration and Booting

Although most features of the i.MX7 microcontroller are configured or programmed during the initialization routine, other features which impact program execution must be configured prior to initialization via pin termination. During the power-on reset cycle the operational system boot mode of the i.MX7 processor is determined by the configuration of the BOOT_CFG [19:0] pins. These signals are named X_LCD1_DATA#_BOOT# at the phyCORE connector. The pull-up and pull-down resistors populated on the SOM set the default BOOT_CFG [19:0] configuration to 0b0000 0001 0011 0001 0000.

For development and debugging purposes, the LCD1_DATA boot pins are all available at the phyCORE connector. However, PHYTEC can provide the SOM with any specific boot configuration for final production. To modify the default boot configuration on a Carrier Board, it is recommended to use 1k pull-up or pull-down resistors to override the SOM settings. Please note that after booting up, these signals are used to transmit data via the LCD1 display interface.

For more information about pad multiplexing configuration please refer to NXP i.MX7 Technical Reference Manual.

6.1 Boot Mode Pin Settings

Table 8 describes the boot mode configuration controlled by X_BOOT_MODE[1:0]. By default, the boot mode pins are strapped to set the boot mode to Internal Boot. For further detail regarding the boot mode settings, please refer to the NXP i.MX7 Technical Reference Manual.

Table 8. Boot Mode Configuration[5]

BOOT_MODE[1:0]	Boot Type
00	Boot from Fuses
01	Serial Downloader
10	**Internal Boot**
11	Reserved for NXP use

6.2 Boot Device Selection

Table 9 describes the external boot devices that are supported by the phyCORE-i.MX7. By default, the boot device is set to SD.

Table 9. Boot Device Selection[5]

BOOT_CFG[15:12]	Boot Device
0001	**SD/eSD/SDXC**
0010	MMC/eMMC
0011	Raw NAND
0100	QSPI

[5] Default settings are in **bold** text

6.3 Boot Device Configuration

Table 10 shows the default boot configuration selected by the phyCORE-i.MX7 default boot strapping. For detailed information regarding all supported boot device configurations, please refer to the NXP i.MX7 Technical Reference Manual.

Table 10. SD/MMC Boot Configuration Description[5]

BOOT_CFG Latching Signal	Definition	Setting
X_LCD1_DATA[15:12]_BOOT[15:12]	Boot Device Selection	**0001 – SD/eSD/SDXC** 0010 – MMC/eMMC
X_LCD1_DATA[11:10]_BOOT[11:10]	SD Port Selection	**00 – USDHC-1** 01 – USDHC-2 10 – USDHC-3
X_LCD1_DATA[9]_BOOT[9]	SD Power Cycle Enable	0 – Disabled **1 – Enabled**
X_LCD1_DATA[8]_BOOT[8]	Loopback Clock Selection	0 – Through SD Pad **1 – Direct**
X_LCD1_DATA[7]_BOOT[7]	Fast Boot Support	**0 – Normal Boot** 1 – Fast Boot
X_LCD1_DATA[6:4]_BOOT[6:4]	Bus Width	0 – 1-bit **1 – 4-bit**
X_LCD1_DATA[3:1]_BOOT[3:1]	Speed	000 – Normal **001 – High** 010 – SDR50 001 – SDR104
X_LCD1_DATA[0]_BOOT[0]	USDHC2 IO Voltage	**0 – 3.3V** 1 – 1.8V

7 System Memory

The phyCORE-i.MX7 provides five types of on-board memory:

- DDR3 SDRAM
- eMMC or NAND FLASH
- SPI NOR FLASH
- I^2C EEPROM

NOTE:
The phyCORE-i.MX7 does not support the use of eMMC and NAND flash storage at the same time. Only one of the storage devices can be populated on the SOM at any given time. Additional NAND or eMMC devices need to be implemented on the Carrier Board.

The following sections of this chapter detail each memory type used on the phyCORE-i.MX7.

7.1 DDR3 SDRAM (U3, U4)

The RAM memory on the phyCORE-i.MX7 is comprised of two 16-bit wide DDR3 SDRAM chips for a 32-bit wide interface providing up to 2GB of SDRAM. These chips are connected to the dedicated DDR controller of the i.MX7 processor.

Typically, the DDR3 SDRAM initialization is performed by a boot loader or operating system following a power-on reset and must not be changed at a later point by any application code. When writing custom code independent of an operating system or boot loader, SDRAM must be initialized through the appropriate SDRAM configuration registers on the i.MX7 controller. Refer to the i.MX7 Technical Reference Manual about accessing and configuring these registers.

7.2 eMMC (U5) and NAND Flash (U6) Memory

The phyCORE-i.MX7 can be populated with either an eMMC or NAND flash as an easy to program nonvolatile memory solution. The phyCORE-i.MX7 does not support the use of both eMMC (U5) and NAND (U6) simultaneously. Only one of these can be populated on the SOM. If it is necessary to support both NAND and eMMC, additional NAND or eMMC devices can be implemented on a Carrier Board.

The eMMC flash is connected to the SD/MMC3 interface of the i.MX7 with a bus width of 8-bits, supporting up to 128GB of eMMC.

NAND flash is supported via the RawNAND interface (multiplexed via the SD/MMC3 interface on the phyCORE-i.MX7) with an 8-bit bus width, supporting up to 8GB of NAND.

7.3 I^2C EEPROM (U11)

The phyCORE-i.MX7 can be populated with a nonvolatile 4KB EEPROM with an I^2C interface as an ordering option. This memory can be used to store configuration data or other general purpose data. This device is accessed through I^2C port 1 on the i.MX7 at address 0x50.

7.4 QSPI NOR Flash Memory (U9)

The phyCORE-i.MX7 can be populated with a SPI Flash memory device via the QSPI_A bus as an ordering option. This would be suitable for applications which require a small code footprint or small RTOS.

Using a SPI Flash can eliminate the need to install NAND Flash or eMMC memory on the SOM. This could reduce BOM costs, free up the NAND signals for other muxing options, and remove the need for the bad block management that is required when using NAND Flash.

7.5 Memory Model

There is no special address decoding device on the phyCORE-i.MX7, therefore the memory model is given according to the memory mapping of the i.MX7. Please refer to the i.MX7 Technical Reference Manual for the memory map.

8 SD/MMC Card Interfaces

The phyCORE-i.MX7 provides three SD/MMC interfaces: SD/MMC1-3. SD/MMC1 and SD/MMC2 are provided at the phyCORE connector directly from the processor. These two ports allow support for external SD/MMC devices, such as an SD card or a WiFi/Blueooth module, and are provided with 22 Ohm source termination resistors on the SOM. The SD/MMC3 interface is used to interface with an on-board flash device, either eMMC at U5 or NAND at U6 depending on the SOM configuration (see Section 7.2).

9 Serial Interfaces

The i.MX7 provides numerous serial interfaces, some of which are provided with an on-board transceiver for direct connection to external devices. Only a subset of the interfaces are brought out of the phyCORE connector as the phyCORE-i.MX7 default multiplexing configuration. The following sections describe the default interfaces on the phyCORE-i.MX7. Additional interfaces can be accessed through alternate muxing configurations. Please refer to NXP's technical reference manual for more information on pin muxing options.

9.1 USB

The phyCORE-i.MX7 provides two USB 2.0 OTG interfaces with integrated USB PHYs. Typically, an external USB connector is all that is needed for USB functionality. However, USB power switch circuits can be implemented on a baseboard to add additional VBUS enable and over-current detection functionality.

An additional HSIC USB 2.0 port is available with an integrated HSIC USB PHY.

9.2 Ethernet

The phyCORE-i.MX7 can connect to a LAN via two i.MX7 embedded 10/100/1000 Ethernet controllers. The Ethernet controllers are available through two ports: Ethernet1 and Ethernet2. Both ports provide MII/RMII/RGMII signals from the processor and require an external Ethernet PHY for connection to a physical network. The SOM provides the option of an Ethernet PHY on Ethernet1, but not on Ethernet2. Ethernet2 is only available at the phyCORE-Connector via the MII/RMII/RGMII signals.

9.2.1 Ethernet1

The phyCORE-i.MX7 can be populated with a 10/100/1000Base-T Ethernet transceiver PHY at U8, allowing direct connection to an RJ-45 connector with integrated magnetics. See Table 3 for the locations of the Ethernet1 signals on the phyCORE-Connector. All Ethernet1 signals are labeled as X_ETH1… on the connector.

The KSZ9031 transceiver supports HP Auto MDIX technology, eliminating the need for the consideration of a direct connect LAN cable, or a cross over patch cable.

Special routing, layout, and other circuit design considerations should be followed by referencing the phyCORE-i.MX7 Carrier Board schematics.

CAUTION:
Please reference the KSZ9031 Ethernet Transceiver datasheet when designing the Ethernet transformer circuitry.

9.2.2 Ethernet2

The i.MX7 Ethernet2 interface signals can connect to any industry standard Ethernet transceiver or configured for other multiplex functionality. The i.MX7 supports MII, RMII, and RGMII modes on the interface. GMII is not supported by the processor.

It is strongly recommended to place the Ethernet PHY on the Carrier Board as close as possible to the RGMII2 pins at the phyCORE connector to achieve a trace length of less than 100mm. Please refer to the datasheet of the chosen Ethernet transceiver for more information regarding signal timings. Additional routing, layout, and other circuit design considerations should be followed by referencing the phyCORE-i.MX7 Carrier Board schematics.

For signal integrity purposes, source termination resistors are placed on the output signals of the RGMII2 interface on the SOM.

9.3 I²C

The phyCORE-i.MX7 provides four independent I²C buses at the phyCORE connector directly from the processor. I2C1, I2C2, I2C3, and I2C4. The I2C1 bus is pulled up to the NVCC_3V3 rail via 2.2KOhm resistors and connects to the PMIC (U2), EEPROM (U11), and RTC (U10). I2C2-4 require external pull-up resistors on custom Carrier Board designs. The following table shows the reserved addresses for the internal components of the phyCORE-i.MX7.

Table 11. I2C1 Reserved Addresses

Device	Address
RTC	0x68
EEPROM	0x50
PMIC	0x08
	0x09
	0x0A
	0x0B
	0x0C
	0x0D
	0x0E
	0x0F

9.4 PCI Express

The phyCORE-i.MX7 provides a single lane PCI Express Gen 2.0 interface with an integrated PHY supporting a data rate up to 5Gbps. The PCIe reference clock into the processor is provided by an external 100MHz oscillator circuit with HCSL termination. Coupling capacitors are not provided on the SOM for the differential TX data signals. These TX coupling capacitors should be implemented on a carrier board.

A 1.5V supply rail (VLDO2_1V5) is provided at the phyCORE-Connector from the PMIC to support Mini-PCI Express on a carrier board). This 1.5V rail can provide a load current of up to 250mA.

NOTE:
According to the PCI Express Mini Card Electromechanical Specification the maximum peak current for the 1.5V rail is 500mA. Not all devices will need this maximum load current, or even utilize the 1.5V rail. However, if the 250mA supplied by the PMIC rail is not sufficient, a regulator should be implemented on a carrier board to provide 1.5V from the main system power.

Refer to the i.MX7 Technical Reference Manual for further details regarding PCI Express.

10 Debug Interface

The phyCORE-i.MX7 is equipped with a JTAG interface for downloading program code into the internal RAM or for debugging programs currently executing. The JTAG interface is accessible via the phyCORE-Connectors.

Please reference the NXP documentation for further information regarding the JTAG interface.

11 Technical Specifications

The physical dimensions of the phyCORE-i.MX7 are represented in Figure 7. The module's profile is approximately 5.4 mm thick from the tallest component on the top to the tallest component on the bottom (excluding the phyCORE connectors). The maximum component height (excluding connectors X1 and X2) is approximately 1.9 mm on the bottom (connector) side of the PCB and approximately 2 mm on the top (microcontroller) side. The PCB is approximately 1.5 mm thick. The distance from the surface of the Carrier Board to the highest component on the top side of the board is approximately 8.55 mm.

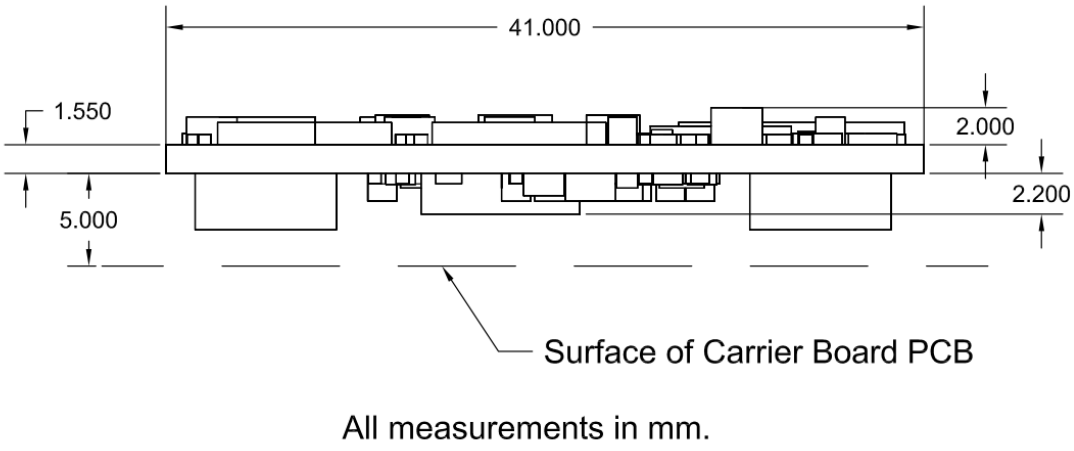

Figure 7. phyCORE-i.MX7 Mechanical Dimensions (profile view)

Table 12. Technical Specifications

Dimensions:	41 mm x 50 mm
Mass:	13.01 g[6]
Storage Temperature:	-40C to +85C
Operating Temperature:	-20C to +85C[7]
Humidity:	TBD
Typ. Idling Power Consumption:	1 W

Table 13. Recommended Operating Conditions for the Input and Output Power Domains

Symbol	Description	Conditions	Min	Typ	Max	Unit
VCC_SOM	3.3V SOM input voltage		3.14	3.3	3.46	VDC
VLDO2_1V5	1.5V Output Voltage		0.8	1.5	1.55	VDC
SW2_1V8	1.8V Output Voltage		1.5	1.8	1.85	VDC
VBAT	Battery backup for RTC		1	3	3.3[8]	VDC
I_{VCC_SOM}	3.3V SOM operating current	Idle in Linux with external interfaces down/disconnected (except for Serial RS-232 and SD card)	-	170	-	mA
		Measured while testing the following interfaces/devices simultaneously via a python test script in Linux: - ETH1/ETH2 (iperf test) - USB1/USB2 (bandwidth test) - LCD Display - RS232 - Mini-PCIe via StarTech Gigabit ethernet adapter card - CAN via PCAN-View - Memtester - RTC - EEPROM - eMMC - SD	-	730	-	mA
I_{VLDO2_1V5}	1.5V Output load current		-	-	250	mA
I_{SW2_1V8}	1.8V Output load current	Not intended for directly supplying 1.8V externally. Use only to sequence additional 1.8V power supplies.	-	-	10	mA
I_{VBAT}	Battery backup operating current	Internal RTC Powered with External RTC Disconnected	-	34.99	-	uA
		External RTC Powered with Internal RTC Disconnected	-	1.32	-	uA
		Internal and External RTCs Powered	-	36.12	-	uA

[6] The mass is calculated by averaging the measurements of 4x PCM-061.A4 units using a digital scale

[7] Temperature range will depend on the processor ordered with the PHYTEC SOM; the minimum temperature will be limited to 0C if using the MCIMX7D7DVK10SC, which is rated for 0C to +95C

[8] The VBAT rail should never exceed the VCC_SOM supply

12 Hints for Integrating and Handling the phyCORE-i.MX7

12.1 Integrating the phyCORE-i.MX7

Successful integration of the phyCORE-i.MX7 SOM into target circuitry greatly depends on adherence to the layout design rules for the GND connections of the phyCORE module. As a general design rule, we recommend connecting all GND pins neighboring signals which are being used in application circuitry. At least one ground pin should be connected for every power pin used. For maximum EMI performance, all GND pins should be connected to a solid ground plane.

Additional information is available to facilitate the integration of the phyCORE-i.MX7 into customer applications, such as:

- phyCORE-i.MX7 Carrier Board schematic reference. Schematics are made available upon request.
- phyCORE-iMX7 Pins file: http://develop.phytec.com/display/public/PRODUCTINFO/phyCORE-i.MX7#Landing-409943289
- Phone, e-mail, FAQ, wiki, and other online support by visiting http://phytec.com/contact/

12.2 Handling the phyCORE-i.MX7

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

WARNING:
Modifications to the SOM, regardless of their nature, will void the warranty.

13 Revision History

Table 14. Revision History

Date	Version Number	Changes in this Manual
2016/06/03	L-821e_0	Preliminary Release
2017/01/13	L-821e_1	Revised explanation of X_3V3MEM_IN and X_3V3MEM_EN. Added 3V3MEM_EN to Power Diagram (Figure 6). Updated pin description for the X_nWDOG_RST soft reset signal. Revised explanation of SW2_1V8 to explicitly recommend only using it for external sequencing. Fixed table numbering. Updated average mass measurement using 4x PCM-061.A4 units.
2017/05/24	L-821e_2	Added mechanical dimensions drawing. Added reference to pin mux file. Revised pin description table. Explicitly describe the signals that can be set as either 1.8V or 3.3V. Revised Table 4 to include UART7 under the J21 jumper description. Updated VCC_SOM operating current values in Table 13. Updated explanation of SW2_1V8 under the Power section. Added option tree ordering information.
2017/12/14	L-821e_3	Updated operating and storage temperature ranges.
2017/05/16	L-821e_4	Revised the wording in the Ethernet section to clarify that two Gigabit Ethernet controllers are provided rather than a ‘switch’.