phyCORE®-AM57x

Hardware Manual

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Conventions, Abbreviations and Acronyms

This hardware manual describes the PCM-057 System on Module in the following referred to as phyCORE-AM57x. The manual specifies the phyCORE-AM57x's design and function. Precise specifications for the Texas Instruments AM57x microcontrollers can be found in Texas Instrument's AM57x Data Sheet and Technical Reference Manual.

NOTE:
The BSP delivered with the phyCORE-AM57x usually includes drivers and/or software for controlling all components such as interfaces, memory, etc. Therefore, programming close to hardware at register level is not necessary in most cases. For this reason, this manual contains no detailed description of the controller's registers, or information relevant for software development. Please refer to the AM57x Reference Manual if such information is required.

Conventions

The conventions used in this manual are as follows:

- Signals that are preceded by an "n", "/", or “#” character (e.g.: nRD, /RD, or #RD), or that have a dash on top of the signal name (e.g.: RD) are designated as active low signals. That is, their active state is when they are driven low, or are driving low.
- A "0" indicates a logic zero or low-level signal, while a "1" represents a logic one or high-level signal.
- The hex-numbers given for addresses of I^2C devices always represent the 7 MSB of the address byte. The correct value of the LSB which depends on the desired command (read (1), or write (0)) must be added to get the complete address byte. E.g. given address in this manual 0x41 => complete address byte = 0x83 to read from the device and 0x82 to write to the device.
- Tables which describe jumper settings show the default position in **bold text**
- Text in blue italic indicates a hyperlink within, or external to the document. Click these links to quickly jump to the applicable URL, part, chapter, table, or figure.
- References made to the phyCORE-Connector always refer to the high density Samtec connectors on the undersides of the phyCORE-AM57x

Abbreviations and Acronyms

Many acronyms and abbreviations are used throughout this manual. Use the table below to navigate unfamiliar terms used in this document.

Table 1. Abbreviations and Acronyms used in this Manual

Abbreviation	Definition
BSP	Board Support Package (Software delivered with the Development Kit including an operating system (Windows or Linux) preinstalled on the module and Development Tools).
CB	Carrier Board; used in reference to the phyCORE-AM57x Development Kit Carrier Board.
DFF	D flip-flop
EMB	External memory bus
EMI	Electromagnetic interference
GPI	General purpose input
GPIO	General purpose input and output
GPO	General purpose output

Abbreviation	Definition
IRAM	Internal RAM; the internal static RAM on the Texas Instruments AM57x microcontroller
J	Solder jumper; these types of jumpers require solder equipment to remove and place
JP	Solderless jumper; these types of jumpers can be removed and placed by hand with no special tools
PCB	Printed circuit board
PDI	PHYTEC Display Interface; defined to connect PHYTEC display adapter boards, or custom adapters
PEB	PHYTEC Extension Board
PMIC	Power management IC
POR	Power-on reset
RTC	Real-time clock
SMT	Surface mount technology
SOM	System on Module; used in reference to the PCM-057 / phyCORE-AM57x System on Module
Sx	User button Sx (e.g. S1, S2, etc.) used in reference to the available user buttons, or DIP switches on the Carrier Board
Sx_y	Switch y of DIP switch Sx; used in reference to the DIP switch on the Carrier Board
VBAT	SOM standby voltage input

Different types of signals are brought out at the phyCORE-Connector. The following table lists the abbreviations used to specify the type of a signal.

Table 2. Types of Signals

Type of Signal	Description	Abbr.
Power	Supply voltage	PWR
Ref-Voltage	Reference voltage	REF
USB-Power	USB voltage	USB
Input	Digital input	IN
Output	Digital output	OUT
Input with pull up	Input with pull-up, must only be connected to GND (jumper or open-collector output).	IPU
Input / output	Bidirectional input / output	IO
5V Input with pulldown	5V tolerant input with pull-down	5V_PD
5V Input with pull-up	5V tolerant input with pull-up	5V_PU
3.3V Input with Pull-up	3.3V tolerant input with pull-up	3V3_PU
3.3V Input with pull-down	3.3V tolerant input with pull-down	3V3_PD
LVDS	Differential line pairs 100 Ohm LVDS	LVDS
Differential 90 Ohm	Differential line pairs 90 Ohm	DIFF90
Differential 100 Ohm	Differential line pairs 100 Ohm	DIFF100
Analog	Analog input or output	Analog

Preface

This phyCORE-AM57x Hardware Manual describes the System on Module's design and functions. Precise specifications for the Texas Instruments AM57x processor can be found in the processor datasheet and/or technical reference manual (TRM).

Declaration of Electro Magnetic Conformity of the PHYTEC phyCORE-AM57x System On Module

PHYTEC System on Modules (SOMs) are designed for installation in electrical appliances or, combined with the PHYTEC Carrier Board, can be used as dedicated Evaluation Boards (for use as a test and prototype platform for hardware/software development) in laboratory environments.

CAUTION:
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

NOTE:
Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The phyCORE-AM57x is one of a series of PHYTEC System on Modules that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports a variety of 8-/16- and 32-bit controllers in two ways:

1. As the basis for Rapid Development Kits which serve as a reference and evaluation platform.
2. As insert-ready, fully functional phyCORE OEM modules, which can be embedded directly into the user's peripheral hardware design.

Implementation of an OEM-able SOM subassembly as the "core" of your embedded design allows you to focus on hardware peripherals and firmware without expending resources to "re-invent" microcontroller circuitry. Furthermore, much of the value of the phyCORE module lies in its layout and test.

Production-ready Board Support Packages (BSPs) and Design Services for our hardware further reduce development time and expenses. Take advantage of PHYTEC products to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks. For more information go to:

http://phytec.com/contact/

Product Change Management

In addition to our HW and SW offerings, the buyer will receive a free obsolescence maintenance service for the HW provided when purchasing a PHYTEC SOM.

Our Product Change Management Team of developers is continuously processing all incoming PCN's (Product Change Notifications) from vendors and distributors concerning parts which are being used in our products. Possible impacts to the functionality of our products, due to changes of functionality or obsolesce of a certain part, are evaluated in order to take the right measures in purchasing or within our HW/SW design.

Our general philosophy here is: We never discontinue a product as long as there is demand for it. Therefore a set of methods has been established to fulfill our philosophy:

Avoidance Strategies

- Avoid changes by evaluating longevity of a parts during design-in phase.
- Ensure availability of equivalent second source parts.
- Maintain close contact with part vendors for awareness of roadmap strategies.

Change Management in Case of Functional Changes

- Avoid impacts on Product functionality by choosing equivalent replacement parts.
- Avoid impacts on Product functionality by compensating changes through HW redesign or backward compatibility

SW Maintenance

- Provide early change notifications concerning functional relevant changes of our Products.

Change Management in Rare Event of an Obsolete and Non-Replaceable Part

- Ensure long term availability by stocking parts through last time buy management, according to product forecasts.
- Offer long term frame contract to customers.

We refrain from providing detailed, part-specific information within this manual, which is subject to changes, due to ongoing part maintenance for our products.

Part I: PCM-057/phyCORE-AM57x System on Module

Part I of this three-part manual provides detailed information on the phyCORE-AM57x System on Module (SOM) designed for custom integration into customer applications. The information in the following chapters is applicable to the 1428.3 PCB revision of the phyCORE-AM57x SOM.

1 Introduction

The phyCORE-AM57x belongs to PHYTEC's phyCORE System on Module family. The phyCORE SOMs represent the continuous development of PHYTEC System on Module technology. Like its mini-, micro- and nanoMODULE predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware development.

Independent research indicates that approximately 70% of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments. The phyCORE board design features an increased pin package that allows dedication of approximately 20% of all connector pins on the phyCORE boards to ground. This improves EMI and EMC characteristics, making it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD components and laser-drilled microvias are implemented, providing phyCORE users with access to this cutting-edge miniaturization technology for integration into their own design.

The phyCORE-AM57x is a subminiature (45 mm x 55 mm) insert-ready System on Module populated with the Texas Instruments AM57x microcontroller. Its universal design enables its insertion in a wide range of embedded applications. All controller signals and ports extend from the controller to high-density pitch (0.5 mm) connectors aligning two sides of the board, allowing it to be inserted like a "big chip" into a target application.

Precise specifications for the controller populating the board can be found in the applicable controller Technical Reference Manual or datasheet. The descriptions in this manual are based on the Texas Instruments AM57x. A description of compatible microcontroller derivative functions is not included, as such functions are not relevant for the basic functioning of the phyCORE-AM57x.

The phyCORE-AM57x offers the following features:

- Insert-ready, sub-miniature (45 mm x 55 mm) System on Module (SOM) subassembly in low EMI design, achieved through advanced SMD technology
- Populated with the Texas Instruments AM57x microcontroller (23 x 23mm, 0.8-mm Pitch, 760 Pin BGA)
- Dual ARM® Cortex™-A15 at max. 1.5 GHz clock frequency
- Dual C66x DSP
- Dual PRU-ICSS
- Dual ARM® Cortex™-M4 (general purpose usage)
- Image and Video Accelerator IVA-HD 1080p
- 3D Graphics Processing Unit (SGX544)
- 2D Graphics Accelerator (GC320)
- Boot from eMMC, NAND Flash, or SPI Flash
- General-Purpose Memory Controller Bus (GPMC): flexible 8/16-bit asynchronous memory interface with up to 8 chip-select signals.
- Up to 4 GB DDR3/3L (2 GB w/ECC)
- Up to 2 GB NAND or 32 GB eMMC
- Up to 32 KB EEPROM
- Up to 32 MB QSPI NOR
- 2x High speed MMC/SD/SDIO
- 2x PCIe Gen2
- SATA/SATA2 up to 3Gbps

- 8x UARTs at TTL level
- 5x I^2C
- 6x MCASP Audio ports
- 4x SPI
- 2x DCAN
- 1x USB 3.0 Dual Role and 1 USB 2.0 Dual Role
- 1x 10/100/1000 MBit Ethernet interface with on SOM Ethernet PHY allowing for direct connection to an Ethernet network
- 1x 10/100/1000 RGMII Ethernet interface. The TTL-level interface is available at the phyCORE connector.
- 3x LCD Interface Display Driver with an integrated touch interface and up to 24 data bits at 1080p Full HD (1920x1080)
- 1x HDMI at 1080p Full HD (1920x1080)
- 3x Parallel camera interfaces
- On-board power management IC with integrated RTC
- Support of standard 20 pin debug interface through JTAG connector
- Ultra-low power off-chip RTC
- Watchdog Timer, PWM, GPIO, and Keyboard

1.1 Block Diagram

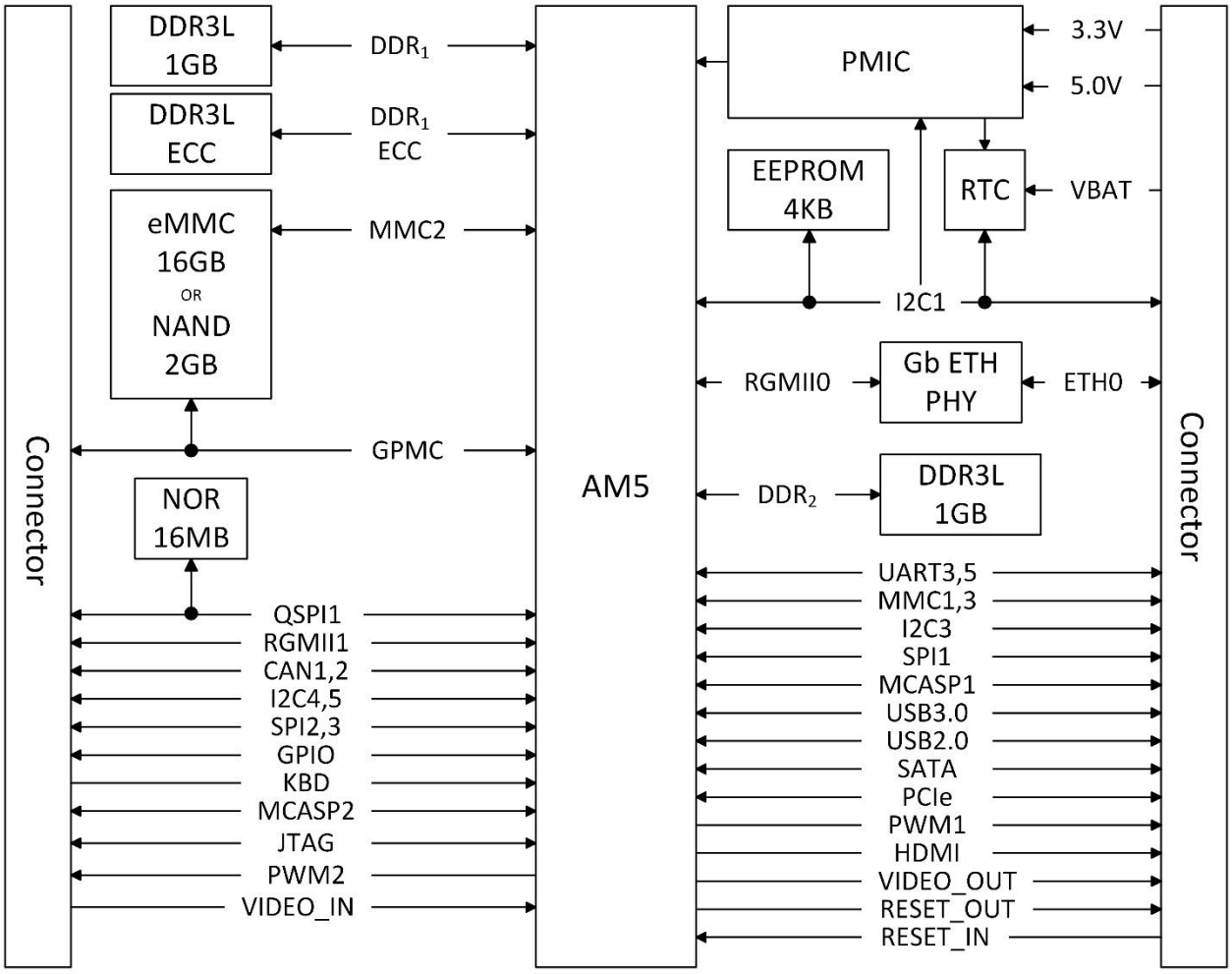

Figure 1. phyCORE-AM57x Block Diagram

1.2 Component Placement Diagram

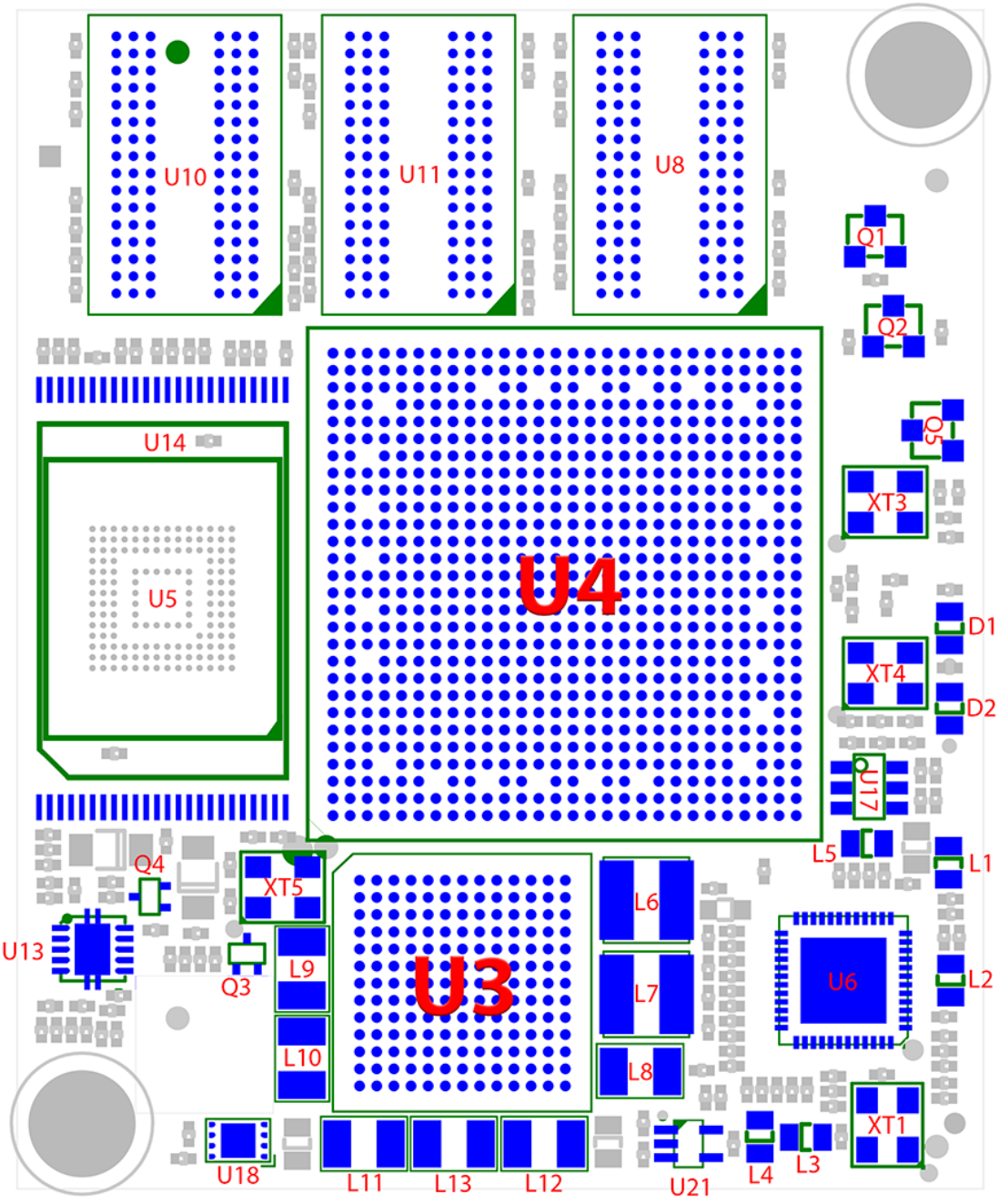

Figure 2. phyCORE-AM57x Component Placement (top view)

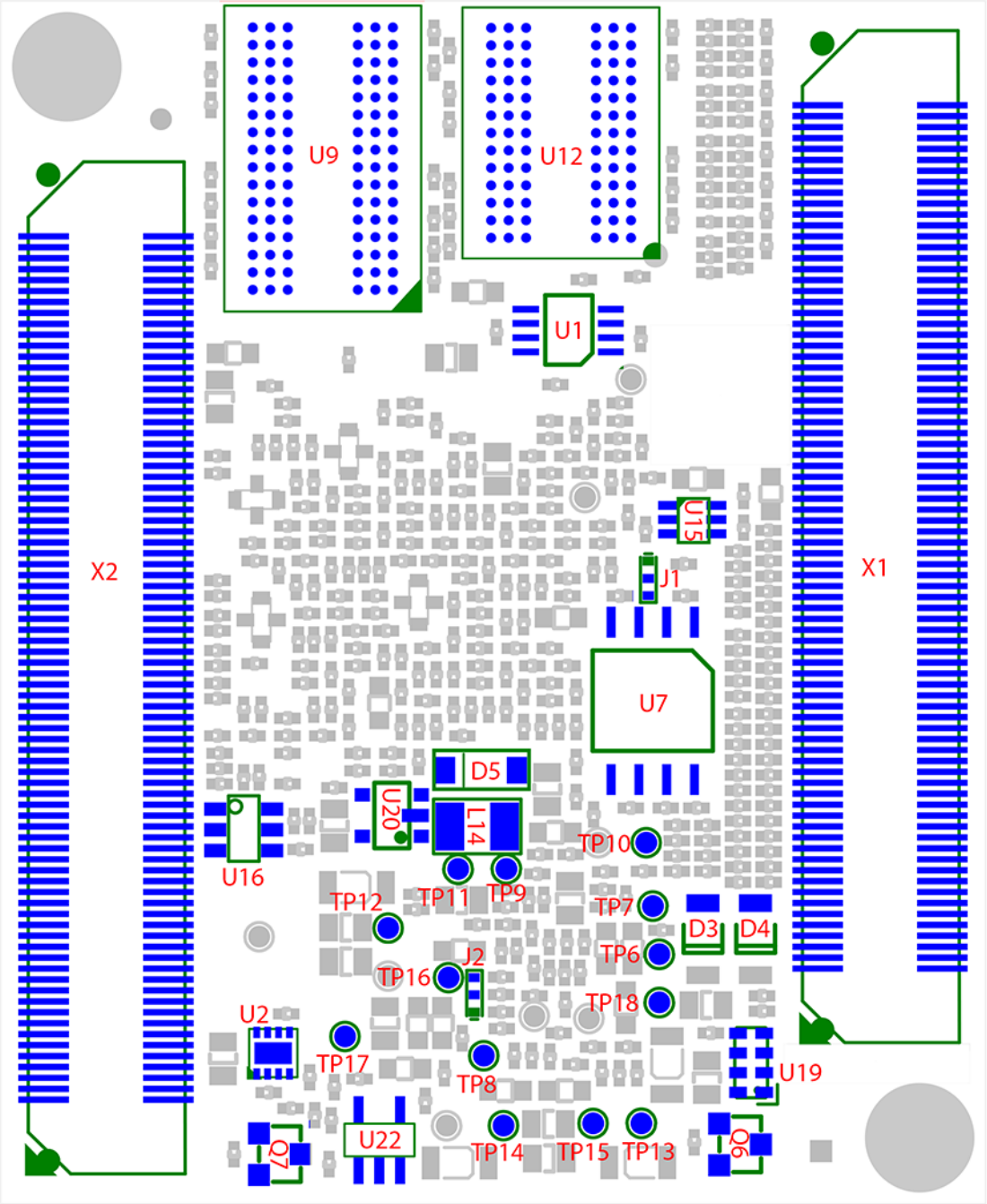

Figure 3. phyCORE-AM57x Component Placement (bottom view)

2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

All controller signals extend to surface mount technology (SMT) connectors (0.5 mm) lining two sides of the module (referred to as the phyCORE-Connector). This allows the phyCORE-AM57x to be inserted into any target application like a "big chip".

The numbering scheme for the phyCORE-Connector is based on a two-dimensional matrix in which column positions are identified by a letter and row position by a number. Pin 1A, for example, is located in the lower right hand corner of the matrix looking down through the top of the SOM. The pin numbering values decrease moving down on the board. Lettering of the pin connector columns progresses alphabetically from right to left for each connector (refer to Figure 4).

The numbered matrix can be aligned with the phyCORE-AM57x (viewed from above; phyCORE-Connector pointing down) or with the socket of the corresponding phyCORE Carrier Board/user target circuitry. The lower right-hand corner of the numbered matrix (pin A1) is thus covered with the corner of the phyCORE-AM57x marked with a triangle. The numbering scheme is always in relation to the PCB as viewed from above, even if all connector contacts extend to the bottom of the module.

The following figure illustrates the numbered matrix system. It shows a phyCORE-AM57x with SMT phyCORE Connectors on its underside (defined with dotted lines) as it would be mounted on a Carrier Board. To facilitate understanding of the pin assignment scheme, the diagram presents a cross-view of the phyCORE-module showing these phyCORE-Connectors mounted on the underside of the module’s PCB.

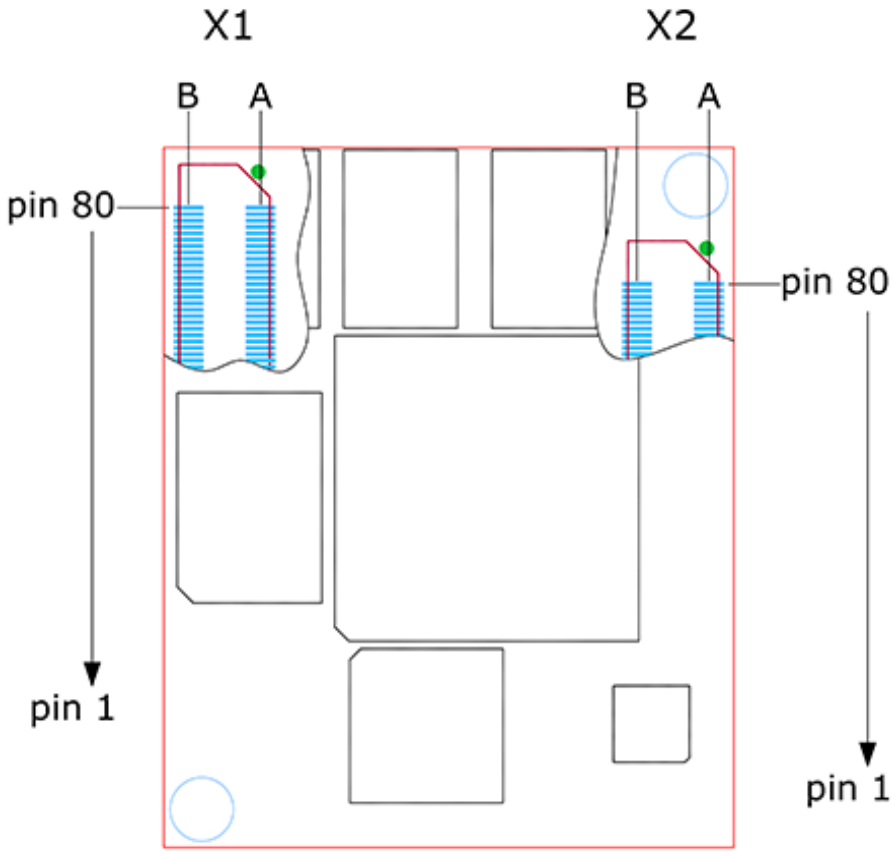

Figure 4. Pinout of the phyCORE-Connector (top view, with cross section insert)

Table 3 provides an overview of the pinout of the phyCORE-Connector with signal names and descriptions specific to the phyCORE-AM57x. It also provides the appropriate signal level interface voltages listed in the Level column, along with the signal direction.

CAUTION:
Most of the controller pins have multiple multiplexed functions. Because most of these pins are connected directly to the phyCORE-Connector the functions are also available at the connector. Signal names and descriptions in Table 3, however, are regarding the specification of the phyCORE-AM57x and the functions defined therein. Please refer to the AM57x datasheet, or the schematic to learn about alternative functions. To utilize a specific pin's alternative, function the corresponding registers must be configured within the appropriate driver of the BSP. To support all features of the phyCORE-AM57x Carrier Board a few changes have been made in the BSP delivered with the module.

The Texas Instruments AM57x is a multi-voltage operated microcontroller and as such special attention should be paid to the interface voltage levels to avoid unintentional damage to the microcontroller and other on-board components. Please refer to the Texas Instruments AM57x Reference Manual for details on the functions and features of controller signals and port pins.

Table 3. phyCORE-Connector (X1, X2) Pin-Out Description

X1, Column A				
Pin #	**Signal**	**Type**	**Level**	**Description**
A1	X_DCAN1_RX	IN	3.3V	DCAN Receive Signal
A2	X_DCAN1_TX	OUT	3.3V	DCAN Transmit Signal
A3	X_QSPI1_RTCLK	IN		QSPI return clock, the qspi1_sclk output must be connected to the qspi1_rtclk input, and is used for controlling the timing of the read return data.
A4	GND	-	-	
A5	X_QSPI1_D3	IN	3.3V	QSPI data input
A6	X_QSPI1_D2	IN	3.3V	QSPI data input
A7	X_QSPI1_D0	IO	3.3V	QSPI data input/output
A8	X_QSPI1_D1	IN	3.3V	QSPI data input
A9	GND	-	-	Ground 0 V
A10	X_GPMC_AD4/ SYSBOOT4	IO	3.3V	General Purpose Memory Controller Interface Address/Data
A11	X_GPMC_AD5/ SYSBOOT5	IO	3.3V	General Purpose Memory Controller Interface Address/Data
A12	X_GPMC_AD6/ SYSBOOT6	IO	3.3V	General Purpose Memory Controller Interface Address/Data
A13	X_GPMC_AD7/ SYSBOOT7	IO	3.3V	General Purpose Memory Controller Interface Address/Data
A14	GND	-	-	Ground 0 V
A15	X_GPMC_AD12/ SYSBOOT12	IO	3.3V	General Purpose Memory Controller Interface Address/Data
A16	X_GPMC_AD13/ SYSBOOT13	IO	3.3V	General Purpose Memory Controller Interface Address/Data
A17	X_GPMC_AD14/ SYSBOOT14	IO	3.3V	General Purpose Memory Controller Interface Address/Data
A18	X_GPMC_AD15/ SYSBOOT15	IO	3.3V	General Purpose Memory Controller Interface Address/Data
A19	GND	-	-	Ground 0 V
A20	X_GPMC_ADVN_ALE	OUT	3.3V	General Purpose Memory Controller Interface address valid / address latch enable
A21	X_GPMC_OEN_REN	OUT	3.3V	General Purpose Memory Controller output enable / read enable
A22	X_GPMC_WAIT0	IO	3.3V	General Purpose Memory Controller WAIT
A23	X_GPMC_WEN	OUT	3.3V	General Purpose Memory Controller write enable
A24	GND	-	-	Ground 0 V
A25	X_RGMII1_TXD3	OUT	3.3V	Ethernet 1 RGMII Transmit data
A26	X_RGMII1_TXD2	OUT	3.3V	Ethernet 1 RGMII Transmit data
A27	X_RGMII1_TXD1	OUT	3.3V	Ethernet 1 RGMII Transmit data
A28	X_RGMII1_TXD0	OUT	3.3V	Ethernet 1 RGMII Transmit data
A29	GND	-	-	Ground 0 V
A30	X_RGMII1_RXD1	IN	3.3V	Ethernet 1 RGMII Receive data
A31	X_RGMII1_RXD0	IN	3.3V	Ethernet 1 RGMII Receive data
A32	X_KBD_ROW2	IN	3.3V	Keypad row

X1, Column A				
Pin #	**Signal**	**Type**	**Level**	**Description**
A33	X_KBD_ROW3	IN	3.3V	Keypad row
A34	GND	-	-	Ground 0 V
A35	X_KBD_COL2	OUT	3.3V	Keypad column
A36	X_KBD_COL3	OUT	3.3V	Keypad column
A37	X_I2C4_SCL	IO	3.3V	I²C bus 4 clock
A38	X_I2C4_SDA	IO	3.3V	I²C bus 4 data
A39	GND	-	-	Ground 0 V
A40	X_SPI3_CS0n	OUT	3.3V	SPI 3 chip select 0, (active low)
A41	X_SPI3_CLK	IO	3.3V	SPI3 Clock
A42	X_SPI3_DIN	IN	3.3V	SPI3 Data in
A43	X_SPI3_DO	OUT	3.3V	SPI3 Data out
A44	GND	-	-	Ground 0 V
A45	X_WAKEUP2	IN	3.3V	External wake-up signal
A46	X_GPIO4_3	IO	3.3V	AM57x GPIO4_3
A47	X_GPIO4_19	IO	3.3V	AM57x GPIO4_19
A48	X_XREF_CLK3	IN	3.3V	External Reference Clock 3. For Audio and other Peripherals.
A49	GND	-	-	Ground 0 V
A50	X_GPIO1_26	IO	3.3V	AM57x GPIO1_26
A51	X_GPIO1_27	IO	3.3V	AM57x GPIO1_27
A52	X_GPIO1_28	IO	3.3V	AM57x GPIO1_28
A53	X_GPIO1_29	IO	3.3V	AM57x GPIO1_29
A54	GND	-	-	Ground 0 V
A55	X_GPIO2_2	IO	3.3V	AM57x GPIO2_2
A56	X_GPIO7_5	IO	3.3V	AM57x GPIO7_5
A57	X_GPIO6_4	IO	3.3V	AM57x GPIO6_4
A58	X_GPIO8_2	IO	3.3V	AM57x GPIO8_2
A59	GND	-	-	Ground 0 V
A60	X_GPIO8_20	IO	3.3V	AM57x GPIO8_20
A61	X_GPIO8_21	IO	3.3V	AM57x GPIO8_21
A62	X_GPIO8_22	IO	3.3V	AM57x GPIO8_22
A63	X_GPIO8_23	IO	3.3V	AM57x GPIO8_23
A64	GND	-	-	Ground 0 V
A65	X_VIN3A_D4	IN	3.3V	Video Input 3 Port A Data input
A66	X_VIN3A_D5	IN	3.3V	Video Input 3 Port A Data input
A67	X_VIN3A_D6	IN	3.3V	Video Input 3 Port A Data input
A68	X_VIN3A_D7	IN	3.3V	Video Input 3 Port A Data input
A69	GND	-	-	Ground 0 V
A70	X_VIN3A_D12	IN	3.3V	Video Input 3 Port A Data input
A71	X_VIN3A_D13	IN	3.3V	Video Input 3 Port A Data input
A72	X_VIN3A_D14	IN	3.3V	Video Input 3 Port A Data input
A73	X_VIN3A_D15	IN	3.3V	Video Input 3 Port A Data input
A74	GND	-	-	Ground 0 V
A75	X_VIN3A_CLK0	IN	3.3V	Video Input 3 Port A Clock input
A76	X_XREF_CLK0	IN	3.3V	External Reference Clock 0. For Audio and other Peripherals.
A77	X_JTAG_TMS	IN	3.3V	JTAG Chain Test Mode Select signal
A78	X_JTAG_TRSTn	IN	3.3V	JTAG Chain Test Reset
A79	GND	-	-	Ground 0 V

X1, Column A				
Pin #	**Signal**	**Type**	**Level**	**Description**
A80	X_JTAG_RTCK	OUT	3.3V	JTAG Chain Return Test Clock signal

X1, Column B				
Pin #	**Signal**	**Type**	**Level**	**Description**
B1	X_DCAN2_TX	OUT	3.3V	DCAN Transmit Signal
B2	GND	-	-	Ground 0 V
B3	X_DCAN2_RX	IN	3.3V	DCAN Receive Signal
B4	X_QSPI1_SCLK	IO	3.3V	QSPI1 Serial Clock Output
B5	X_QSPI1_CS0			QSPI1 Chip Select [0]. This pin is Used for QSPI1 boot modes. (active low)
B6	X_QSPI1_CS1			QSPI1 Chip Select[1] (active low)
B7	GND	-	-	Ground 0 V
B8	X_GPMC_BEN0	OUT	3.3V	GPMC lower-byte enable active low
B9	X_GPMC_BEN1	OUT	3.3V	GPMC upper-byte enable active low
B10	X_GPMC_CLK	IO	3.3V	GPMC Clock output
B11	X_GPMC_CS0	OUT	3.3V	GPMC Chip Select 0 (active low)
B12	GND	-	-	Ground 0 V
B13	X_GPMC_AD0/ SYSBOOT0	IO	3.3V	General Purpose Memory Controller Interface Address/Data
B14	X_GPMC_AD1/ SYSBOOT1	IO	3.3V	General Purpose Memory Controller Interface Address/Data
B15	X_GPMC_AD2/ SYSBOOT2	IO	3.3V	General Purpose Memory Controller Interface Address/Data
B16	X_GPMC_AD3/ SYSBOOT3	IO	3.3V	General Purpose Memory Controller Interface Address/Data
B17	GND	-	-	Ground 0 V
B18	X_GPMC_AD8/ SYSBOOT8	IO	3.3V	General Purpose Memory Controller Interface Address/Data
B19	X_GPMC_AD9/ SYSBOOT9	IO	3.3V	General Purpose Memory Controller Interface Address/Data
B20	X_GPMC_AD10/ SYSBOOT10	IO	3.3V	General Purpose Memory Controller Interface Address/Data
B21	X_GPMC_AD11/ SYSBOOT11	IO	3.3V	General Purpose Memory Controller Interface Address/Data
B22	GND	-	-	Ground 0 V
B23	X_MDIO_D	IO	3.3V	Ethernet MDIO interface data
B24	X_MDIO_MCLK	OUT	3.3V	Ethernet MDIO interface clock
B25	X_RGMII1_TXC	OUT	3.3V	Ethernet 1 RGMII transmit clock
B26	X_RGMII1_TXCTL	OUT	3.3V	Ethernet 1 RGMII transmit control
B27	GND	-	-	Ground 0 V
B28	X_RGMII1_RXC	IN	3.3V	Ethernet 1 RGMII Receive clock
B29	X_RGMII1_RXCTL	IN	3.3V	Ethernet 1 RGMII Receive control
B30	X_RGMII1_RXD3	IN	3.3V	Ethernet 1 RGMII Receive data
B31	X_RGMII1_RXD2	IN	3.3V	Ethernet 1 RGMII Receive data
B32	GND	-	-	Ground 0 V
B33	X_KBD_ROW0	IN	3.3V	Keypad row

X1, Column B				
Pin #	**Signal**	**Type**	**Level**	**Description**
B34	X_KBD_ROW1	IN	3.3V	Keypad row
B35	X_KBD_COL0	OUT	3.3V	Keypad column
B36	X_KBD_COL1	OUT	3.3V	Keypad column
B37	GND	-	-	Ground 0 V
B38	X_I2C5_SDA	IO	3.3V	I²C bus 5 clock
B39	X_I2C5_SCL	IO	3.3V	I²C bus 5 data
B40	X_EHRPWM1B	OUT	3.3V	EHRPWM1 Output B
B41	X_SPI3_nCS1	IO	3.3V	SPI3 chip select 1, (active low)
B42	GND	-	-	Ground 0 V
B43	X_MCASP2_ACLKX	IO	3.3V	MCASP2 Transmit Bit Clock
B44	X_MCASP2_AXR2	IO	3.3V	MCASP3 Transmit/Receive Data
B45	X_MCASP2_AXR3	IO	3.3V	MCASP3 Transmit/Receive Data
B46	X_MCASP2_FSX	IO	3.3V	MCASP3 Transmit Frame Sync
B47	GND	-	-	Ground 0 V
B48	X_SPI2_nCS0	OUT	3.3V	SPI 2 chip select 0, (active low)
B49	X_SPI2_DIN	IN	3.3V	SPI3 Data in
B50	X_SPI2_DOUT	OUT	3.3V	SPI3 Data out
B51	X_SPI2_CLK	IO	3.3V	SPI3 Clock
B52	GND	-	-	Ground 0 V
B53	X_GPIO8_3	IO	3.3V	AM57x GPIO8_3
B54	X_GPIO8_4	IO	3.3V	AM57x GPIO8_4
B55	X_GPIO8_5	IO	3.3V	AM57x GPIO8_5
B56	X_GPIO8_6	IO	3.3V	AM57x GPIO8_6
B57	GND	-	-	Ground 0 V
B58	X_GPIO8_7	IO	3.3V	AM57x GPIO8_7
B59	X_GPIO4_20	IO	3.3V	AM57x GPIO4_20
B60	X_GPIO4_21	IO	3.3V	No Connect, **do not use in design**
B61	X_GPIO4_22	IO	3.3V	AM57x GPIO4_23, **known issue with signal and AM57x PAD naming mismatch**
B62	GND	-	-	Ground 0 V
B63	X_VIN3A_D0	IN	3.3V	Video Input 3 Port A Data input
B64	X_VIN3A_D1	IN	3.3V	Video Input 3 Port A Data input
B65	X_VIN3A_D2	IN	3.3V	Video Input 3 Port A Data input
B66	X_VIN3A_D3	IN	3.3V	Video Input 3 Port A Data input
B67	GND	-	-	Ground 0 V
B68	X_VIN3A_D8	IN	3.3V	Video Input 3 Port A Data input
B69	X_VIN3A_D9	IN	3.3V	Video Input 3 Port A Data input
B70	X_VIN3A_D10	IN	3.3V	Video Input 3 Port A Data input
B71	X_VIN3A_D11	IN	3.3V	Video Input 3 Port A Data input
B72	GND	-	-	Ground 0 V
B73	X_VIN3A_DE0	IN	3.3V	Video Input 3 Port A Data Enable input
B74	X_VIN3A_FLD0	IN	3.3V	Video Input 3 Port A Field ID input
B75	X_VIN3A_HSYNC0	IN	3.3V	Video Input 3 Port A Horizontal Sync input
B76	X_VIN3A_VSYNC0	IN	3.3V	Video Input 3 Port A Vertical Sync input
B77	GND	-	-	Ground 0 V
B78	X_JTAG_TCLK	IN	3.3V	JTAG test clock input
B79	X_JTAG_TDI	IN	3.3V	JTAG test data input

X1, Column B				
Pin #	**Signal**	**Type**	**Level**	**Description**
B80	X_JTAG_TDO	OUT	3.3V	JTAG test port data output

X2, Column A				
Pin #	**Signal**	**Type**	**Level**	**Description**
A1	VCC_3V3_IN	PWR	3.3V	3.3V power input
A2	VCC_3V3_IN	PWR	3.3V	3.3V power input
A3	VCC_3V3_IN	PWR	3.3V	3.3V power input
A4	VDD_SD	PWR	3.3V	3.3V SD card power output
A5	GND	-	-	Ground 0 V
A6	VBAT	PWR	3V-5V	Optional always-on power for the Real-Time Clock (RTC).
A7	X_UART3_RXD	IN	3.3V	UART3 Receive Data Input
A8	X_UART3_TXD	OUT	3.3V	UART3 Transmit Data Output
A9	X_nRESET_OUT	OUT	3.3V	Reset output (active low)
A10	GND	-	-	Ground 0 V
A11	X_MMC1_CLK	IO	3.3V	MMC1 clock
A12	X_MMC1_CMD	IO	3.3V	MMC1 command
A13	X_MMC1_CD	IN	3.3V	MMC1 Card Detect (active low)
A14	X_MMC1_WP	IN	3.3V	MMC1 Write Protect (active low)
A15	GND	-	-	Ground 0 V
A16	X_I2C1_SCL	IO	3.3V	I²C bus 1 clock
A17	X_I2C1_SDA	IO	3.3V	I²C bus 1 data
A18	X_USB1_DM	DIFF100	3.3V	USB 1 data minus
A19	X_USB1_DP	DIFF100	3.3V	USB 1 data plus
A20	GND	-	-	Ground 0 V
A21	X_USB_TXN0	DIFF100	3.3V	USB1 USB3.0 transmitter negative lane
A22	X_USB_TXP0	DIFF100	3.3V	USB1 USB3.0 transmitter positive lane
A23	GND	-	-	Ground 0 V
A24	X_USB_RXP0	DIFF100	3.3V	USB1 USB3.0 receiver negative lane
A25	X_USB_RXN0	DIFF100	3.3V	USB1 USB3.0 receiver positive lane
A26	GND	-	-	Ground 0 V
A27	X_USB2_DM	DIFF100	3.3V	USB 2 data minus
A28	X_USB2_DP	DIFF100	3.3V	USB 2 data plus
A29	X_USB2_DRVVBUS	OUT	3.3V	USB 2 VBUS control output
A30	X_USB1_DRVVBUS	OUT	3.3V	USB 1 VBUS control output
A31	X_I2C3_SDA	IO	3.3V	I²C bus 3 data
A32	X_I2C3_SCL	IO	3.3V	I²C bus 3 clock
A33	X_SPI1_nCS0	OUT	3.3V	SPI 1 chip select 0, (active low)
A34	X_SPI1_nCS1	OUT	3.3V	SPI 1 chip select 1, (active low)
A35	GND	-	-	Ground 0 V
A36	X_SPI1_DIN	IN	3.3V	SPI1 Data in
A37	X_SPI1_DOUT	OUT	3.3V	SPI1 Data out
A38	X_SPI1_CLK	IO	3.3V	SPI1 Clock
A39	X_PWRON	IN	3.3V	Push-button power control
A40	GND	-	-	Ground 0 V
A41	X_MCASP1_ACLKX	IO	3.3V	MCASP1 Transmit Bit Clock
A42	X_MCASP1_AXR14	IO	3.3V	MCASP1 Transmit/Receive Data

X2, Column A				
Pin #	**Signal**	**Type**	**Level**	**Description**
A43	X_MCASP1_AXR15	IO	3.3V	MCASP1 Transmit/Receive Data
A44	X_MCASP1_FSX	IO	3.3V	MCASP1 Transmit Frame Sync
A45	GND	-	-	Ground 0 V
A46	X_XREF_CLK1	IN	3.3V	External Reference Clock 1. For Audio and other Peripherals.
A47	X_XREF_CLK2	IN	3.3V	External Reference Clock 2. For Audio and other Peripherals.
A48	X_WAKEUP1	IN	3.3V	External wake-up signal
A49	X_GPIO4_23	IO	3.3V	AM57x GPIO4_22, **known issue with signal and AM57x PAD naming mismatch**
A50	GND	-	-	Ground 0 V
A51	X_ETH0_A+/TX0+	DIFF100	3.3V	Gigabit ETH data A plus or 10/100 transmit data plus
A52	X_ETH0_A-/TX0-	DIFF100	3.3V	Gigabit ETH data A minus or 10/100 transmit data minus
A53	X_ETH0_B+/RX0+	DIFF100	3.3V	Gigabit ETH data B plus or 10/100 receive data plus
A54	X_ETH0_B-/RX0-	DIFF100	3.3V	Gigabit ETH data B minus or 10/100 transmit data plus
A55	GND	-	-	Ground 0 V
A56	X_HDMI1_CLK+	DIFF100	3.3V	HDMI clock differential positive
A57	X_HDMI1_CLK-	DIFF100	3.3V	HDMI clock differential negative
A58	X_HDMI_D0+	DIFF100	3.3V	HDMI data 0 differential positive
A59	X_HDMI_D0-	DIFF100	3.3V	HDMI data 0 differential negative
A60	GND	-	-	Ground 0 V
A61	X_HDMI_D1+	DIFF100	3.3V	HDMI data 1 differential positive
A62	X_HDMI_D1-	DIFF100	3.3V	HDMI data 1 differential negative
A63	X_HDMI_D2+	DIFF100	3.3V	HDMI data 2 differential positive
A64	X_HDMI_D2-	DIFF100	3.3V	HDMI data 2 differential negative
A65	GND	-	-	Ground 0 V
A66	X_VOUT2_D4	OUT	3.3V	Video Output 2 Data
A67	X_VOUT2_D5	OUT	3.3V	Video Output 2 Data
A68	X_VOUT2_D6	OUT	3.3V	Video Output 2 Data
A69	X_VOUT2_D7	OUT	3.3V	Video Output 2 Data
A70	GND	-	-	Ground 0 V
A71	X_VOUT2_D12	OUT	3.3V	Video Output 2 Data
A72	X_VOUT2_D13	OUT	3.3V	Video Output 2 Data
A73	X_VOUT2_D14	OUT	3.3V	Video Output 2 Data
A74	X_VOUT2_D15	OUT	3.3V	Video Output 2 Data
A75	GND	-	-	Ground 0 V
A76	X_VOUT2_D20	OUT	3.3V	Video Output 2 Data
A77	X_VOUT2_D21	OUT	3.3V	Video Output 2 Data
A78	X_VOUT2_D22	OUT	3.3V	Video Output 2 Data
A79	X_VOUT2_D23	OUT	3.3V	Video Output 2 Data
A80	GND	-	-	Ground 0 V

X2, Column B				
Pin #	**Signal**	**Type**	**Level**	**Description**
B1	VCC_3V3_IN	PWR	3.3V	3.3V power input
B2	VCC_3V3_IN	PWR	3.3V	3.3V power input

X2, Column B				
Pin #	**Signal**	**Type**	**Level**	**Description**
B3	VCC_3V3_IN	PWR	3.3V	3.3V power input
B4	X_USB2_VBUS	USB	5.0V	USB2 bus voltage
B5	GND			
B6	VCC_5V0_IN	PWR	5.0V	5.0V power input
B7	X_UART5_RXD	IN	3.3V	UART5 Receive Data Input
B8	X_UART5_TXD	OUT	3.3V	UART5 Transmit Data Output
B9	X_nRESET_IN	IN	3.3V	Reset input (active low)
B10	X_EXT_PWR_ON	OUT	3.3V	Power good signal from PMIC (active low)
B11	GND	-	-	Ground 0 V
B12	X_MMC1_DAT0	IO	3.3V	MMC1 data
B13	X_MMC1_DAT1	IO	3.3V	MMC1 data
B14	X_MMC1_DAT2	IO	3.3V	MMC1 data
B15	X_MMC1_DAT3	IO	3.3V	MMC1 data
B16	GND	-	-	Ground 0 V
B17	X_SATA_RX-	DIFF100	3.3V	SATA differential negative receiver lane 0
B18	X_SATA_RX+	DIFF100	3.3V	SATA differential positive receiver lane 0
B19	GND	-	-	Ground 0 V
B20	X_SATA_TX-	DIFF100	3.3V	SATA differential negative transmitter lane 0
B21	X_SATA_TX+	DIFF100	3.3V	SATA differential positive transmitter lane 0
B22	GND	-	-	Ground 0 V
B23	X_PCIE_RXN0	DIFF100	3.3V	PCIe differential negative receiver lane 0
B24	X_PCIE_RXP0	DIFF100	3.3V	PCIe differential positive receiver lane 0
B25	GND	-	-	Ground 0 V
B26	X_PCIE_TXN0	DIFF100	3.3V	PCIe differential negative transmitter lane 0
B27	X_PCIE_TXP0	DIFF100	3.3V	PCIe differential positive transmitter lane 0
B28	GND	-	-	Ground 0 V
B29	X_PCIE_TXN1	DIFF100	3.3V	PCIe differential negative transmitter lane 1
B30	X_PCIE_TXP1	DIFF100	3.3V	PCIe differential positive transmitter lane 1
B31	GND	-	-	Ground 0 V
B32	X_PCIE_RXN1	DIFF100	3.3V	PCIe differential negative receiver lane 1
B33	X_PCIE_RXP1	DIFF100	3.3V	PCIe differential positive receiver lane 1
B34	GND	-	-	Ground 0 V
B35	X_PCIE_REFCLKN	DIFF100	3.3V	PCIe differential negative reference clock
B36	X_PCIE_REFCLKP	DIFF100	3.3V	PCIe differential positive reference clock
B37	GND	-	-	Ground 0 V
B38	X_MMC3_CLK	IO	3.3V	MMC3 clock
B39	X_MMC3_CMD	IO	3.3V	MMC3 command
B40	X_MMC3_DAT0	IO	3.3V	MMC3data
B41	X_MMC3_DAT1	IO	3.3V	MMC3data
B42	X_MMC3_DAT2	IO	3.3V	MMC3data
B43	X_MMC3_DAT3	IO	3.3V	MMC3data
B44	X_MMC3_DAT4	IO	3.3V	MMC3data
B45	X_MMC3_DAT5	IO	3.3V	MMC3data
B46	X_MMC3_DAT6	IO	3.3V	MMC3data
B47	X_MMC3_DAT7	IO	3.3V	MMC3data
B48	GND	-	-	Ground 0 V
B49	X_ETH0_C+	DIFF100	3.3V	Gigabit differential ETH data C plus

X2, Column B				
Pin #	**Signal**	**Type**	**Level**	**Description**
B50	X_ETH0_C-	DIFF100	3.3V	Gigabit differential ETH data C minus
B51	X_ETH0_D+	DIFF100	3.3V	Gigabit differential ETH data D plus
B52	X_ETH0_D-	DIFF100	3.3V	Gigabit differential ETH data D minus
B53	GND	-	-	Ground 0 V
B54	X_ETH0_LED1	IO	3.3V	Ethernet configuration input and speed LED control output
B55	X_ETH0_LED2	IO	3.3V	Ethernet configuration input and speed LED control output
B56	X_EHRPWM1A	OUT	3.3V	EHRPWM1 Output A
B57	X_HDMI1_DDC_SDA	IO	3.3V	HDMI display data channel data
B58	X_HDMI1_DDC_SCL	IO	3.3V	HDMI display data channel clock
B59	X_HDMI1_HPD		3.3V	HDMI display hot plug detect
B60	X_HDMI1_CEC		3.3V	HDMI consumer electronic control
B61	GND	-	-	Ground 0 V
B62	X_VOUT2_D0	OUT	3.3V	Video Output 2 Data
B63	X_VOUT2_D1	OUT	3.3V	Video Output 2 Data
B64	X_VOUT2_D2	OUT	3.3V	Video Output 2 Data
B65	X_VOUT2_D3	OUT	3.3V	Video Output 2 Data
B66	GND	-	-	Ground 0 V
B67	X_VOUT2_D8	OUT	3.3V	Video Output 2 Data
B68	X_VOUT2_D9	OUT	3.3V	Video Output 2 Data
B69	X_VOUT2_D10	OUT	3.3V	Video Output 2 Data
B70	X_VOUT2_D11	OUT	3.3V	Video Output 2 Data
B71	GND	-	-	Ground 0 V
B72	X_VOUT2_D16	OUT	3.3V	Video Output 2 Data
B73	X_VOUT2_D17	OUT	3.3V	Video Output 2 Data
B74	X_VOUT2_D18	OUT	3.3V	Video Output 2 Data
B75	X_VOUT2_D19	OUT	3.3V	Video Output 2 Data
B76	GND	-	-	Ground 0 V
B77	X_VOUT2_DE	OUT	3.3V	Video Output 2 Data Enable output
B78	X_VOUT2_CLK	OUT	3.3V	Video Output 2 Clock output
B79	X_VOUT2_HSYNC	OUT	3.3V	Video Output 2 Horizontal Sync output
B80	X_VOUT2_VSYNC	OUT	3.3V	Video Output 2 Vertical Sync output

3 Power

Basic operation of the phyCORE-AM57x requires a +5.0V input voltage supply with a minimum 70mA current capacity, and a +3.3V input voltage supply with minimum 2500mA current capacity. 5V power is supplied to the VCC_5V0_IN domain through connector pin X2-B6, while 3.3V power is supplied to the VCC_3V3_IN domain through connector pins X2-A1,A2,A3,B1,B2,B3.

CAUTION:
As a general design rule, we recommend connecting all 5V and 3.3V input pins to your power supply and at least a matching number of ground (GND) pins. For the best EMI performance, it is recommended to connect ALL ground pins at the phyCORE-Connector (X1, X2) to a solid ground plane. At the very least a matching number of ground pins to power pins should be made, in addition to using the ground pins surrounding signals used in application circuitry. Please refer to Table 3 for the locations of all ground pins on the phyCORE-Connector.

For systems that do not require the RTC, the VBAT input is not required and can be left floating.

Power on is controlled through the X_PWRON signal at connector X2-A39. Access to this signal is provided through a button on the Carrier Board. See chapter 16 for details on button usage.

The following sections of this chapter describe the power design of the phyCORE-AM57x.

3.1 5.0V System Power (VCC_5V0_IN)

The phyCORE-AM57x operates from a voltage supply with a nominal value of +5.0V. On-board drop out regulators generate the 3.3V voltage supplies required by the AM57x processor and on-board components from the 5.0 V supplied to the SOM.

For proper operation, the phyCORE-AM57x must be supplied with a voltage source of +5.0V ±5% with at least 70mA current capacity at the VCC_5V0_IN pins on the phyCORE connector X2. The VCC_5V0_IN pin can be found at connector X2-B6.

Connect all 5V input pins to your power supply and at least the matching number of GND pins.

3.2 3.3V System Power (VCC_3V3_IN)

The phyCORE-AM57x requires a voltage supply with a nominal value of +3.3V. The PMIC and On-board switching regulators generate the 1.09V, 1.35V, 1.06V, 1.03V, 1.8V, 1.2V, 1.05V voltage supplies required by the AM57x processor and on-board components from the 3.3V supplied to the SOM.

For proper operation, the phyCORE-AM57x must be supplied with a voltage source of +3.3V ±5% with at least 2500mA current capacity at the VCC_3V3_IN pins on the phyCORE connector X2. The VCC_3V3_IN pins can be found at connector X2-A1, A2, A3, B1, B2, B3.

Connect all 3.3V input pins to your power supply and at least the matching number of GND pins.

3.3 3.3V SD Power (VDD_SD)

The phyCORE-AM57x SOM provides the VDD_SD voltage supply with a nominal value of 3.3V and a maximum current draw of 300mA. The PMIC generates the VDD_SD to provide the power rail for an SD card on the Carrier Board. The VDD_SD pin can be found at connector X2-A4.

3.4 Off-chip RTC Power (VBAT)

The SOM provides a VBAT input for applications requiring an ultra-low power RTC that retains time when VCC_3V3_IN and VCC_5V0_IN are removed. Connect a 3.0V battery or other supply to the VBAT input at pin X2-A6. VBAT voltage should not exceed the VCC_3V3_IN supply. The RTC will continue to maintain its time down to approximately 1.0V on the VBAT pin.

For applications not requiring RTC backup, VBAT can be left floating.

3.5 Power Management IC (U3)

The phyCORE-AM57x provides an on-board Power Management IC (PMIC), Texas Instruments TPS659037, at position U3 to generate the voltages required by the processor and on-board components.

Figure 5 presents a graphical depiction of the SOM powering scheme.

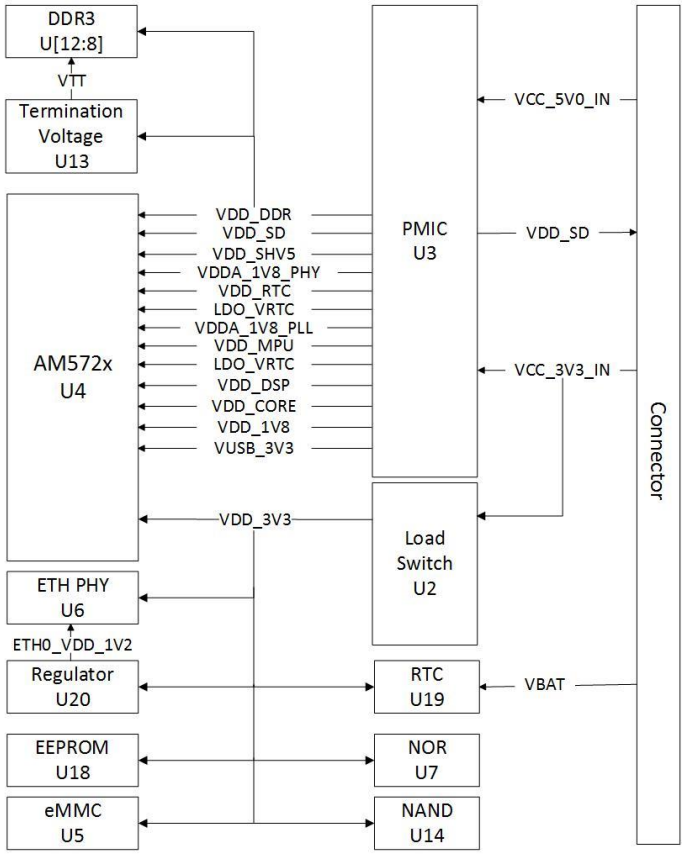

Figure 5. Power Supply Diagram

3.5.1 Power Domains

The SOM has three input voltage rails and one output rail. Two input rails, VCC_5V0_IN and VCC_3V3_IN, provide input power to the PMIC. The PMIC generates all its output voltages from these two input rails, including the VDD_SD output rail that is made available for external use (see Figure 5). A load switch is used to generate the VDD_3V3 rail from the VCC_3V3_IN rail. This load switch is controlled by the PMIC to ensure proper power sequencing for all on-board supplies. The third input rail, VBAT, provides power for an off-chip RTC on the SOM (see Chapter 4.2 for more details).

The following tables summarize the relationships between the voltage rails and the devices on the phyCORE-AM57x.

Table 4. External Supply Voltages

Signal	Description	Direction	Function
VCC_5V0_IN	5.0V system power supply	IN	Power up PMIC U3
VCC_3V3_IN	3.3V system power supply	IN	Power for PMIC U3 and Load switch U2
VBAT	3.0V RTC battery supply	IN	Backup power for RTC U19
VDD_SD	3.3V SD Card power supply	OUT	Power rail for SD card on Carrier Board

Table 5. Internal Voltage Rails

Device	Device Output	Schematic Signal	Voltage	Function
PMIC U3	LDOUSB_OUT	VUSB_3V3	3.3	AM57x USB analog supply
	LDOVRTC_OUT	LDO_VRTC	1.8	AM57x RTC bias and RTC LFOSC analog supply
	LDO1_OUT	VDD_SD	3.3	AM57x MMC1 supply, phyCORE Connector for SD
	LDO2_OUT	VDD_SHV5	3.3	AM57x RTC Power group supply
	LDO3_OUT	VDDA_1V8_PHY	1.8	AM57x PLL and PHY analog supply
	LDO9_OUT	VDD_RTC	1.05	AM57x RTC Domain supply
	LDOLN_OUT	VDDA_1V8_PLL	1.8	AM57x DPLL_IVA analog supply
	SMPS1	VDD_MPU	1.09	AM57x MPU Supply
	SMPS2			
	SMPS3	VDD_DDR	1.35	AM57x DDR Supply
	SMPS4	VDD_DSP	1.06	AM57x DSP-EVE domain supply
	SMPS5			
	SMPS6	VDD_CORE	1.03	AM57x Core voltage supply
	SMPS8	VDD_1V8	1.8	AM57x power supply
	SMPS9	ETH0_VDD_1V2	1.2	PHYTEC Reserved for future use
Load Switch U2	VOUT	VDD_3V3	3.3	Multiple component voltage supply
Regulator U20	SW	VDD_1V2	1.2	KSZ9031 Ethernet PHY supply
Termination U13	VO	VTT	1.35	DDR3 termination voltage supply

4 Real-Time Clock (RTC)

There are two options for an RTC on the phyCORE-AM57x: the on-chip RTC and an external on-board RTC. The following chapters detail these two RTC options.

4.1 AM57x RTC

The AM57x processor includes an integrated RTC. However, the RTC integrated in the AM57x uses significantly more power than the external RTC on the SOM. Because of this power disadvantage, the SOM has not been designed to support the AM57x RTC with backup power.

4.2 External RTC

The SOM also provides an ordering option to populate an additional, external RTC at U19 which is connected to the I2C1 bus at address 0x68. This external RTC uses less power than the RTC integrated in AM57x, and it could be used when very-low battery power is important. The external RTC typically uses 350nA at 3V. In order for the external RTC to maintain time when main system power is removed, the VBAT input must be supplied with power. See Chapter 3.4 for more details on supplying the VBAT power domain.

4.2.1 Power-On Wake

The external RTC's interrupt output is connected to the processors WAKEUP3 input, allowing the RTC to wake the processor at a preset time. This can be useful as a method of resuming normal processor operation at a specified time when a low power sleep state is implemented to save system power.

5 System Configuration and Booting

Although most features of the AM57x microcontroller are configured or programmed during the initialization routine, other features which impact program execution must be configured prior to initialization via pin termination. During the power-on reset cycle the operational system boot mode of the AM57x processor is determined by the configuration of the SYSBOOT [15:0] pins. These signals are named X_GPMC_ADxx/SYSBOOTxx at the phyCORE connector. The pull-up and pull-down resistors populated on the SOM set the default sysboot [15:0] configuration to 0b1000000100100010.

For development and debugging purposes, the sysboot pins are all available at the phyCORE connector. However, PHYTEC can provide the SOM with any specific boot setup for final production.

Table 6 describes the function of the SYSBOOT signals.

Table 6. Sysboot Signal Description

Signal	Description
sysboot[15]	Must be pulled up for proper device operation.
sysboot[14]	Must be pulled down for proper device operation.
sysboot[13:10]	Configure the GPMC interface when booting from XIP/NAND memory on GPMC (Table 7)
sysboot[9]	Must be pulled down for proper device operation.
sysboot[8]	Must be pulled up for proper device operation.
sysboot[7:6]	Sector offset for the location of the redundant SBL images in QSPI. (Table 8)
sysboot[5:0]	Select interfaces or devices. (Table 9)

The SYSBOOT signals are latched and sampled after nPORZ. These signals can be used for other purposes after boot. To modify the default SYSBOOT configuration, use 1k pull-up, or pull-down resistors on your Carrier Board to override the SOM settings. When adding a pull-up, ensure the signal is pulled up to the 3.3V power rail enabled by the X_EXT_PWR_ON signal. In general, only the SYSBOOT [5:0] pins need to be modified to adjust the desired boot mode.

For more information about pad multiplexing configuration please refer to TI AM57x Technical Reference Manual.

5.1 GPMC Configuration for XIP/NAND

Table 7 describes the GPMC configuration controlled by SYSBOOT [13:10] for booting from NAND or XIP.

Table 7. GPMC for XIP/NAND Configuration

Signal	Function	Value	Configuration
SYSBOOT[13]	Bus Width	0b0	8-bit
		0b1	16-bit
SYSBOOT[12:11]	A/D-muxed/non-muxed Device on CS0	0b00	Non-muxed device
		0b01	A/D-muxed device
SYSBOOT[10]	Wait-pin Monitoring for Read Accesses	0b0	Disabled

5.2 QSPI Redundant SBL Images Offset

Table 8 describes the four available options to set the offset for redundant SBL images. Only the primary image will be used if not using the redundant SBL feature, therefore no change in SYSBOOT will be required.

Table 8. Redundant SBL Image Offset

SYSBOOT[7:6]	Offset
0b00	64 KiB
0b01	128KiB
0b10	256 KiB
0b11	512 KiB

5.3 Boot Device Order

Table 9 shows the different boot device orders, which can be selected by configuring the five boot-order configuration pins, X_GPMC_AD/SYSBOOT [5:0] of the phyCORE-AM57x. Please note that only a subset of possible configurations are listed in the tables. For a complete list of the AM57x boot modes please refer to the Texas Instruments AM57x Technical Reference Manual.

Table 9. Boot Device Order[1]

SYSBOOT[5:0]	First Device	Second Device	Third Device
0b000000	USB	eMMC	
0b000001	USB	NAND	
0b000010	USB	SD	eMMC
0b000011	USB	SATA	SD
0b000100	USB		XIP
0b000101	SD	XIP	
0b000110	SD	QSPI_1	
0b000111	SD	QSPI_4	
0b001010	SD	Fast XIP	
0b010000	USB		
0b0101XX	SD	USB	
0b0110XX	SD	USB	
0b100000	eMMC	USB	
0b100001	NAND	USB	
0b100010	**SD**	**eMMC**	**USB**
0b100011	SATA	SD	USB
0b100100	XIP	USB	
0b100101	XIP	SD	USB
0b100110	QSPI_1	SD	USB
0b100111	QSPI_4	SD	USB
0b110000	SD		
0b110100	SATA		
0b110101	XIP		
0b110110	QSPI_1		

[1] Default boot mode is in **bold text**

0b110111	QSPI_4		
0b111000	eMMC		
0b111001	NAND		
0b111010	Fast XIP		
0b111011	eMMC(boot partition)		

5.4 Boot Peripheral Pin Multiplexing

Table 10 lists the pin multiplexing mode and associated signals on the SOM for each boot device found in Table 9.

Table 10. Pin Multiplexing According to Boot Peripheral

Boot Device	Boot Interface	Pads	MuxMode	SOM Signals
eMMC	MMC2	gpmc_a[22:19]	0x1	MMC2_DAT[7:4]
		gpmc_a[23]		MMC2_CLK
		gpmc_a[27:24]		MMC2_DAT[3:0]
		gpmc_cs[1]		MMC2_CMD
SD	MMC1	mmc1_clk	0x0	X_MMC1_CLK
		mmc1_cmd		X_MMC1_CMD
		mmc1_dat[3:0]		X_MMC1_DAT[3:0]
NAND	GPMC	GPMC on CS0	0x0	GPMC on CS0
XIP	GPMC	GPMC on CS0	0x0	GPMC on CS0, per wait signal setting SYSBOOT[10]
SATA	SATA	sata1_txp0	-	X_SATA_TX+
		sata1_txn0		X_SATA_TX-
		sata1_rxp0		X_SATA_RX+
		sata1_rxn0		X_SATA_RX-
QSPI_1/QSPI_4	QSPI_1	gpmc_a[18]	0x1	X_QSPI1_SCLK
		gpmc_a[17:14]		X_QSPI1_D[3:0]
		gpmc_a[13]		X_QSPI1_RTCLK
		gpmc_cs[2]		X_QSPI1_CS0
USB	USB1	usb1_dp	-	X_USB1_DP
		usb1_dm		X_USB1_DM

6 System Memory

The phyCORE-AM57x provides five types of on-board memory:

- DDR3 SDRAM
- eMMC or NAND FLASH
- SPI NOR FLASH
- I^2C EEPROM

NOTE:
The phyCORE-AM57x does not support the use of eMMC and NAND flash storage at the same time. Only one of the storage devices can be populated on the SOM at any given time. Additional NAND or eMMC devices need to be implemented on the Carrier Board.

These following sections of this chapter detail each memory type used on the phyCORE-AM57x.

6.1 DDR3 SDRAM (U8, U9, U10, U11, U12)

The RAM memory on the phyCORE-AM57x is comprised of two independent banks. One bank consists of two 16-bit wide DDR3 SDRAM chips for a 32-bit wide interface. The other bank consists of two 16-bit wide DDR3 SDRAM chips for a 32-bit wide interface, plus an additional 8-bit wide chip for Error Correction Code (ECC) support. The chips are connected to the dedicated DDR interface called the Extended Memory Interface (EMIF) of the AM57x processor.

Typically, the DDR3-SDRAM initialization is performed by a boot loader or operating system following a power-on reset and must not be changed at a later point by any application code. When writing custom code independent of an operating system or boot loader, SDRAM must be initialized through the appropriate SDRAM configuration registers on the AM57x controller. Refer to the AM57x Technical Reference Manual about accessing and configuring these registers.

The following sections details each DDR3 memory bank on the phyCORE-AM57x.

6.1.1 DDR3 Bank1 (U8, U9, U12)

DDR3 SDRAM Bank1 is connected to the EMIF1 controller. Bank 1 consists of two 16-bit wide chips at U8 and U9 (32-bit wide total) and an optional 8-bit wide ECC SDRAM at U12.

The EMIF1 CS0 address is 0x8000 0000 at reset, and CS0 uses a 1-GiB address space at reset.

6.1.1.1 DDR3 Bank1 ECC (U12)

Error Correction Code (ECC) RAM is a reliable solution for server design or other systems with high value data and low tolerance for data corruption. The ECC on the SDRAM data bus for EMIF1 consists of an 8-bit wide chip at U12. For more information about ECC on the EMIF1 please refer to the AM57x Technical Reference Manual.

6.1.2 DDR3 Bank2 (U10, U11)

DDR3 SDRAM Bank2 is connected to the EMIF2 controller. Bank 2 consists of two 16-bit wide chips at U10 and U11 (32-bit wide total).

For the EMIF2 CS0 address space please refer to the AM57x Technical Reference Manual.

6.2 eMMC Memory (U5)

The phyCORE-AM57x can be populated with an eMMC flash as an easy to program nonvolatile memory. The eMMC flash is connected to the MMC2 interface of the AM57x with a bus width of 8bits. Table 11 shows the MMC signals used for eMMC flash.

Table 11. eMMC Signal Connections to Processor

AM57x pad	Signal	Mux	Type	Description
GPMC_A[27:24]	MMC2_DAT[3:0]	0x1	IO	MMC2 data bit[3:0]
GPMC_A[23]	MMC2_CLK	0x1	IO	MMC2 clock
GPMC_A[22:20]	MMC2_DAT[7:4]	0x1	IO	MMC2 data bit[7:4]

NOTE:
The phyCORE-AM57x does not support the use of eMMC and NAND flash storage at the same time. Only one of the storage devices can be populated on the SOM at any given time. Additional NAND or eMMC devices need to be implemented on the Carrier Board.

6.3 NAND Flash Memory (U14)

The phyCORE-AM57x can be populated with an NAND flash as an easy to program nonvolatile memory. The NAND flash is connected to the GPMC interface of the AM57x with a bus width of 8-bit or 16-bit depending on the NAND device on CS0, CS1, CS2, and CS3. Table 12 shows the GPMC signals used for NAND flash.

Table 12. NAND Flash Signal Connections to Processor

AM57x pad	Signal	Connector Pin	Mux	Type	Description
GPMC_AD0	X_GPMC_AD0	X1-B13	0x0	IO	Address / Data 0
GPMC_AD1	X_GPMC_AD1	X1-B14	0x0	IO	Address / Data 1
GPMC_AD2	X_GPMC_AD2	X1-B15	0x0	IO	Address / Data 2
GPMC_AD3	X_GPMC_AD3	X1-B16	0x0	IO	Address / Data 3
GPMC_AD4	X_GPMC_AD4	X1-A10	0x0	IO	Address / Data 4
GPMC_AD5	X_GPMC_AD5	X1-A11	0x0	IO	Address / Data 5
GPMC_AD6	X_GPMC_AD6	X1-A12	0x0	IO	Address / Data 6
GPMC_AD7	X_GPMC_AD7	X1-A13	0x0	IO	Address / Data 7
GPMC_AD8	X_GPMC_AD8	X1-B18	0x0	IO	Address / Data 8
GPMC_AD9	X_GPMC_AD9	X1-B19	0x0	IO	Address / Data 9
GPMC_AD10	X_GPMC_AD10	X1-B20	0x0	IO	Address / Data 10
GPMC_AD11	X_GPMC_AD11	X1-B21	0x0	IO	Address / Data 11
GPMC_AD12	X_GPMC_AD12	X1-A15	0x0	IO	Address / Data 12
GPMC_AD13	X_GPMC_AD13	X1-A16	0x0	IO	Address / Data 13
GPMC_AD14	X_GPMC_AD14	X1-A17	0x0	IO	Address / Data 14
GPMC_AD15	X_GPMC_AD15	X1-A18	0x0	IO	Address / Data 15
GPMC_CS0	X_GPMC_CS0	X1-B11	0x0	O	Chip select 0
GPMC_CS1	MMC2_CMD	Not Available	0x0	O	Chip select 1
GPMC_CS2	X_GPMC_CS2	Not Available	0x0	O	Chip select 2
GPMC_CS3	X_GPMC_CS3	Not Available	0x0	O	Chip select 3
GPMC_ADVN_ALE	X_GPMC_ADVN_ALE	X1-A20	0x0	O	GPMC address valid active low or address latch enable

AM57x pad	Signal	Connector Pin	Mux	Type	Description
GPMC_OEN_REN	X_GPMC_OEN_REN	X1-A21	0x0	O	GPMC output enable active low or read enable
GPMC_WAIT0	X_GPMC_WAIT0	X1-A22	0x0	I	GPMC external indication of wait 0
GPMC_BEN0	X_GPMC_BEN0	X1-B8	0x0	O	GPMC lower-byte enable active low
GPMC_WEN	X_GPMC_WEN	X1-A23	0x0	O	GPMC write enable active low
VIN2A_D1	GPIO4_2	Not Available	0x14	O	Write protect

NOTE:
The phyCORE-AM57x does not support the use of eMMC and NAND flash storage at the same time. Only one of the storage devices can be populated on the SOM at any given time. Additional NAND or eMMC devices need to be implemented on the Carrier Board.

6.4 I²C EEPROM (U18)

The phyCORE-AM57x can be populated with a nonvolatile 4KB EEPROM with an I²C interface as an ordering option. This memory can be used to store configuration data or other general purpose data. This device is accessed through I²C port 1 on the AM57x at address 0x50.

6.5 QSPI NOR Flash Memory (U7)

The phyCORE-AM57x can be populated with a SPI Flash memory device as an ordering option. This would be suitable for applications which require a small code footprint or small RTOS.

Using a SPI Flash can eliminate the need to install NAND Flash or eMMC memory on the SOM. This could reduce BOM costs, free up the NAND signals for other devices on the AM57x GPMC interface, and remove the need for doing the bad block management that is required when using NAND Flash.

6.6 Memory Model

There is no special address decoding device on the phyCORE-AM57x, which means that the memory model is given according to the memory mapping of the AM57x. Please refer to the AM57x Technical Reference Manual for the memory map.

7 SD/MMC Card Interfaces

The phyCORE-AM57x includes two SD / MMC Card interfaces: MMC1 and MMC3. The MMC signals are directly routed from the processor to the phyCORE connector. Please note that the VDD_SD power signal on the phyCORE connector X2-A4 must be used as power the rail for an SD card connected to MMC1.

8 Serial Interfaces

The AM57x provides numerous serial interfaces. However, only a subset of the interfaces is brought out of the phyCORE connector as the phyCORE-AM57x default multiplexing configuration. The following sections describe the default interfaces on the phyCORE-AM57x. Additional interfaces can be accessed through alternate muxing configurations. Please refer to TI's technical reference manual for more information on pin muxing options.

Some of the serial interfaces are equipped with a transceiver to allow direct connection to external devices.

8.1 USB

The phyCORE-AM57x provides two USB interfaces with embedded USB PHYs. Generally, an external USB connector is all that is needed for USB functionality. USB power switch circuits add additional functionality to power externally connected devices.

Please note that the X_USB2_VBUS signal located on X2-B4 pin of the phyCORE connector must be connected to the VBUS rail of the USB connector for USB2 to function properly.

8.2 Ethernet

The phyCORE-AM57x can connect to a LAN via the AM57x embedded 10/100/1000 Ethernet switch. The Ethernet switch has two ports: Ethernet0 and Ethernet1.

8.2.1 Ethernet0

The phyCORE-AM57x can be populated with a 10/100/1000Base-T Ethernet transceiver PHY at U6. Table14 shows the location of the Ethernet0 pins on the connector. See Table 3 for the locations of the Ethernet0 signals on the phyCORE-Connector. All Ethernet0 signals are labeled as X_ETH0… on the connector.

The KSZ9031 transceiver supports HP Auto MDIX technology, eliminating the need for the consideration of a direct connect LAN cable, or a cross over patch cable.

Special routing, layout, and other circuit design considerations should be followed by referencing the phyCORE-AM57x Carrier Board schematics along with the phyCORE-AM57x Design In Guide.

CAUTION:
Please see the KSZ9031 Ethernet Controller datasheet when designing the Ethernet transformer circuitry.

8.2.2 Ethernet1

The AM57x Ethernet1 interface signals can connect to any industry standard Ethernet transceiver or configured for other multiplex functionality. The AM57x supports MII, RMII, and RGMII modes on the interface. GMII is not supported by the processor.

It is strongly recommended to place the Ethernet PHY on the Carrier Board close to the pins of the SOMs Ethernet interface pins to achieve a trace length of less than 100mm. To match the timing requirement for the MII, RMII, RGMII interfaces a 0.5ns delay is implemented in the trace length of the X_RGMII1_RXC signal. Please refer to the datasheet of the chosen Ethernet transceiver for more information for signal timings. Additional routing, layout, and other circuit design considerations should be followed by referencing the phyCORE-AM57x Carrier Board schematics along with the phyCORE-AM57x Design In Guide.

For signal integrity purposes, source termination resistors are placed on the output signals of the Ethernet interface.

8.3 I²C

The phyCORE-AM57x provides five independent I²C buses at the phyCORE connector directly from the processor. I2C1, I2C2, I2C3, I2C4, and I2C5. The I2C1 bus is pulled up to the 3.3V rail via 2.2KOhm resistors and connects to the PMIC (U3), EEPROM (U18), and RTC (U19). I2C2-5 require external pull-up resistors on custom Carrier Board designs. The following table shows the reserved addresses for the internal components of the phyCORE-AM57x.

Table 13. I2C1 Reserved Addresses

Device	Address
RTC	0x68
EEPROM	0x50
PMIC	0x58
	0x59
	0x5A
	0x5B

8.4 SATA

The phyCORE-AM57x provides one SATA interface with maximum data rate of 3Gbps. All of the SATA signals are AC coupled through series 10nF capacitors. Please refer to Table 3 for the location of the SATA signals on the phyCORE connector.

8.5 PCIe

The phyCORE-AM57x supports the embedded PCIe module on the AM57x.The PCIe interface on the phyCORE-AM57x provides up to 5 Gbps data rate. All transmit and reference clock signals on the PCIe interface are AC coupled via 100nF capacitors. Please refer to Table 3 for the location of the PCIe signals on the phyCORE connector.

9 Debug Interface

The phyCORE-AM57x is equipped with a JTAG interface for downloading program code into the internal RAM controller or for debugging programs currently executing.

Please note that the X_JTAG_nTRST signal is pulled down to the ground via a 4.7Kohm resistor. In addition, 22 Ohm series termination resistors are installed on the X_JTAG_TDO and X_JTAG_RTCK signals for signal integrity purposes.

10 Technical Specifications

The physical dimensions of the phyCORE-AM57x are represented in Figure 6. The module's profile is approximately 7.6mm thick. The maximum component height (excluding connectors X1 and X2) is approximately 3.5mm on the bottom (connector) side of the PCB and approximately 2.6mm on the top (microcontroller) side. The PCB is approximately 1.4mm thick. The distance from the surface of the Carrier Board to the highest component on the top side of the board is approximately 9.75mm.

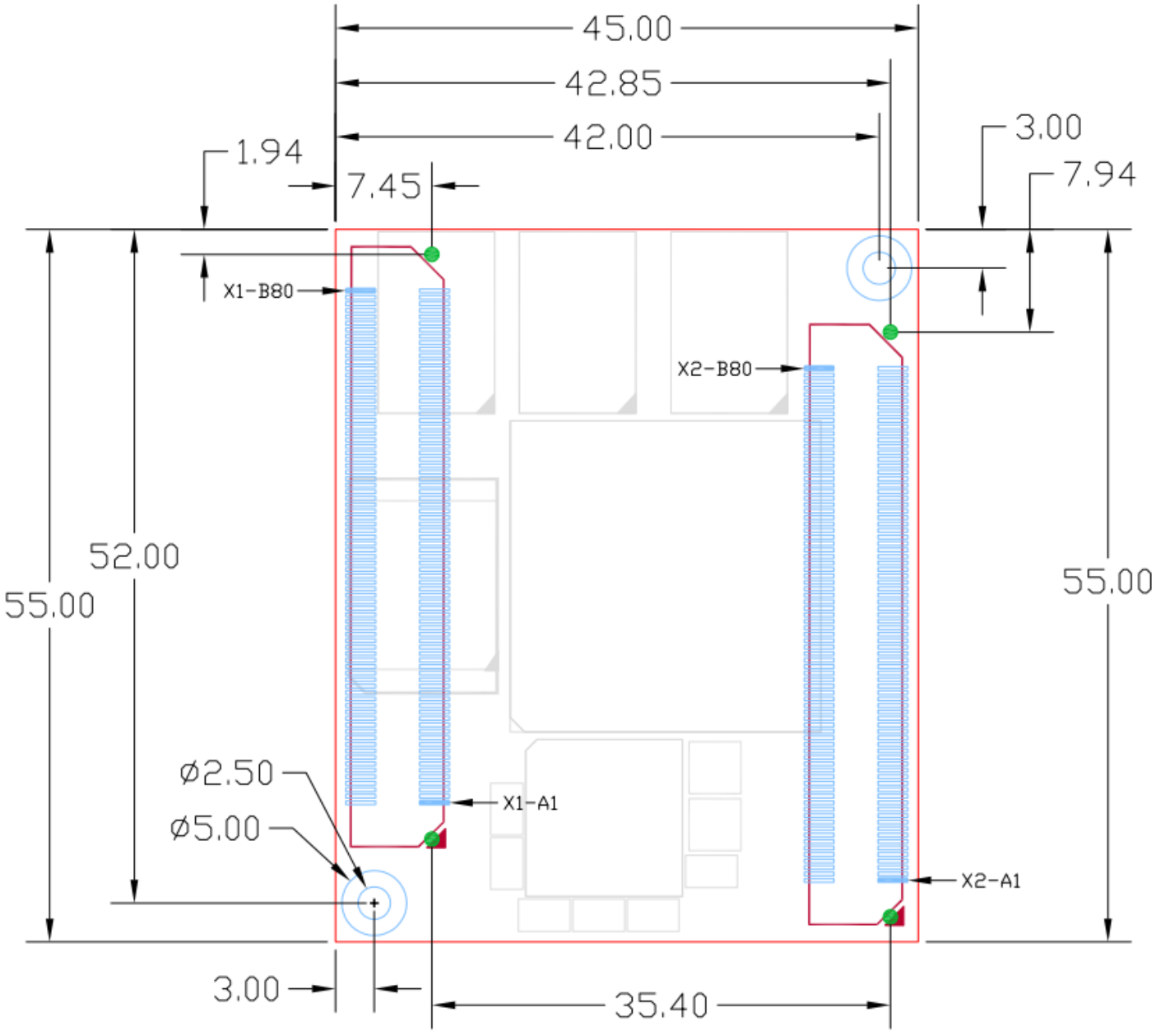

Figure 6. phyCORE-AM57x Mechanical Dimensions (top down view as seen from controller side)

Table 14. Technical Specifications

Dimensions:	45 x 55mm
Weight (approximate):	20.9g
Storage Temperature:	-40C to +90C
Operating Temperature:	-40C to +85C
Humidity:	95 % r.F. not condensed
Power Consumption:	VCC 3V3 Linux idle: Typical 3.00 +/- 0.15W iperf: Typical 3.37W +/- 0.15W memtester: Typical 6.94W +/- 0.17W Full load + Video demo: 7.26W VCC 5V0 Linux idle: Typical 30mW Full load + Video demo: 300mW Conditions: 2GB DDR3L_SDRAM, 4GB eMMC, EEPROM, SD card, SATA, USB1, USB2

Table 15. Operating Characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
VCC_3V3_IN	3.3V SOM input voltage		3.14	3.3	3.46	VDC
VCC_5V0_IN	5.0V SOM input voltage		4.75	5	5.25	VDC
VDD_SD	3.3V SD card output voltage		3.14	3.3	3.46	VDC
VBAT	Battery backup for RTC		1	3	4.4	VDC
$I_{VCC\_3V3\_IN}$	3.3V SOM operating current	Stress test	2090	2200	2310	mA
		Iperf test	929	1035	1093	mA
		memtester	2097	2165	2256	mA
		Linux idle	830	919	988	mA
$I_{VCC\_5V0\_IN}$	5.0V SOM operating current	Stress test	55	60	65	mA
I_{VBAT}	Battery backup operating current	Time keeping		350	500	nA

11 Hints for Integrating and Handling the phyCORE-AM57x

11.1 Integrating the phyCORE-AM57x

Successful integration of the phyCORE-AM57x SOM into target circuitry greatly depends on adherence to the layout design rules for the GND connections of the phyCORE module. As a general design rule, we recommend connecting all GND pins neighboring signals which are being used in application circuitry. At least one ground pin should be connected for every power pin used. For maximum EMI performance, all GND pins should be connected to a solid ground plane.

Additional information is available to facilitate the integration of the phyCORE-AM57x into customer applications, such as:

- phyCORE-AM57x Design In Guide [TBD]
- phyCORE-AM57x Carrier Board schematic reference. Schematics are made available upon request.
- Phone, e-mail, FAQ, wiki, and other online support by visiting http://phytec.com/contact/

11.2 Handling the phyCORE-AM57x

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

WARNING:
If any modifications to the module are performed, regardless of their nature, the manufacturer guarantee is voided.

Part II: PCM-948/phyCORE-AM57x Carrier Board

Part II of this manual provides detailed information regarding the phyCORE-AM57x Carrier Board and its usage with the phyCORE-AM57x SOM.

All board images and the information presented in the following sections are applicable to the 1435.2 PCB revision of the phyCORE-AM57x Carrier Board.

The phyCORE-AM57x Carrier Board also serves as a reference design for development of custom target hardware that integrates with the phyCORE-AM57x System on Module. The Carrier Board schematics and Bill of Materials are available under a Non-Disclosure Agreement (NDA). Re-use of Carrier Board circuitry likewise enables users of PHYTEC SOMs to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks.

12 Introduction

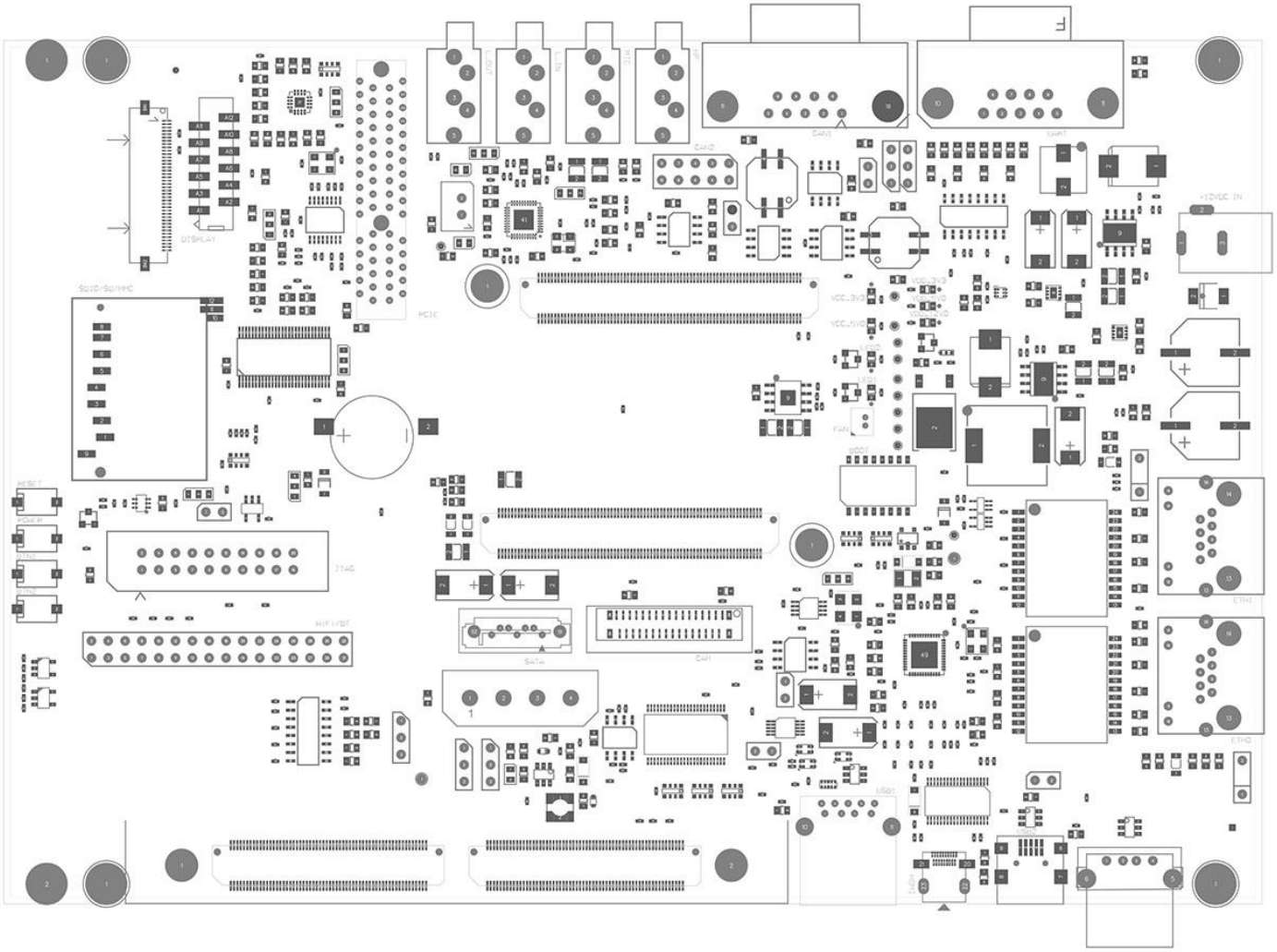

Figure 7. phyCORE-AM57x Carrier Board

PHYTEC Carrier Boards are fully equipped with all mechanical and electrical components necessary for quick start-up, communication, and programming of the applicable PHYTEC System on Module (SOM). Carrier Boards are designed for evaluation, testing, and prototyping of PHYTEC SOMs in laboratory environments prior to their implementation in customer designed applications.

The phyCORE-AM57x Carrier Board provides a flexible development platform that enables a quick and simple start-up of the phyCORE-AM57x System on Module. The Carrier Board design allows for the connection of additional expansion boards that support convenient prototyping and software evaluation.

13 Overview of Peripherals

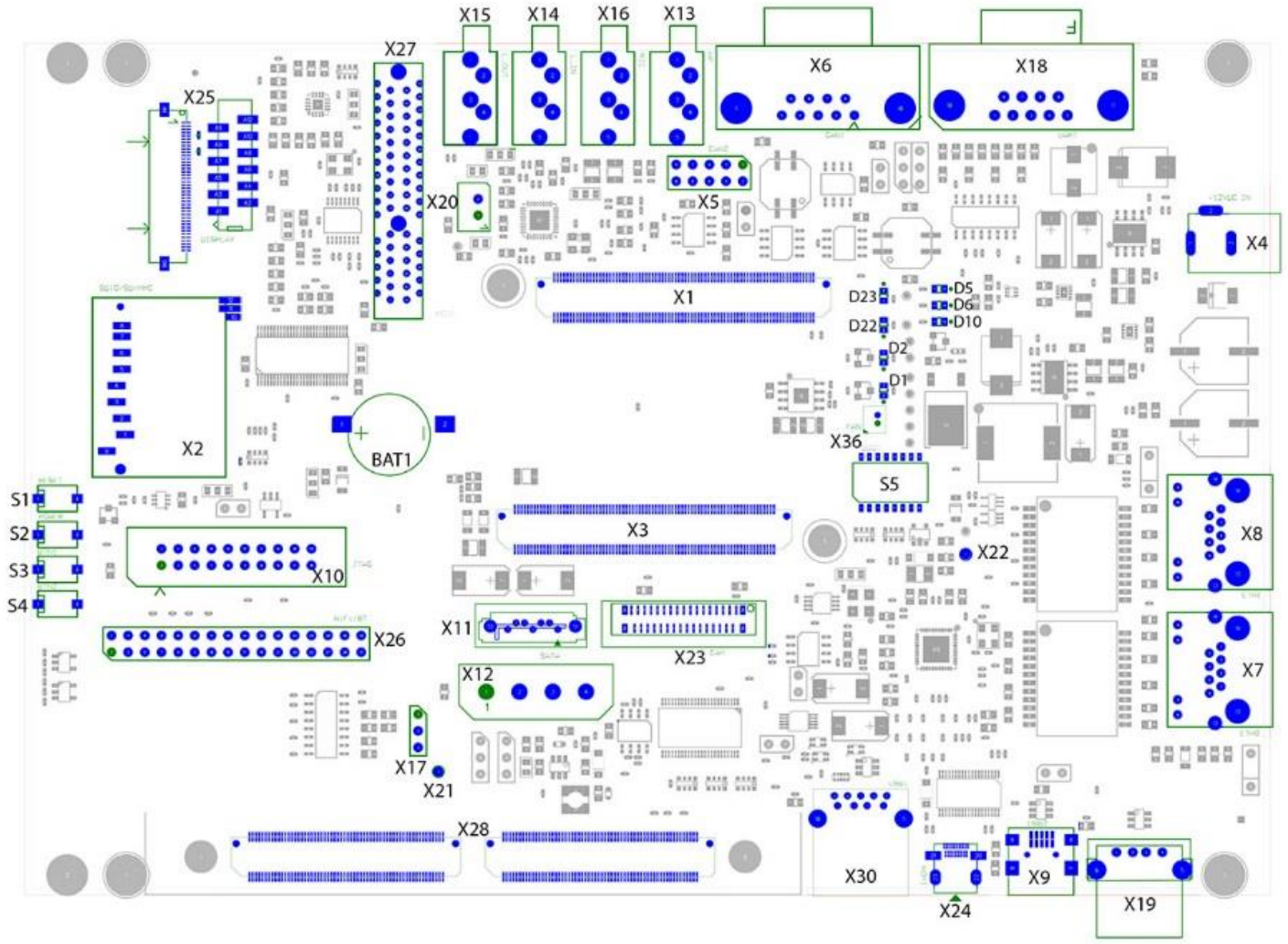

Figure 8. Overview of Peripherals

The phyCORE-AM57x Carrier Board is depicted in Figure 8 and includes the following components and peripherals listed in Table 16, Table 17, and Table 18. For a detailed description of each peripheral, refer to the appropriate chapter listed in the respective table.

13.1 Connectors and Headers

Table 16. Connectors and Headers

Ref. Des.	Description	Chapter
X1, X3	phyCORE-AM57x connectors to SOM	15
X2	SDIO/SD/MMC Connector	18
X4	Wall adapter input power jack to supply main board power	16
X5	CAN Connector (CAN2)	17
X6	CAN Connector (CAN1)	17

Ref. Des.	Description	Chapter
X7	Ethernet Connector (ETH0)	20
X8	Ethernet Connector (ETH1)	20
X9	USB Mini-AB OTG Connector (USB2)	21
X10	JTAG Connector	24
X11, X12	SATA Signal and Power Connectors	23
X13	Audio Headset Connector	29
X14	Audio Line In	29
X15	Audio Line Out	29
X16	Audio Mic In Connector	29
X17	UART5 RS-232 Connector	22
X18	UART3 RS-232 Connector	22
X19	USB-A High Speed Host Connector (USB2)	21
X20	Loudspeaker Connector	29
X21	Ground Test Point	N/A
X22	Ground Test Point	N/A
X23	PHYTEC Camera Interface	28
X24	HDMI Connector	26
X25	LCD LVDS Connector	26
X26	WiFi and Bluetooth Connector	19
X27	PCIe Connector	25
X28	GPIO Expansion Connectors	35
X30	USB-A Super Speed Host Connector (USB1)	21
X36	Cooling Fan Connector	30

13.2 Buttons and Switches

Table 17. Buttons and Switches

Ref. Des.	Description	Chapter
S1	System Reset Button	34
S2	Power Button	16
S3	User Button 1 (Labeled BTN1)	31
S4	User Button 2 (Labeled BTN2)	31
S5	Boot Switch	33

13.3 LEDs

Table 18. LEDs

Ref. Des.	Description	Chapter
D1	User LED 1 (Labeled LED1)	32
D2	User LED 2 (Labeled LED2)	32
D5	VDD_3V3 Power LED	16
D6	VDD_5V0 Power LED	16

Ref. Des.	Description	Chapter
D10	VDD_12V0 Power LED	16
D22	VCC_5V0 Power LED	16
D23	VCC_3V3 Power LED	16

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

14 Jumpers

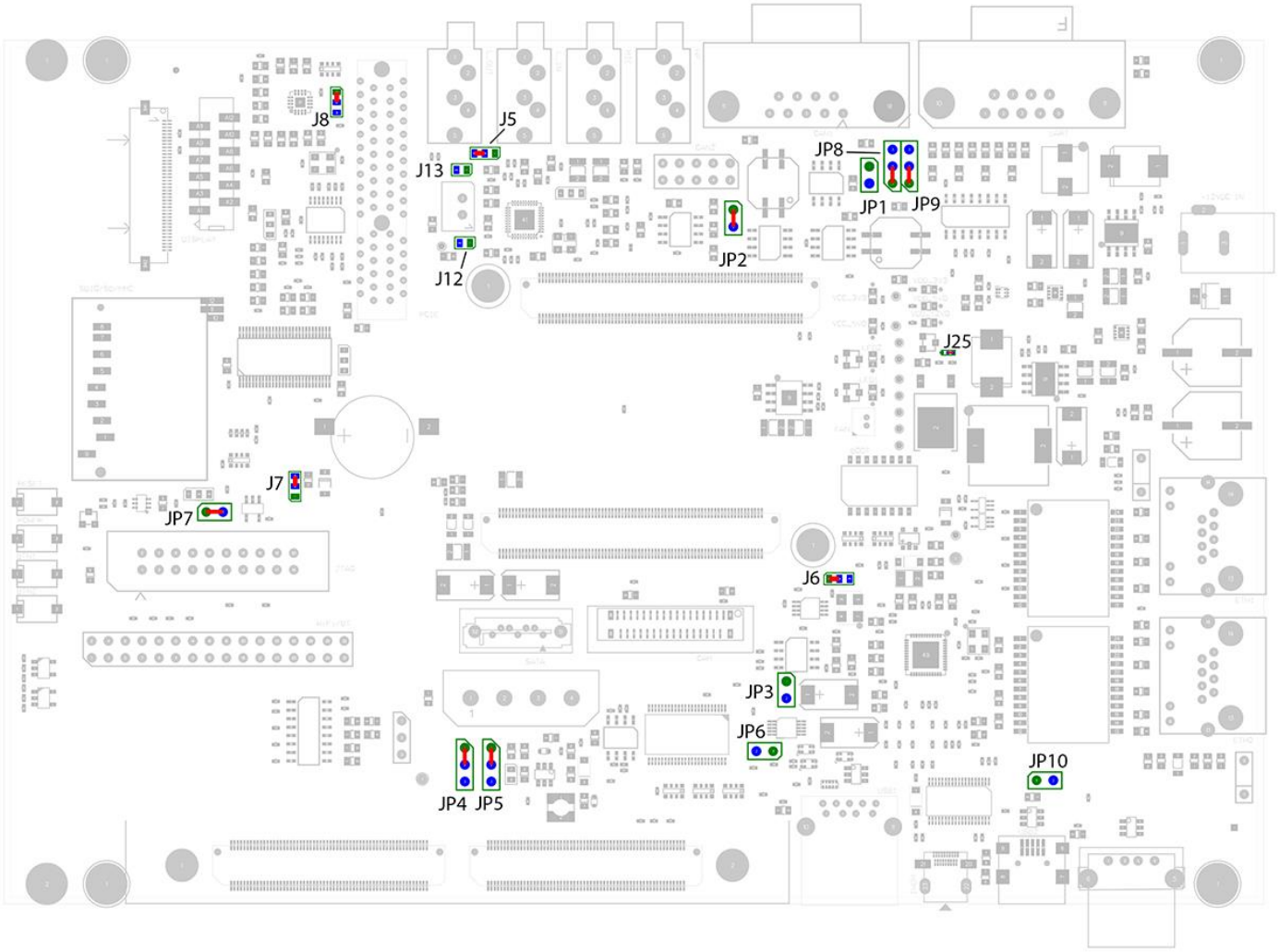

Figure 9. Jumper Locations and Default Settings

The phyCORE-AM57x Carrier Board is designed with various removable jumpers (JP) and several solder jumpers (J). These jumpers provide the user flexibility in routing a number of signals as well as configuring various control signals. Table 19 lists the solderless jumpers, their default positions, and the function they serve in each position. Table 20 lists the default positions and functions of the solder jumpers. For a detailed description of each jumper, reference the applicable chapter listed in the tables. Figure 9 provides a detailed view of the phyCORE-AM57x Carrier Board jumpers and their default settings.

Figure 10 details the jumper pad numbering scheme for reference when configuring the positions of the jumpers. Note that pin 1 is always designated by a cut corner on the PCB silk-screen.

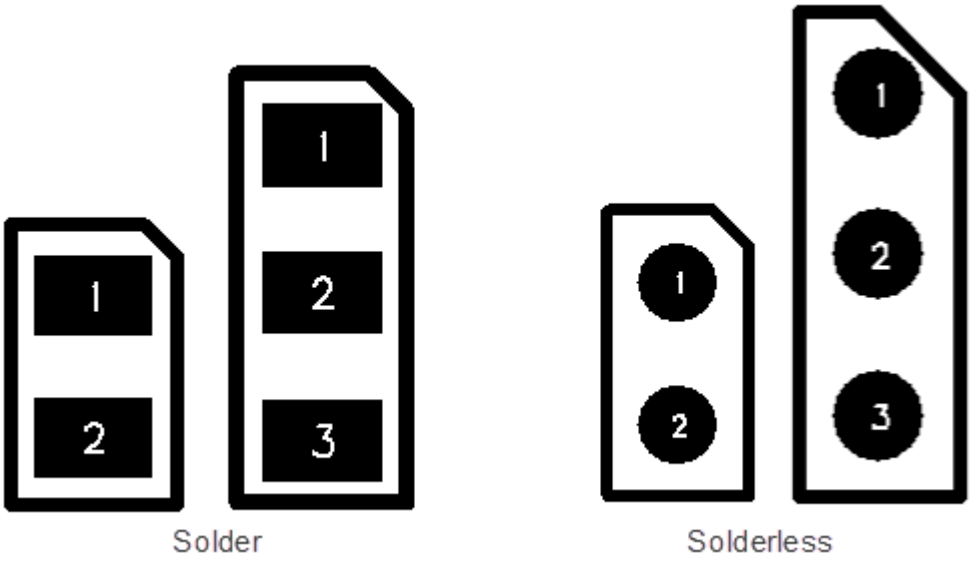

Figure 10. Jumper Numbering Scheme

The following conventions are used to describe jumper types.

J = solder jumper

JP = solderless jumper

The **bold** items in each table below represent the default configuration for each jumper.

Table 19. Solderless Jumper Settings

JP	Setting	Description	Chapter
JP1	**Open** Closed	**Configures the Carrier Board as an intermediate node on the CAN1 network.** Provides CAN1 termination impedance at the Carrier Board.	17
JP2	Open **Closed**	Configures the Carrier Board as an intermediate node on the CAN2 network. **Provides CAN2 termination impedance at the Carrier Board.**	17
JP3	**Open** Closed	**Sets USB2 capacitance on VBUS to 4.7uF for OTG mode.** Sets USB2 capacitance on VBUS so that an additional 150uF is added for Host mode.	21
JP4	**1+2** 2+3	**See phyCAM-P interface manual for operation of this jumper.**	28
JP5	**1+2** 2+3	**See phyCAM-P interface manual for operation of this jumper.**	28
JP6	**Open** Closed	**Selects the USB2 differential signals to be routed to the X9 OTG connector.** Selects the USB2 differential signals to be routed to the X19 USB-A connector.	21

JP7	**Open** Closed	**Disconnects X_JTAG_RTCK from X_JTAG_TCLK.** Connects X_JTAG_RTCK to X_JTAG_TCLK.	24
JP8	**1+2** 2+3	**Provides UART3_nRTS for UART3 hardware flow control.** Provides X_SPI2_nCS0 for SPI2 at the expansion connector.	22
JP9	**1+2** 2+3	**Provides UART3_nCTS for UART3 hardware flow control.** Provides X_SPI2_DIN for SPI2 at the expansion connector.	22
JP10	**Open** Closed	**USB2 OTG ID pin pulled high for OTG mode.** USB2 OTG ID pin grounded to set Host mode.	21

Table 20. Solder Jumper Settings

J	Setting	Description	Chapter
J5	1+2 **2+3**	Connects the shield contact of X9 (Headset Out) to ground, disables jack detection. **Connects the shield contact of X9 (Headset Out) to the HPCOM output of the audio codec, enables jack detection.**	29
J6	1+2 **2+3**	Selects internal reference clock for camera operation. **Selects external, fixed 26MHz clock for camera operation.**	28
J7	1+2 **2+3**	Disconnects Carrier Board battery from VBAT; VBAT will not be powered when main power is off. This setting is used when supplying VBAT from the expansion connector. **Sources the VBAT power rail from the BAT1 battery on the Carrier Board.**	16.4
J8	**1+2** 2+3	**Sets the touch controller A0 bit low, which configures the touch controller's I^2C address to 0x82.** Sets the touch controller A0 bit high, which configures the touch controller's I^2C address to 0x88.	27
J12	**Open** Closed	**Selects SPOM to X20-1.** Selects SWOUTM to X20-1. (See Audio Codec datasheet for further information)	29
J13	**Open** Closed	**Selects SPOP to X20-2.** Selects SWOUTP to X20-2. (See Audio Codec datasheet for further information)	29
J25	1+2 **2+3**	Directly enable VDD_12V0 to be powered. **VDD_12V0 is enabled by X_EXT_PWR_ON.**	16

15 phyCORE-AM57x SOM Connectivity

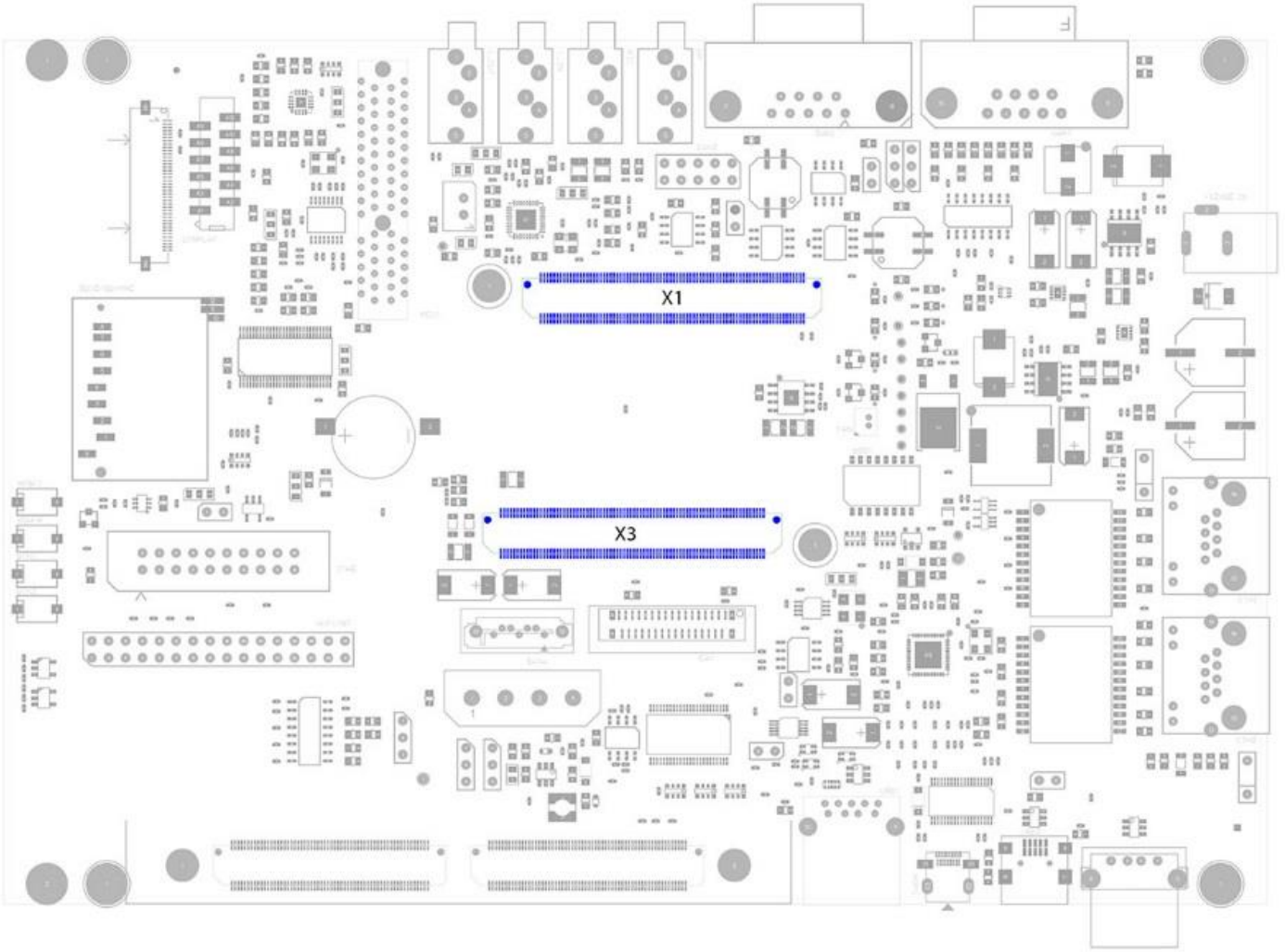

Figure 11. phyCORE-AM57x System on Module Connectivity to the Carrier Board

Connectors X1 and X3 on the Carrier Board provide connectivity for the phyCORE System on Module. The connectors are keyed for proper insertion of the SOM. Figure 11 above shows the location of the X1 and X3 connectors. The pin numbering scheme is shown in Figure 4.

16 Power

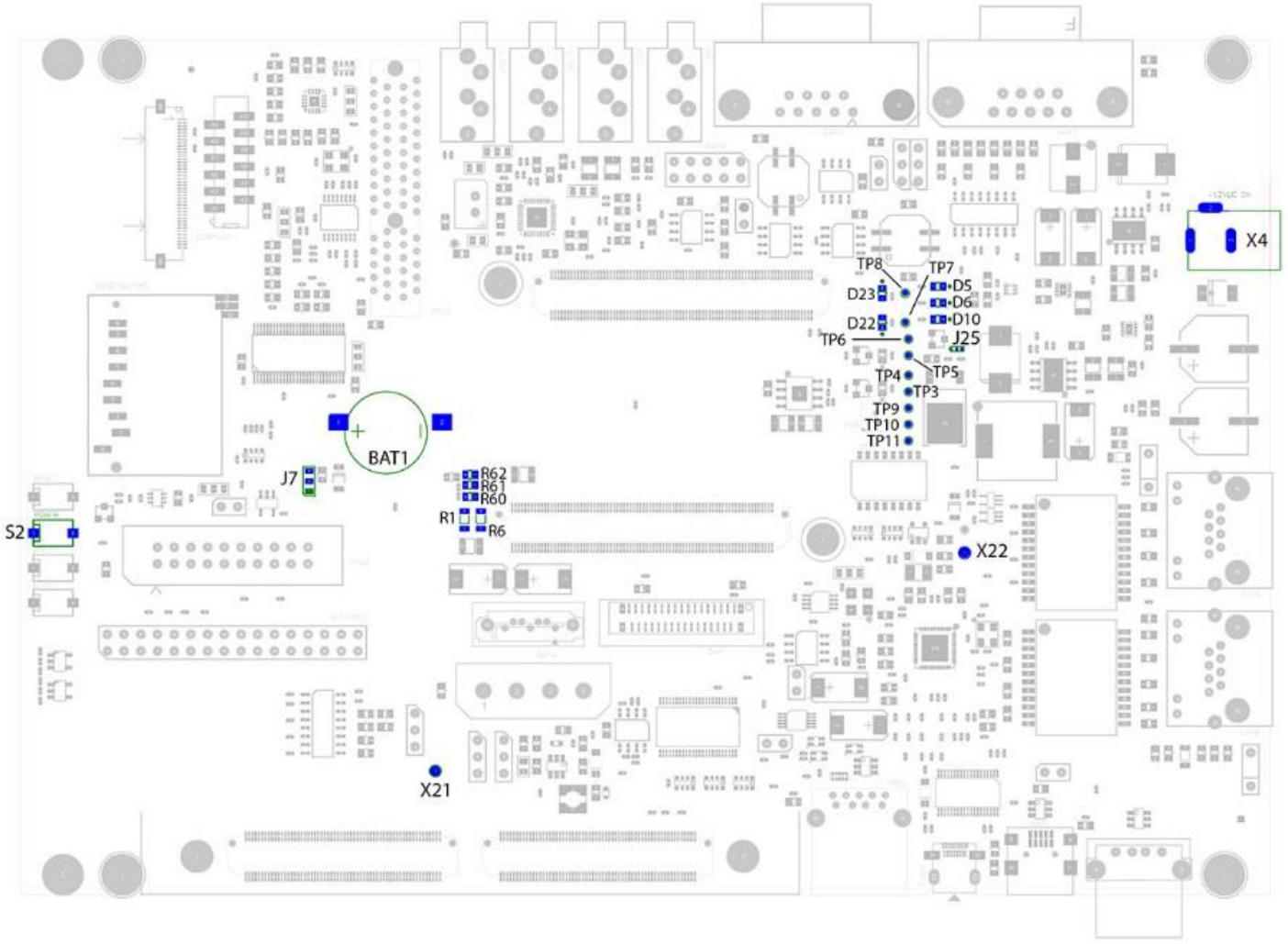

Figure 12. Power Scheme

The phyCORE-AM57x Carrier Board is powered through the power jack at connector X4 using an external 12V wall adapter. All on-board power supplies are generated from the 12V input supply except VBAT, which is generated by an on-board battery (BAT1).

The battery supply input (VBAT) to the SOM is powered directly from the battery at BAT1. By default, the Carrier Board comes with a battery installed, providing power to the SOM. Therefore, care should be taken before performing any electrical work on the boards to prevent shorting the battery.

The Carrier Board provides a power button at S2 that drives the X_PWRON signal. When S2 is pressed, it will pull X_PWRON low, which triggers a power-on interrupt on the PMIC located on the SOM. Please reference the PMIC datasheet for further details regarding this signal.

The power supply rails can be measured through several test pads (TP) present on the Carrier Board as shown in Figure 12. These test pads are described in detail in Table 21.

Table 21. Description of Power Supply Test Pads

Test Pad	Power Supply Rail
TP3	VDD_VCAM
TP4	ETH1_VDD_1V2
TP5	VDD_1V8
TP6	VDD_3V3
TP7	VDD_5V0
TP8	VDD_5V0
TP9	VCC_3V3
TP10	VDD_12V0
TP11	VBAT

The Carrier Board provides 5 status LEDs for the main power supply rails: D5, D6, D10, D22, and D23. The location of these LEDs on the carrier board is shown in Figure 12. The LEDs will turn on when their respective power supply rails are powered on. The power supplies these LEDs represent are shown in Table 22.

Table 22. Description of Power Supply Status LEDs

LED Name	Power Supply Rail
D5	VDD_3V3
D6	VDD_5V0
D10	VDD_12V0
D22	VCC_5V0
D23	VCC_3V3

Permissible input voltage at X4: +12 VDC regulated to ± 5%

The primary input power to the phyCORE-AM57x Carrier Board is located at X4. The required load current capacity of the power supply depends on the specific configuration of the phyCORE-AM57x SOM mounted on the Carrier Board, and the interfaces enabled while executing software. An adapter with a minimum supply of 2000 mA is recommended.

16.1 5V Supply

The Texas Instruments TPS54531 switching regulator (U21) powers the VCC_5V0 power supply rail, which in turn supplies power to the SOM.

The Texas Instruments TPS22965 load switch (U8) powers the VDD_5V0 power supply rail from VCC_5V0. The VDD_5V0 power supply rail powers various accessory circuits on the Carrier Board. Once the PMIC on the SOM has enabled all of its rails it will assert the X_EXT_PWR_ON signal to enable the load switch (U8), providing power to the VDD_5V0 rail.

This powering scheme verifies that the System on Module power is stable before providing power to the Carrier Board accessory circuits.

16.2 3V3 Supply

The Texas Instruments TPS54531 switching regulator (U29) powers the VCC_3V3 power supply rail, which in turn supplies power to the SOM.

The Texas Instruments TPS22965 load switch (U11) powers the VDD_3V3 power supply rail from VCC_3V3. The VDD_3V3 power supply rail powers most of the accessory circuits on the Carrier Board. Once the PMIC on the SOM has enabled all of its rails it will assert the X_EXT_PWR_ON signal to enable the load switch (U11), providing power to the VDD_3V3 rail.

This powering scheme verifies that the System on Module power is stable before providing power to the Carrier Board accessory circuits.

16.3 1V8 Supply

The Texas Instruments TLV70018DSE low dropout regulator (U23) powers the VDD_1V8 power supply rail. This power supply only powers a few accessory circuits on the Carrier Board, such as the WiFi/Bluetooth connector.

16.4 Battery

The phyCORE-AM57x Carrier Board utilizes a Panasonic ML1220 Lithium-Ion Battery (BAT1) to power the VBAT power supply rail when the main power is off. The VBAT supply will power the RTC on the SOM when the main power is off. The RTC requires a source of continuous power to keep time.

Be default, jumper J7 is configured to 2+3 to connect the VBAT supply to the phyCORE-AM57x. This configuration sources VBAT from the battery. J7 can be set to 1+2 to ground the VBAT supply, which will disconnect the battery. With VBAT grounded the RTC will not preserve time when the main power is off. If another VBAT solution is provided through the GPIO Expansion Board, then J7 can be set to 1+2 to prevent the Carrier Board battery solution from driving the VBAT rail.

16.5 Current Measurement

To facilitate current measurement, resistors R60 – R62, R1, and R6 are provided as current measurement access points. Replace these jumpers with precision shunt resistors and measure the voltage drop across the shunt resistors to calculate the current draw. A recommended value to begin with for your shunt resistor is 100mΩ on for the VDD_5V0 rail, and 10mΩ on for the VDD_3V3 rail. The shunt resistor should be small enough so that its voltage drop will not affect the output voltage. Yet the shunt resistors should be large enough to have a discernible measurement from supply noise.

17 Controller Area Network (CAN)

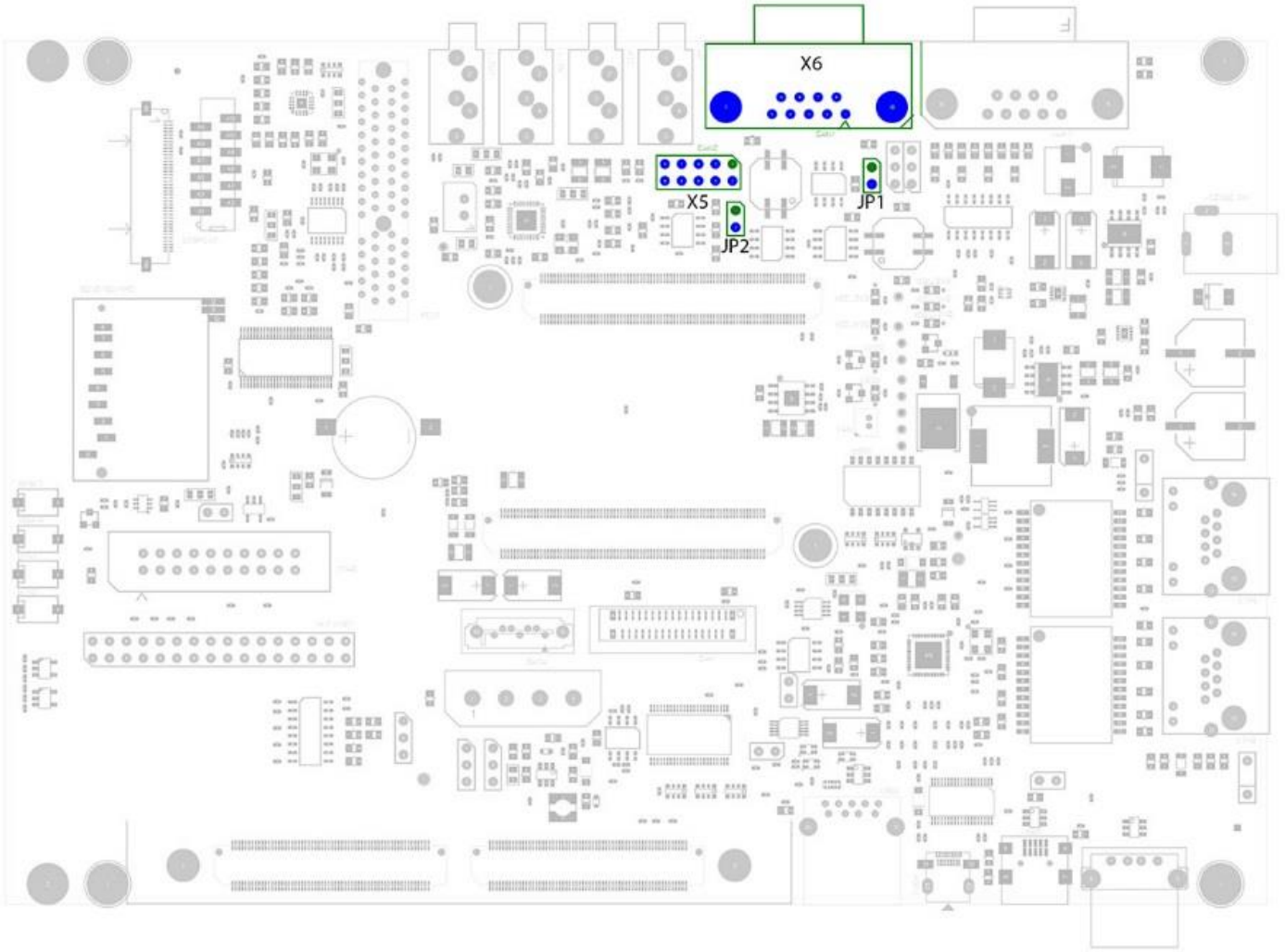

Figure 13. CAN Connectors and Jumpers

17.1 CAN1

The phyCORE-AM57x Carrier Board provides the CAN1 interface via the DB9 connector at X6.

The CAN1 signals are routed to a CAN transceiver (SN65HVDD234) at U3. The Carrier Board transceiver translates the single-ended CAN signals of the controller to the physical layer differential signals. These differential signals are then routed through the X6 connector. Additional ESD protection and EMI filtering are provided on the Carrier Board. CAN bus line termination can be enabled using a removable jumper (JP1).

Below is a detailed list of the connectors and jumpers associated with the CAN1 interface.

X6 Standard CAN DB9 connection point for CAN1 connectivity.

JP1 Jumper JP1 is provided to add 120 Ω termination impedance across the CAN1 data lines if necessary. By default, the jumper is OPEN so that the termination impedance is not added. This jumper position should be OPEN if the

Carrier Board is an intermediate node on the CAN network. JP1 should be set to CLOSED, adding termination impedance, when the Carrier Board is the end point of a CAN network.

17.2 CAN2

The phyCORE-AM57x Carrier Board provides the CAN2 interface via the 2x5 pin header X5.

The CAN2 signals are routed to a CAN transceiver (SN65HVDD234) at U4. The Carrier Board transceiver translates the single-ended CAN signals of the controller to the physical layer differential signals. These differential signals are then routed through the X5 connector. Additional ESD protection and EMI filtering are provided on the Carrier Board. CAN bus line termination can be enabled using a removable jumper (JP2).

Below is a detailed list of the connectors and jumpers associated with the CAN1 interface.

X5 Standard CAN DB9 connection point for CAN2 connectivity.

JP2 Jumper JP2 is provided to add 120 Ω termination impedance across the CAN2 data lines if necessary. By default, the jumper is CLOSED so that the termination impedance is added. This jumper position should be OPEN if the Carrier Board is an intermediate node on the CAN network. JP2 should be set to CLOSED, adding termination impedance, when the Carrier Board is the end point of a CAN network.

18 SDIO/SD/MMC

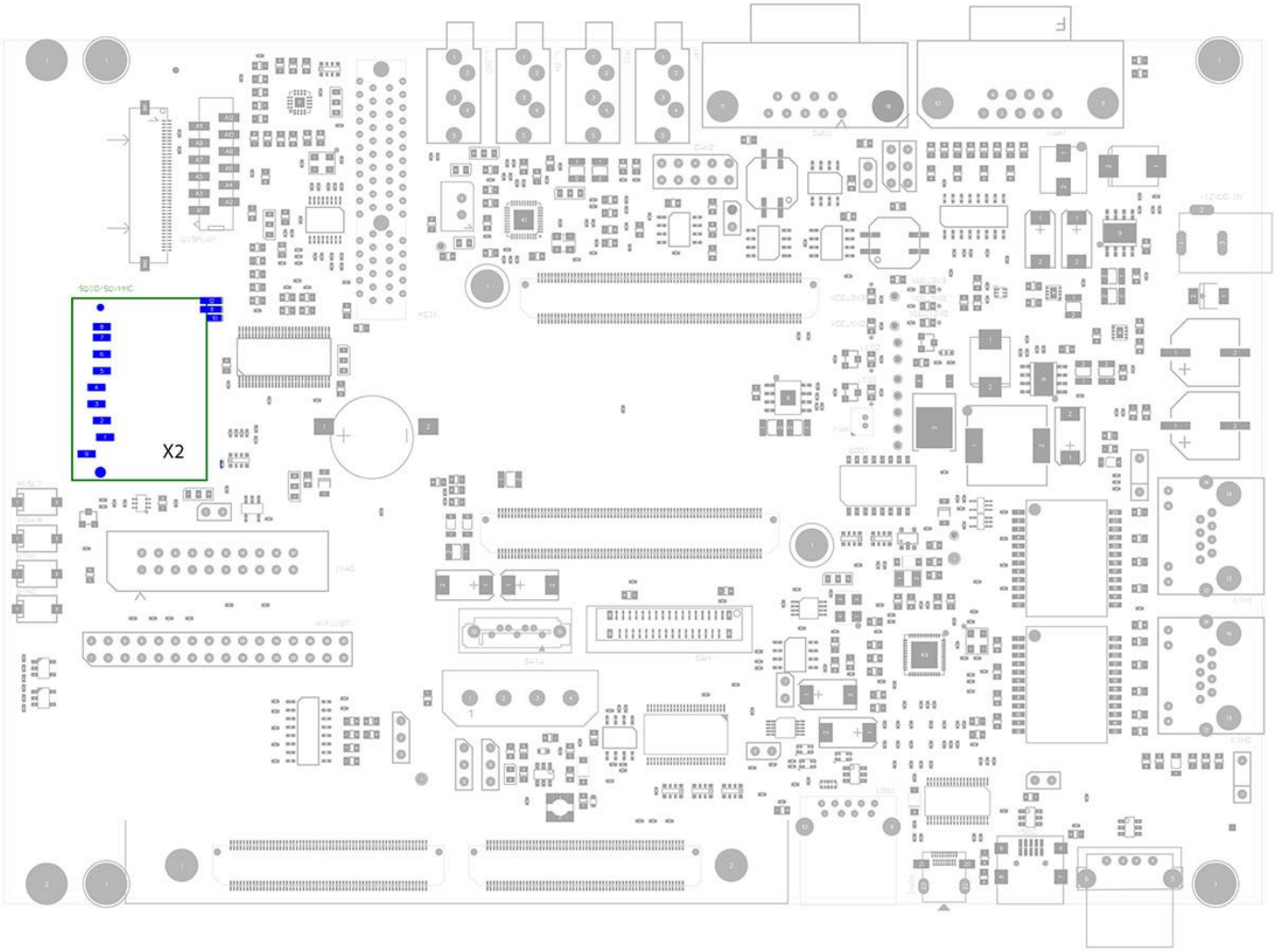

Figure 14. SDIO/SD/MMC Connectors and Jumpers

The phyCORE Carrier Board provides a standard Secure Digital Memory SDHC card slot at X2 for connection to SD / MMC interface cards via the MMC1 interface. The power circuit is controlled via the card detection function of the SD card connector. At initial card insertion, the VDD_SDMMC1 power supply is enabled by the card detect signal.

The phyCORE-AM57x supports an additional MMC3 interface. This interface is utilized through the WiFi/Bluetooth connector, and is documented in chapter 19.

19 WiFi/Bluetooth Connector

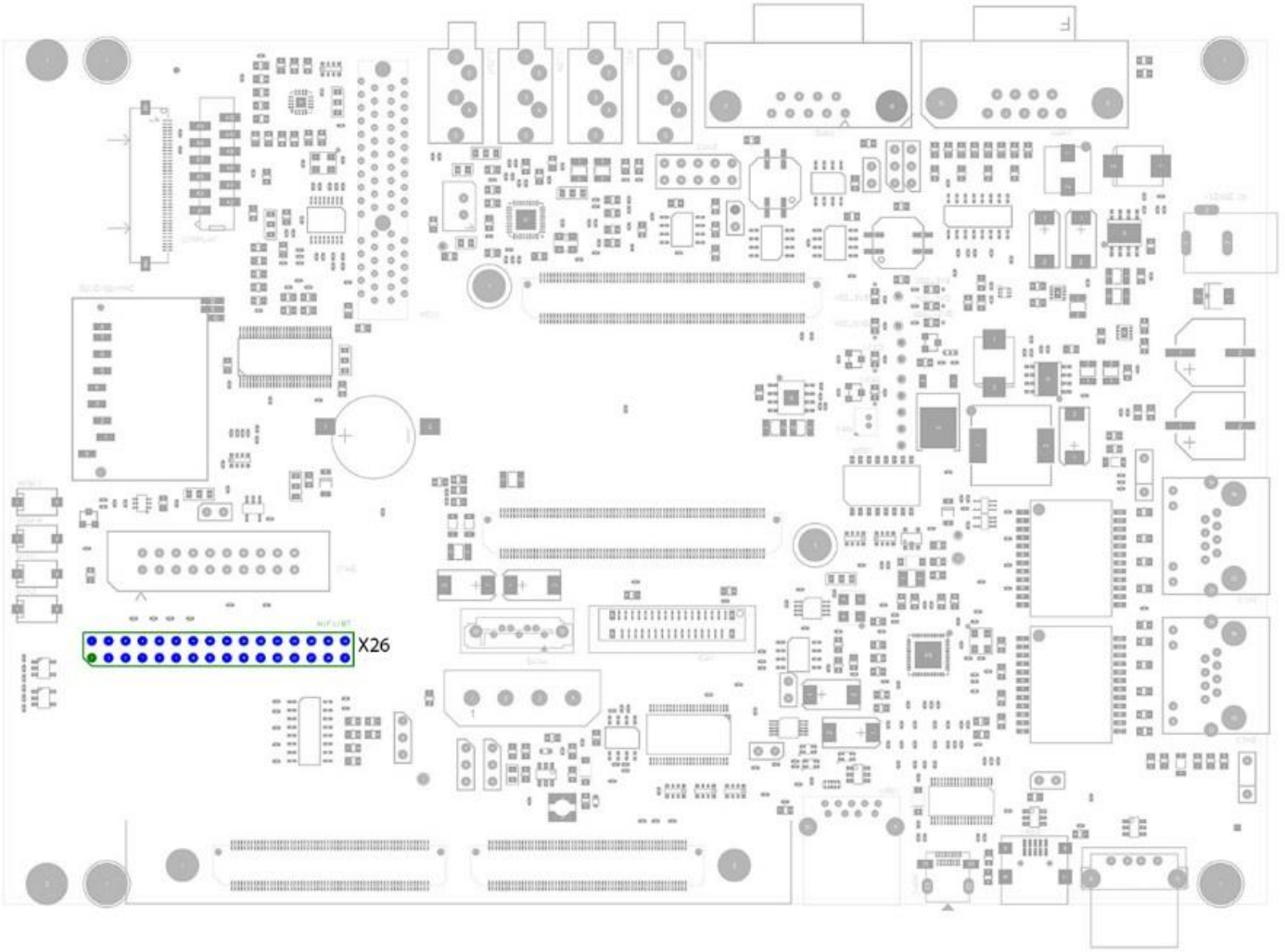

Figure 15. WiFi/Bluetooth Connector

The WiFi/Bluetooth connector (X26) is a 0.1”/2.54mm 2x16 pin header that provides connectivity for a WiFi/Bluetooth module, such as the PHYTEC PCM-958.

The signals routed to the WiFi/Bluetooth connector are listed in Table 23 below.

Table 23. WiFi/Bluetooth Signals at X26

Signal Type	Signal Name	Signal Level	Description	X26 Pin Number
Audio	X_MCASP2_FSX	3.3 V	Audio Frame	1
	X_MCASP2_AXR2	3.3 V	Audio Data	3
	X_MCASP2_AXR3	3.3 V	Audio Data	20
	X_MCASP2_ACLKX	3.3 V	Audio Clock	5
UART	X_KBD_COL0	3.3 V	UART10_TXD	9
	X_KBD_COL2	3.3 V	UART10_RTSn	11

	X_GPIO4_3	3.3 V	UART10_RXD	22
	X_KBD_COL1	3.3 V	UART10_CTSn	24
SD/MMC	X_MMC3_DAT0	3.3 V	MMC Data	29
	X_MMC3_DAT1	3.3 V	MMC Data	27
	X_MMC3_DAT2	3.3 V	MMC Data	25
	X_MMC3_DAT3	3.3 V	MMC Data	21
	X_MMC3_DAT4	3.3 V	MMC Data	17
	X_MMC3_DAT5	3.3 V	MMC Data	13
	X_MMC3_DAT6	3.3 V	MMC Data	19
	X_MMC3_DAT7	3.3 V	MMC Data	28
	X_MMC3_CLK	3.3 V	MMC Clock	32
	X_MMC3_CMD	3.3 V	MMC Command	30
Power/Ground	VDD_3V3	-	3.3 V Supply	10, 12, 14, 16
	VDD_1V8	-	1.8 V Supply	4, 6
	GND	-	Ground	2, 7, 8, 15, 18, 23, 26, 31

20 Ethernet

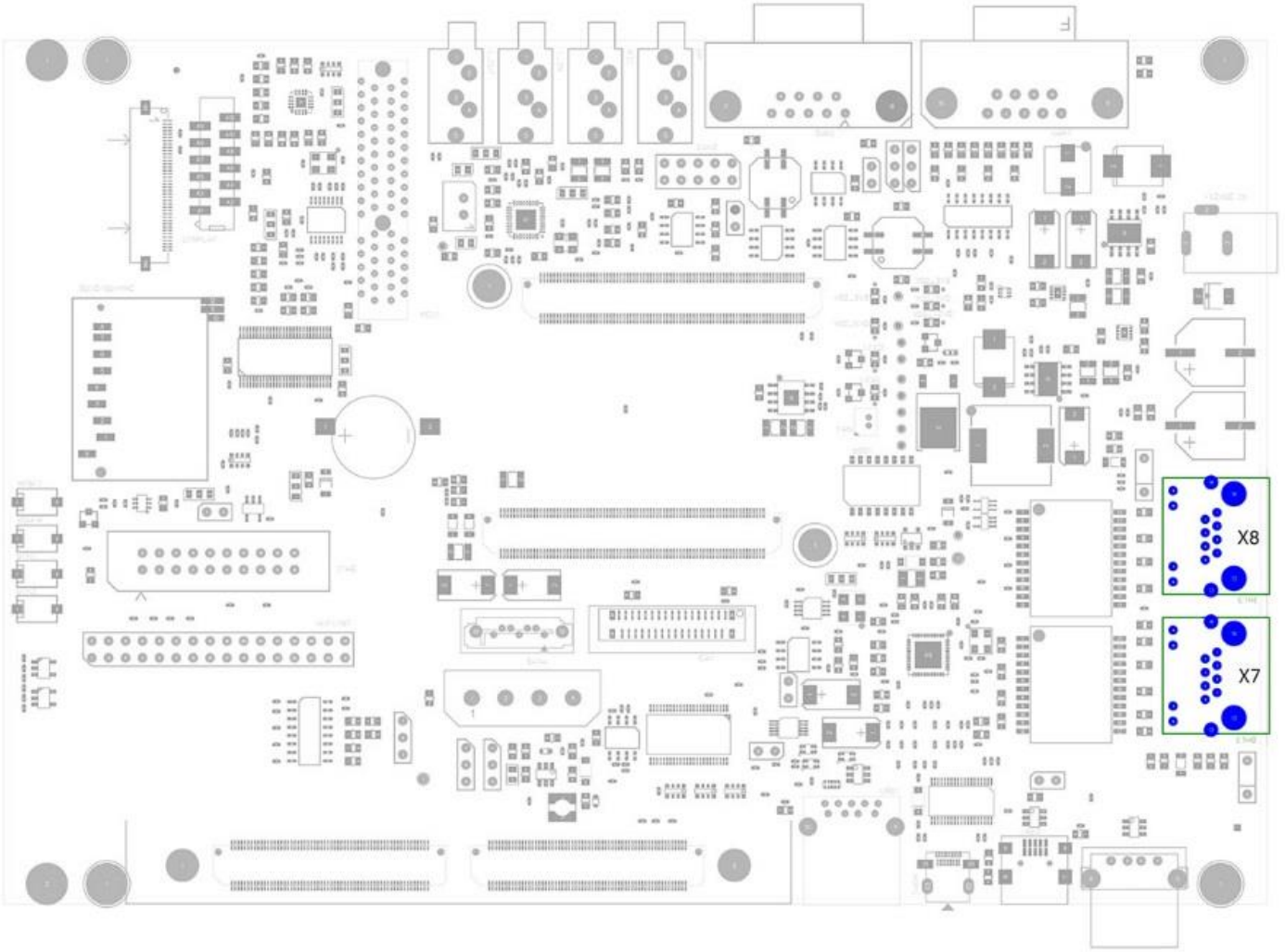

Figure 16. Ethernet Connectors

20.1 ETH0

The Ethernet0 interface of the phyCORE-AM57x is accessible at an RJ-45 connector (X7) on the Carrier Board. The indication LEDs for SPEED (green) and LINK (yellow) are integrated into the connector.

The differential pairs from the phyCORE-AM57x SOM transceiver are routed through a gigabit magnetics module to the RJ-45 connector at X7.

20.2 ETH1

The Ethernet1 interface of the phyCORE-AM57x is accessible at an RJ-45 connector (X8) on the Carrier Board. The indication LEDs for SPEED (green) and LINK (yellow) are integrated into the connector.

The single-ended Ethernet1 RGMII signals from the AM57x route through the phyCORE connector to a Micrel KSZ9031RNX RGMII Ethernet transceiver at U20. The differential pairs from the transceiver are then routed through a gigabit magnetics module to the RJ-45 connector at X8.

The default strapping options are listed in Table 24 below.

Table 24. Ethernet1 Default Strapping Options

Strapping Option	Signal Names	Strapping Value	Function
RGMII Mode	X_RGMII1_RXD3 X_RGMII1_RXD2 X_RGMII1_RXD1 X_RGMII1_RXD0	1 1 1 1	Advertise all capabilities (10/100/1000 speed half-/full-duplex)
LED Mode	ETH1_LED_MODE	1	Single-LED Mode
PHY Address	X_RGMII1_RXC (PHYAD2) ETH1_LED2 (PHYAD1) ETH1_LED1 (PHYAD0)	0 1 0	Set the PHY address to **0x02.**
125MHz reference clock output	X_RGMII1_RXCTL	0	Disable 125MHz clock output at Pin 41 (CLK125_NDO)

Please reference the KSZ9031RNX datasheet for detailed information regarding the strapping options.

21 USB

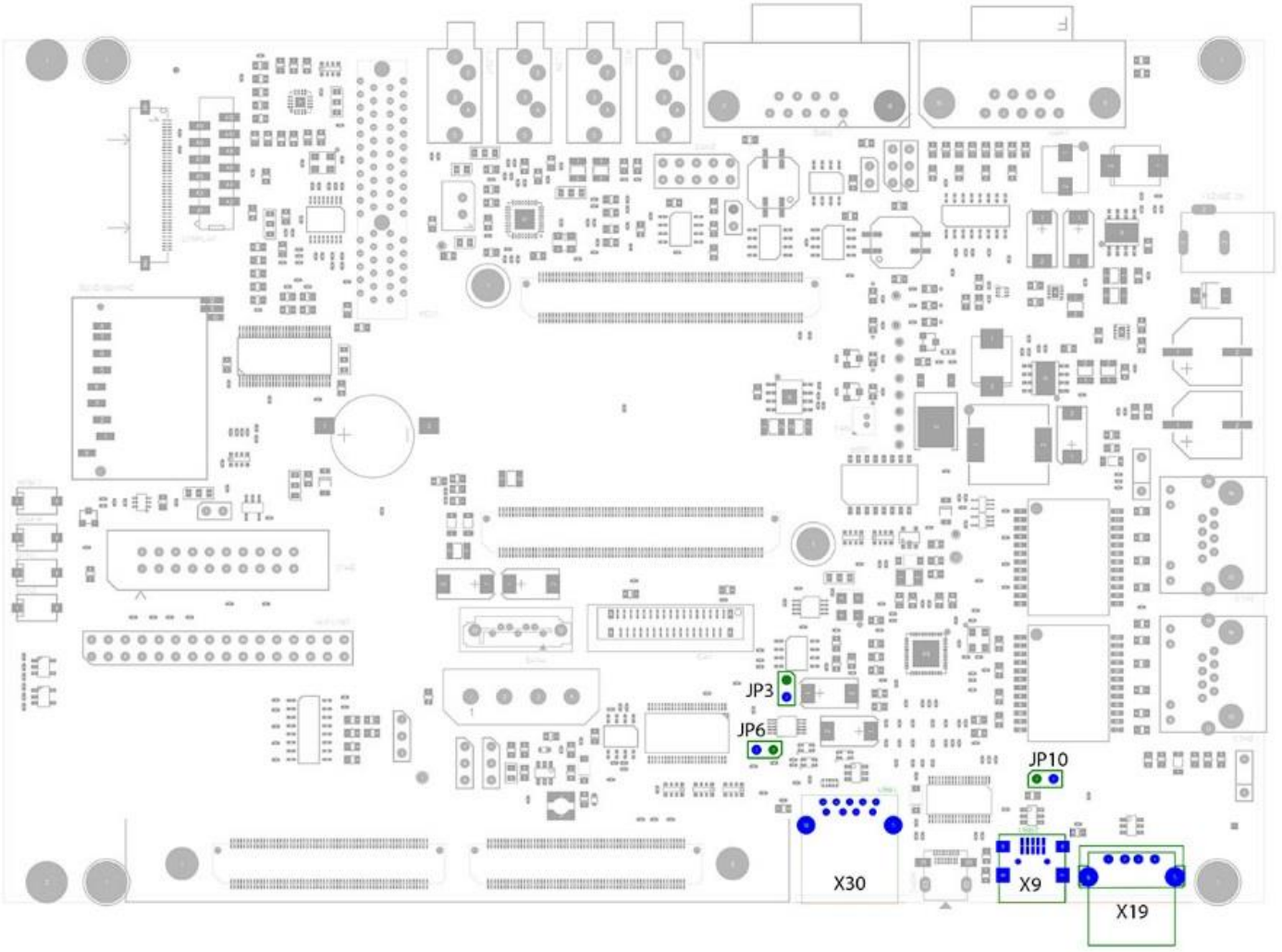

Figure 17. USB Connectors and Jumpers

21.1 USB1

The USB1 interface supports USB 3.0 SuperSpeed signals. The interface is accessible through a USB3.0 Standard-A host connector at X30. The USB1 interface is compliant with USB revision 3.0.

Below is a detailed description of the USB1 connector.

X30 USB 3.0 Standard-A host connection interface. Connect a USB 3.0 Standard-A mating cable to this connector when operating this USB interface in host mode.

21.2 USB2

The USB2 interface supports On-The-Go (OTG). USB OTG devices are capable of initiating a session, controlling the connection, and exchanging host and peripheral roles between each other. This interface is accessible through a USB Mini-AB OTG connector at X9 or a USB Standard-A host connector at X19, which is determined by the provided jumper control. Jumpers JP3, JP6, and JP10 are used to select which connector, X9 or X19, will be used. The AM57x USB2 interface is compliant with USB revision 2.0.

Below is a detailed list of the connectors and jumpers associated with the USB2 interface.

X9 USB Mini-AB OTG connection interface. To use the USB2 interface in OTG mode via this connector, open jumpers JP3, JP6, and JP10. Connect a USB OTG cable to this connector when operating this USB interface in OTG mode. Connect a USB Mini-AB connector to this interface to use in peripheral mode.

X19 USB Standard-A host connection interface. To use the USB2 interface in Host mode via this connector, close jumpers JP3, JP6, and JP10. Connect a USB Standard-A mating cable to this connector when operating this USB interface in host mode.

JP3 Controls the VBUS capacitance level for OTG mode and Host mode operation. By default, this jumper is open, which sets the VBUS capacitance to 4.7uF. This jumper should be left open when operating in OTG mode via the X9 connector. Close this jumper to add another 150uF of capacitance on VBUS when operating in Host mode via the X19 connector.

JP6 Determines which USB connector is active. By default, this jumper is open, which routes the USB differential data signals to the OTG connector at X9. Close this jumper to route the signals to the host connector at X19.

JP10 Sets the state of the ID signal. By default, this jumper is open, which allows the R35 pull-up resistor to pull the ID signal high for use with OTG mode on connector X9. Close this jumper to ground this signal when operating in Host mode via the X19 connector.

22 RS-232

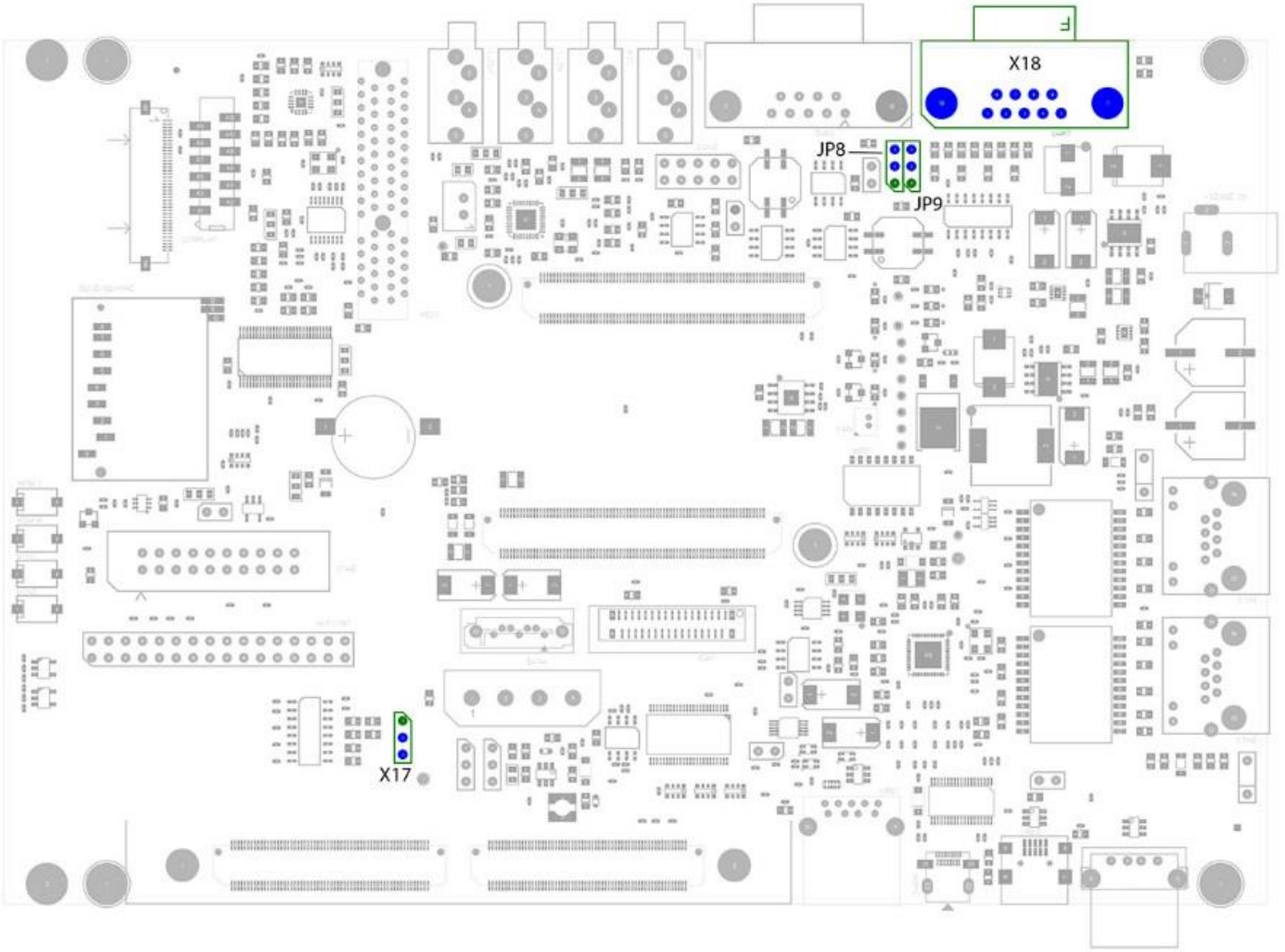

Figure 18. RS-232 Connectors

The phyCORE-AM57x provides connectivity to the UART3 and UART5 interfaces through two connectors on the Carrier Board at RS-232 level. The DB9 connector X18 provides the UART3 signals, and the UART5 interface is provided through a 3 pin 0.1”/2.54mm spaced header at X17. Two RS-232 transceivers at U6 and U7 convert the TTL level signals from the SOM to RS-232 level signals.

Figure 19 provides the pin numbering scheme for the DB9 connector at X18. Table 25 provides a detailed description of the signals routed to X18.

The UART3 interface provides RTS and CTS signals, allowing for hardware flow control. The UART3 control signals are multiplexed with signals from the SPI2 interface. Jumpers JP8 and JP9 determine which interface is selected (SPI2 vs. UART3). The UART3 RTS and CTS are selected/enabled by default.

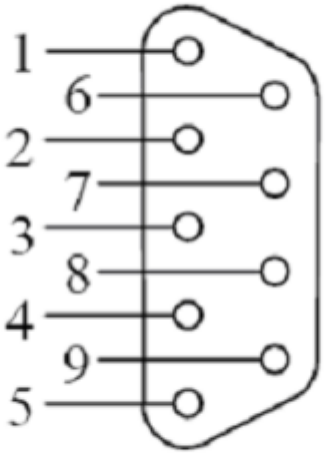

Figure 19. DB9 RS-232 Connector X18 (UART 3) Pin Numbering

Table 25. UART3 DB9 (X18) Pin Description

Pin	Signal	I/O	Description
1	N.C.	-	Not Connected
2	UART3_TX	O	UART3 Transmit
3	UART3_RX	I	UART3 Receive
4	N.C.	-	Not Connected
5	GND	-	Ground
6	N.C.	-	Not Connected
7	UART3_CTS	I	UART3 Clear To Send
8	UART3_RTS	O	UART3 Request To Send
9	N.C.	-	Not Connected

Table 26 provides a detailed description of the signals routed to X17.

The UART5 interface does not support RTS and CTS signals for hardware flow control.

Table 26. UART5 Header (X17) Pin Description

Pin	Signal	I/O	Description
1	UART5_TX	O	UART5 Transmit
2	GND	-	Ground
3	UART5_RX	I	UART5 Receive

A detailed list of applicable configuration jumpers and connectors is provided below.

X17 UART5 3 pin header connection point. This connector supports RS-232 level signals.

X18 UART3 DB9 connection point. This connector supports RS-232 level signals

JP8 This jumper routes X_SPI2_nCS0 to UART3_nRTS when set to the default setting of 1+2. When jumper JP8 is set to 2+3, the X_SPI2_nCS0 signal will be routed to the expansion connector as SPI2_nCS0.

JP9 This jumper routes X_SPI2_DIN to UART3_nCTS when set to the default setting of 1+2. When jumper JP9 is set to 2+3, the X_SPI2_DIN signal will be routed to the expansion connector as SPI2_DIN.

23 SATA

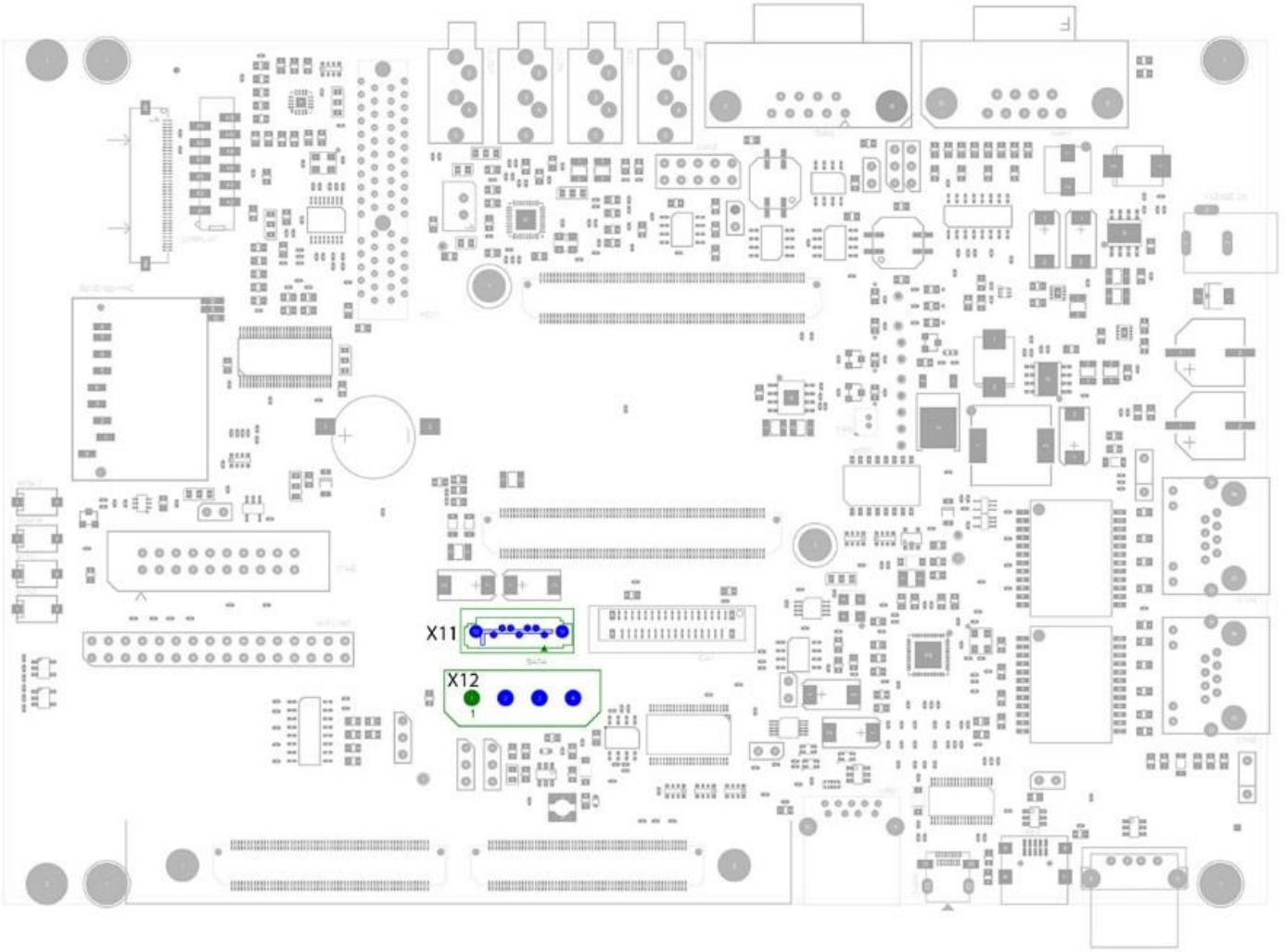

Figure 20. SATA Power and Signal Connectors

The phyCORE-AM57x Carrier Board provides support to connect a SATA hard disk drive. The Carrier Board provides a data signal connector at X11 and a power supply connector at X12. The pin descriptions for X11 and X12 are provided in Table 27 and Table 28 respectively.

Table 27. SATA Data Connector (X11) Pin Description

Pin	Signal	Description
1	GND	Ground
2	X_SATA_TX+	SATA Transmit +
3	X_SATA_TX-	SATA Transmit-
4	GND	Ground
5	X_SATA_RX-	SATA Receive -
6	X_SATA_RX+	SATA Receive +
7	GND	Ground

Pin	Signal	Description
S1	SHIELD1	Ground
S2	SHIELD2	Ground

Table 28. SATA Power Connector (X12) Pin Description

Pin	Signal	Description
1	VDD_12V0	12 V Power Supply
2	GND	Ground
3	GND	Ground
4	VDD_5V0	5 V Power Supply

24 JTAG

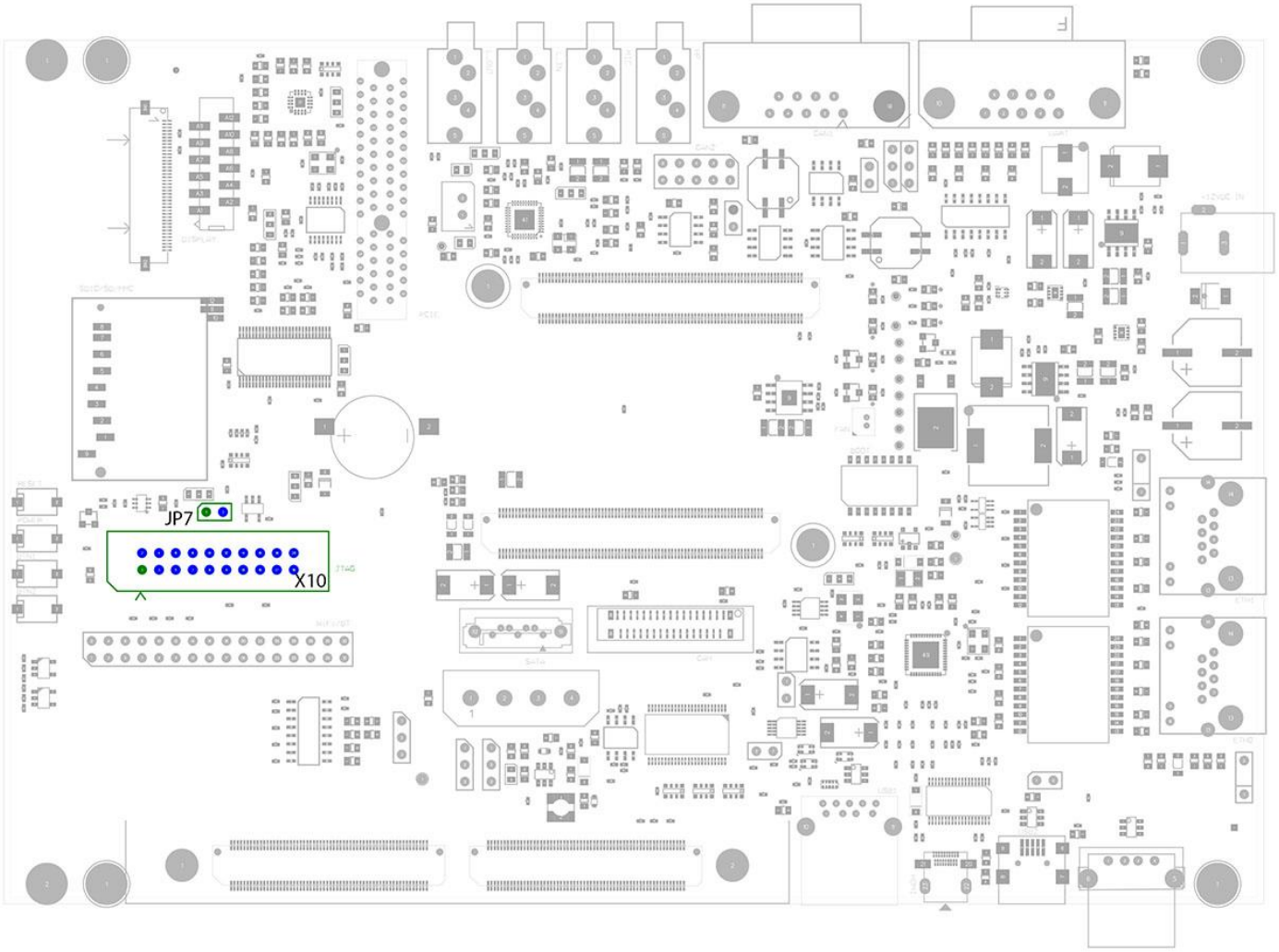

Figure 21. JTAG Debug Connector

The phyCORE-AM57x JTAG interface is accessible at connector X10 on the Carrier Board. This interface is compliant with JTAG specification IEEE 1149.1 or IEEE 1149.7. The angled corner of the connector designates the location of pin 1. Table 29 describes each pin of the JTAG connector.

NOTE:

Jumper **JP7** should be set to **OPEN** for proper JTAG operation, it should **NOT** be populated/closed. Since the AM57x processor has an RTCK pin, this signal should be connected directly to the JTAG connector and not to TCK.

Table 29. JTAG Connector (X10) Pin Description

Pin	Signal	Description
1, 2	VDD_3V3	JTAG Chain Reference Voltage
3	X_JTAG_nTRST	JTAG Chain Test Reset
4, 6, 8, 10, 12, 14, 16, 18, 20	GND	Ground
5	X_JTAG_TDI	JTAG Chain Test Data Input
7	X_JTAG_TMS	JTAG Chain Test Mode Select
9	X_JTAG_TCLK	JTAG Chain Test Clock
11	X_JTAG_RTCK	JTAG Chain Return Test Clock
13	X_JTAG_TDO	JTAG Chain Test Data Output
15	JTAG_SRST	System Reset
17, 19	N.C.	Not Connected

25 PCIe

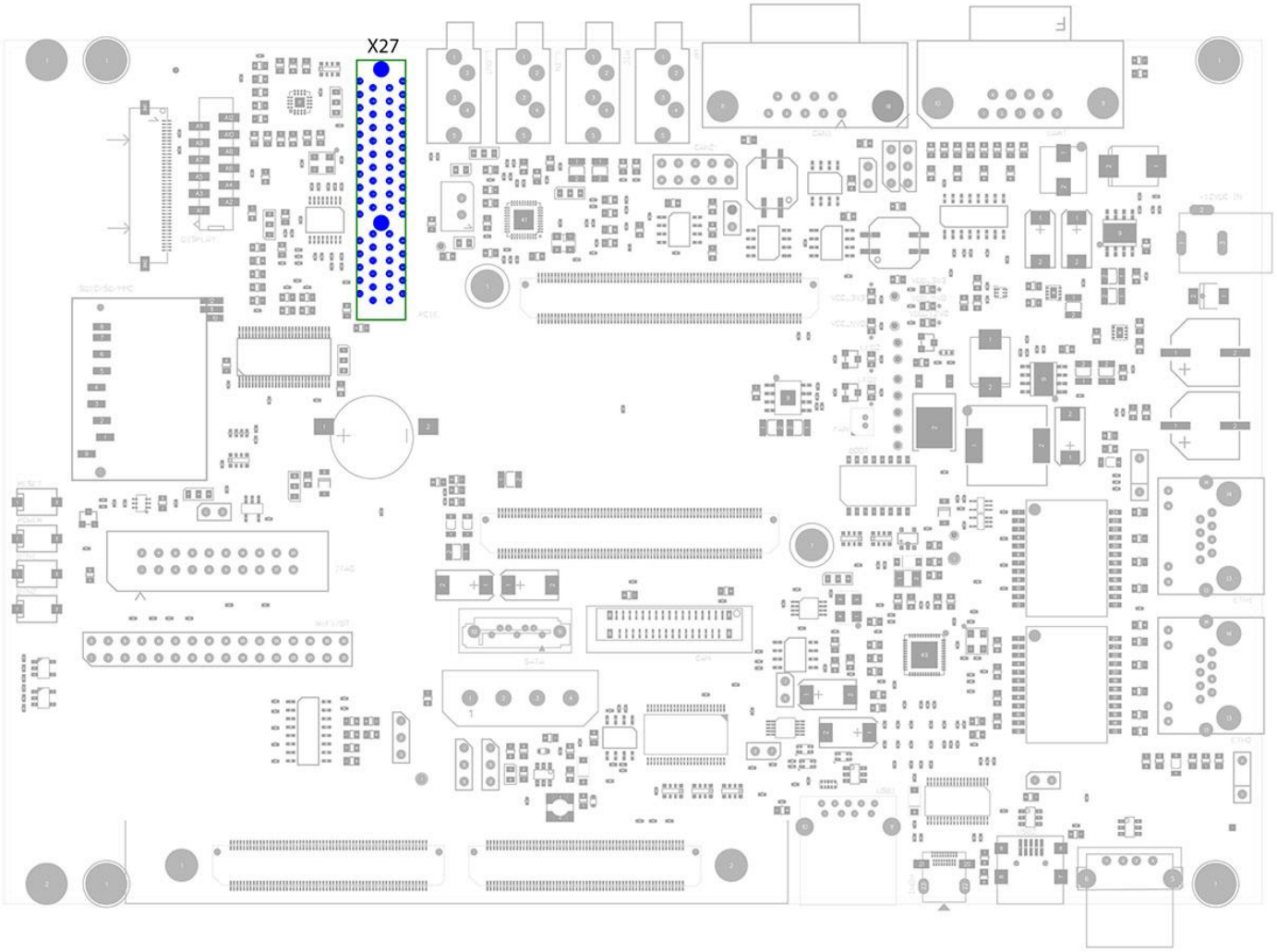

Figure 22. PCIe Connector

PCI-Express connectivity is accessible at the 4x PCIe connector at X27, which provides 2x PCIe lanes. The reference clock signals are generated externally by a PI6C557-03 PCI Express Clock generator at U28.

The pin descriptions for the PCIe connector are listed in Table 30 below.

Table 30. PCIe Connector (X27) Pin Description

Pin	Side B			Side A	
#	Name	Description		Name	Description
1	VDD_12V0	12 V Power Supply		GND	Ground
2	VDD_12V0	12 V Power Supply		VDD_12V0	12 V Power Supply
3	N.C.	Not Connected		VDD_12V0	12 V Power Supply
4	GND	Ground		GND	Ground
5	N.C.	Not Connected		N.C.	Not Connected

6	N.C.	Not Connected		N.C.	Not Connected
7	GND	Ground		N.C.	Not Connected
8	VDD_3V3	3.3 V Power Supply		N.C.	Not Connected
9	N.C.	Not Connected		VDD_3V3	3.3 V Power Supply
10	VDD_3V3	3.3 V Power Supply		VDD_3V3	3.3 V Power Supply
11	WAKE	Link Reactivation		PWRGD	Power Good
12	N.C.	Not Connected		GND	Ground
13	GND	Ground		PCIE_REFCLKP	PCIe Reference Clock +
14	X_PCIe_TXP0	PCIe Lane 0 Transmit +		PCIe_REFCLKn	PCIe Reference Clock -
15	X_PCIe_TXN0	PCIe Lane 0 Transmit -		GND	Ground
16	GND	Ground		X_PCIe_RXP0	PCIe Lane 0 Receive +
17	PRSNT2_1	Hot plug Detect		X_PCIe_RXN0	PCIe Lane 0 Receive -
18	GND	Ground		GND	Ground
19	X_PCIe_TXP1	PCIe Lane 1 Transmit +		N.C.	Not Connected
20	X_PCIe_TXN1	PCIe Lane 1 Transmit -		GND	Ground
21	GND	Ground		X_PCIe_RXP1	PCIe Lane 1 Receive +
22	GND	Ground		X_PCIe_RXN1	PCIe Lane 1 Receive -
23	N.C.	Not Connected		GND	Ground
24	N.C.	Not Connected		GND	Ground
25	GND	Ground		N.C.	Not Connected
26	GND	Ground		N.C.	Not Connected
27	N.C.	Not Connected		GND	Ground
28	N.C.	Not Connected		GND	Ground
29	GND	Ground		N.C.	Not Connected
30	N.C.	Not Connected		N.C.	Not Connected
31	N.C.	Not Connected		GND	Ground
32	GND	Ground		N.C.	Not Connected

26 Display

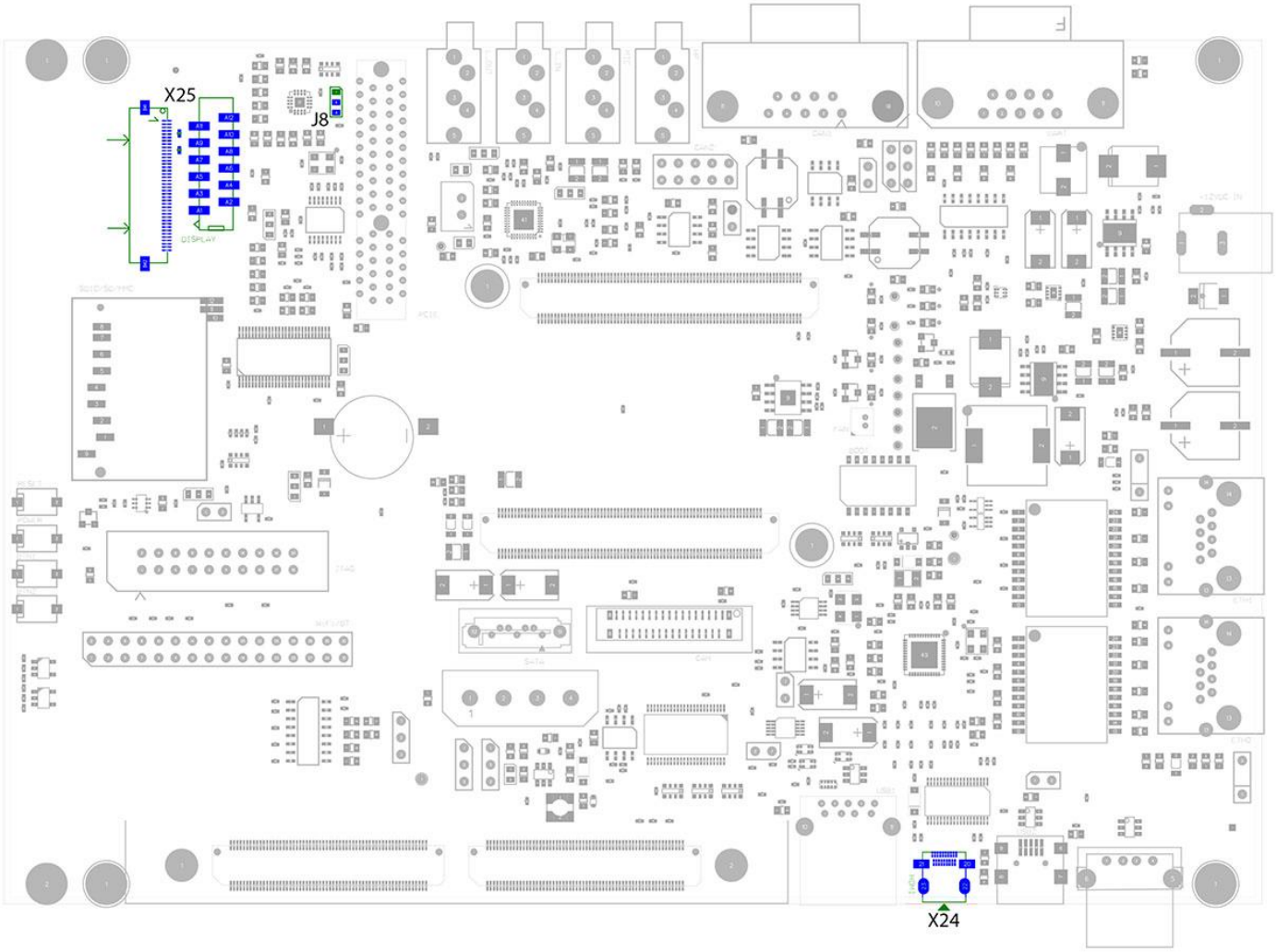

Figure 23. Display Connectors and Jumpers

26.1 HDMI

The phyCORE-AM57x High-Definition Multimedia Interface is compliant with HDMI 1.4a, HDCP 1.4, and DVI 1.0.

The HDMI signals are routed from the SOM through an ESD protection and current limiter IC at U25. The signals are then accessible through the Micro-HDMI connector at X24. The HDMI signals are described in Table 31.

Table 31. Micro-HDMI Connector (X24) Pin Description

Pin	Signal	Description
1	HDMI_HPD_OUT	Hot Plug Detection
2	GND	Reserved
3	X_HDMI1_D2+	Data Channel 2 Positive Output
4	GND	Shield

5	X_HDMI1_D2-	Data Channel 2 Negative Output
6	X_HDMI1_D1+	Data Channel 1 Positive Output
7	GND	Shield
8	X_HDMI1_D1-	Data Channel 1 Negative Output
9	X_HDMI1_D0+	Data Channel 0 Positive Output
10	GND	Shield
11	X_HDMI1_D0-	Data Channel 0 Negative Output
12	X_HDMI1_CLK+	Clock Positive Output
13	GND	Shield
14	X_HDMI1_CLK-	Clock Negative Output
15	HDMI_CEC_OUT	Consumer Electronics Control
16	GND	Shield
17	HDMI_CTRL_CK_OUT	DDC Clock
18	HDMI_CTRL_DAT_OUT	DDC Data
19	HDMI_5V	5 V Power Supply
20	HDMI_SHIELD	Shield
21	HDMI_SHIELD	Shield
22	HDMI_SHIELD	Shield
23	HDMI_SHIELD	Shield

26.2 LVDS

Support for LVDS LCDs is provided through X25, which is comprised of an LVDS signal connector and a power connector. These connectors provide connection to support various PHYTEC LCDs, such as LCD-018. The LVDS data connector signals are described in Table 32. The LVDS power connector signals are described in Table 33.

Table 32. LVDS Data Connector (X25) Pin Description

Pin	Signal	Description
1	X_SPI1_CLK	SPI1 Clock
2	X_SPI1_DIN	SPI1 Master Data In; Slave Data Out
3	X_SPI1_DOUT	SPI1 Master Data Out; Slave Data In
4	X_nSPI1_CS0	SPI1 Chip Select 0
5	X_GPIO8_22	LVDS Interrupt
6	VDD_3V3	Logic Supply Voltage
7	X_I2C4_SCL	I^2C Clock Signal
8	X_I2C4_SDA	I^2C Data Signal
9	GND	Ground
10	X_EHRPWM1A	PWM Brightness Control
11	VDD_3V3	Logic Supply Voltage
12	N.C.	Not Connected
13	X_GPIO8_23	Display Enable Signal
14	N.C.	Not Connected
15	GND	Ground
16	N.C.	Not Connected
17	N.C.	Not Connected
18	GND	Ground

19	LVDS_S0-	LVDS Data Channel 0 Output -
20	LVDS_S0+	LVDS Data Channel 0 Output +
21	GND	Ground
22	LVDS_S1-	LVDS Data Channel 1 Output -
23	LVDS_S1+	LVDS Data Channel 1 Output +
24	GND	Ground
25	LVDS_S2-	LVDS Data Channel 2 Output -
26	LVDS_S2+	LVDS Data Channel 2 Output +
27	GND	Ground
28	LVDS_S3-	LVDS Data Channel 3 Output -
29	LVDS_S3+	LVDS Data Channel 3 Output +
30	GND	Ground
31	LVDS_CK-	LVDS Clock Channel Output -
32	LVDS_CK+	LVDS Clock Channel Output +
33	GND	Ground
34	TOUCH_X+	Touch Controller X Output +
35	TOUCH_X-	Touch Controller X Output -
36	TOUCH_Y+	Touch Controller Y Output +
37	TOUCH_Y-	Touch Controller X Output -
38	N.C.	Not Connected
39	GND	Ground
40	N.C.	Not Connected

Table 33. LVDS Power Connector (X25) Pin Description

Pin	Signal	Description
1	GND	Ground
2	VDD_3V3	3.3V Power Supply
3	GND	Ground
4	VDD_5V0	5V Power Supply
5	GND	Ground
6	VDD_5V0	5V Power Supply
7	GND	Ground
8	VDD_5V0	5V Power Supply
9	GND	Ground
10	X_EHRPWM1A	PWM Brightness Output Control
11	N.C.	Not Connected
12	N.C.	Not Connected

27 Touch Controller

The phyCORE-AM57x Carrier Board provides a touch controller (STMPE811) at U13. The touch controller interfaces with a resistive touch panel typically integrated into an LCD. The touch controller communicates with the AM57x through I^2C. The default I^2C address is 0x82. The touch signals are routed to the LVDS connector X25 to support an external resistive touch panel.

The configuration jumper J8 is described below.

J8 Configures the I^2C address of the touch controller. The default configuration 1+2 sets the touch controller A0 bit low, which configures the touch controller's I^2C address to 0x82. Configuring J8 to 2+3 drives the touch controller A0 bit high, which configures the touch controller's I^2C address to 0x88.

28 Camera

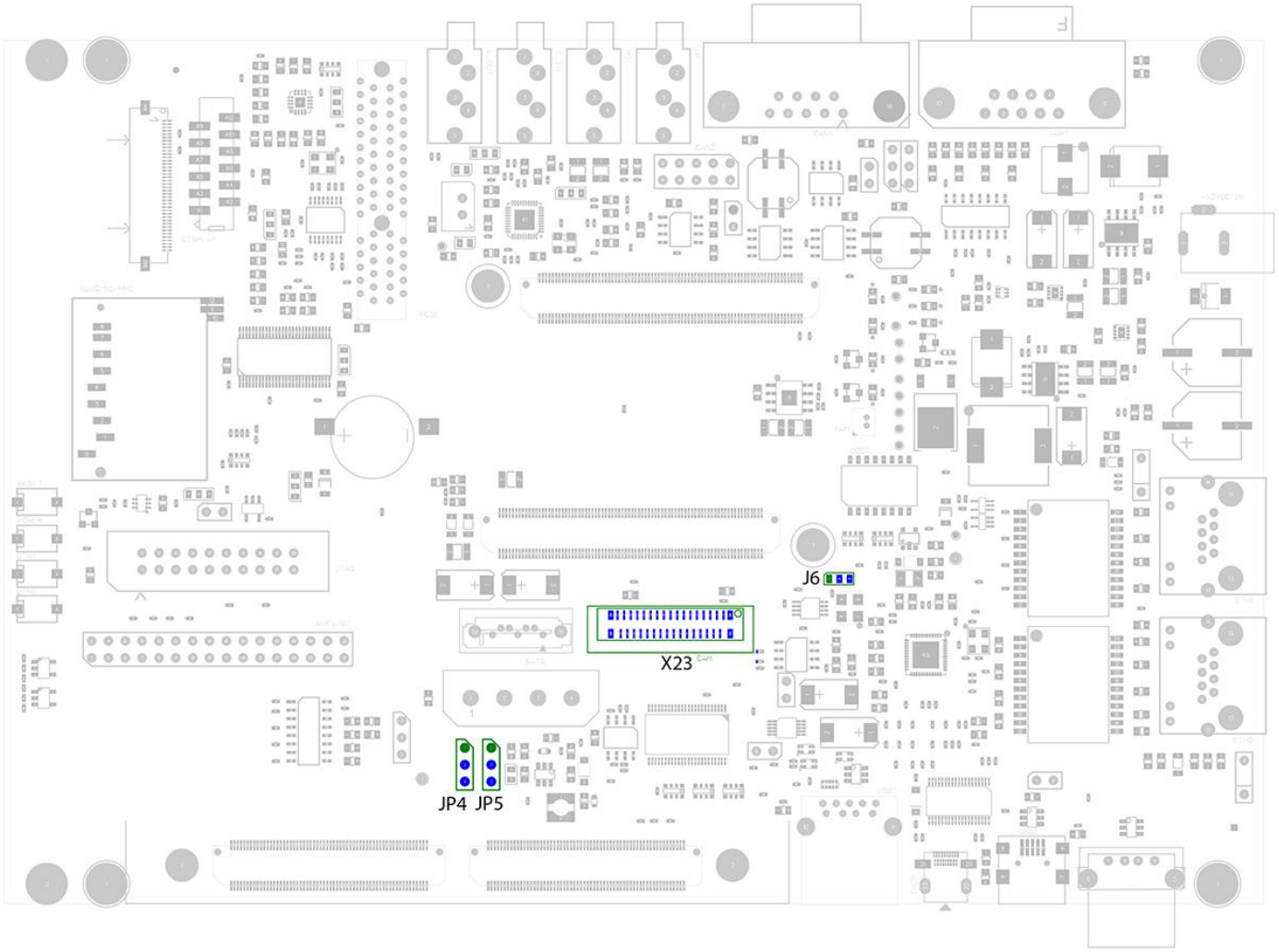

Figure 24. Camera Interface Connectors and Jumpers

The X23 connector provides a connection to PHYTEC Camera devices. The Carrier Board camera circuit only supports an 8-bit camera interface. Please refer to the phyCAM-P manual for details on interfacing with PHYTEC camera devices.

Below is a detailed list of the connectors and jumpers associated with the camera interface.

X23 Provides connection to a PHYTEC supported camera flex cable. See PHYTEC camera offerings for specifics.

JP4 Sets the CAM_CTRL2 signal to control the Camera. Setting the jumper to 1+2 will pull the signal high, while setting it to 2+3 will pull it low. Please see the phyCAM-P manual for further details.

JP5 Sets the CAM_CTRL1 signal to control the Camera. Setting the jumper to 1+2 will pull the signal high, while setting it to 2+3 will pull it low. Please see the phyCAM-P manual for further details.

J6 Selects the reference clock source for camera operation. Setting the jumper to 1+2 will drive the camera clock from an internal processor clock, while setting it to 2+3 will drive the camera clock from an external, fixed 26MHz clock.

29 Audio

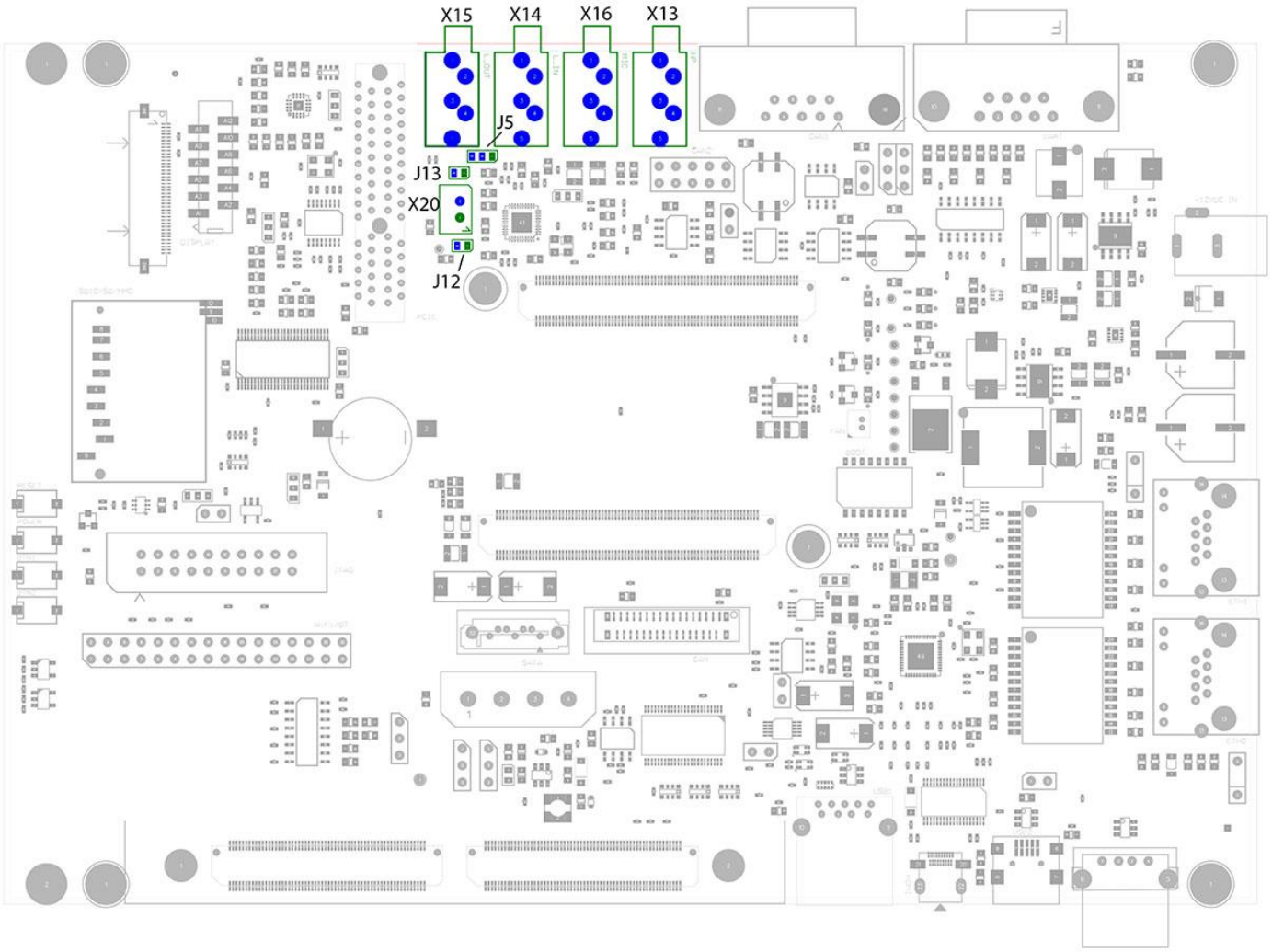

Figure 25. Audio Interface Connectors and Jumpers

The phyCORE-AM57x Carrier Board is designed with a low-power stereo audio codec with integrated mono class-d amplifier at U2. It provides a High Performance Audio DAC and ADC with sample rates from 8 kHz to 96 kHz. It supports a stereo line input, stereo microphone input, stereo line output, stereo headphone output, and direct speaker output.

The audio codec is interfaced to the phyCORE-AM57x via the MCASP1 interface for audio data and the I2C4 interface for codec configuration. The I^2C address for the audio codec is 0x18.

Audio devices can be connected via the 3.5 mm audio jacks at X13, X14, X15, and X16. The X20 pin header allows for direct connection of a Mono Class-D 1W BTL 8 Ohm Speaker. These connectors are described in

Table 34. Description of Audio Connectors

Connector	Input/Output	Description
X13	O	Headset Output
X14	I	Line In
X15	O	Line Out
X16	I	Microphone In
X20	O	Speaker Output

The microphone input and headset output provide a jack detection feature. The jack detection of the microphone input is hardwired, but jack detection of the headset output is enabled by jumper J5. The default position of 2+3 connects the shield contact of the X13 audio jack to the HPCOM output driver of the audio codec. This configuration enables jack detection on the headset output. By connecting the shield contact to ground (setting J5 to 1+2), jack detection is disabled.

Please refer to the audio codec reference manual for additional details on the special interface specification.

30 Cooling Fan Connector

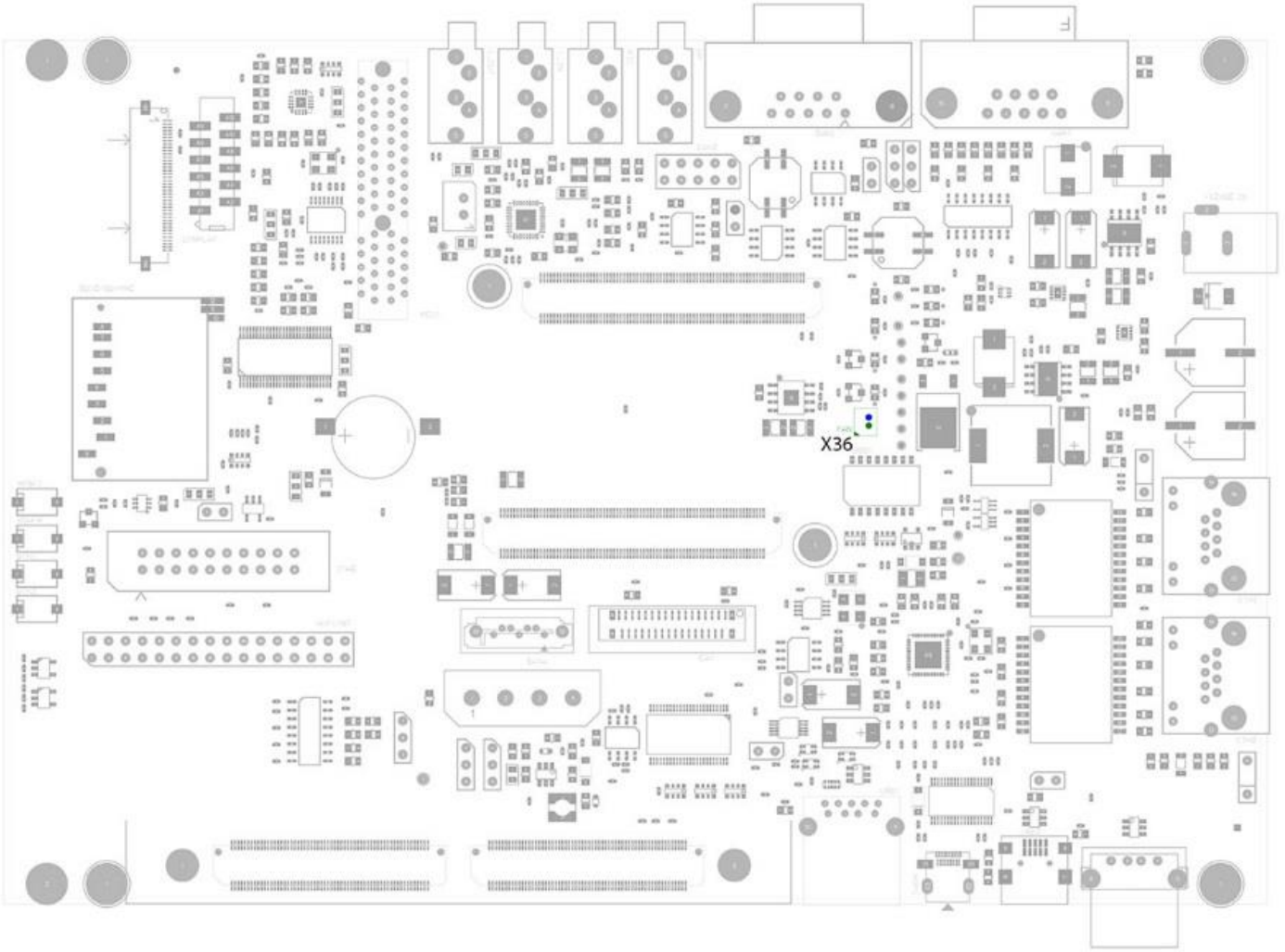

Figure 26. Cooling Fan Connector

The phyCORE-AM57x Carrier Board provides connectivity for a processor cooling fan via a 2 pin connector at X36. The fan is intended to be mounted directly to the processor heat sink for thermal management. The 5V power supplied to the X36 connector is regulated from the VDD_12V0 power rail through a LP3878-ADJ regulator at U12. The regulated 5V output is enabled by driving X_GPIO7_5 high. When X_GPIO7_5 is pulled low, the 5V supplied to the fan connector will be turned off. The enabling of the fan is controlled by a driver that supervises the temperature of the processor, turning on the fan when necessary to prevent the processor from overheating. Table 35 describes the pins of the X36 connector.

Table 35. Cooling Fan Connector (X36) Pin Description

Pin	Description
1	5 V Power Supply
2	Ground

31 User Buttons

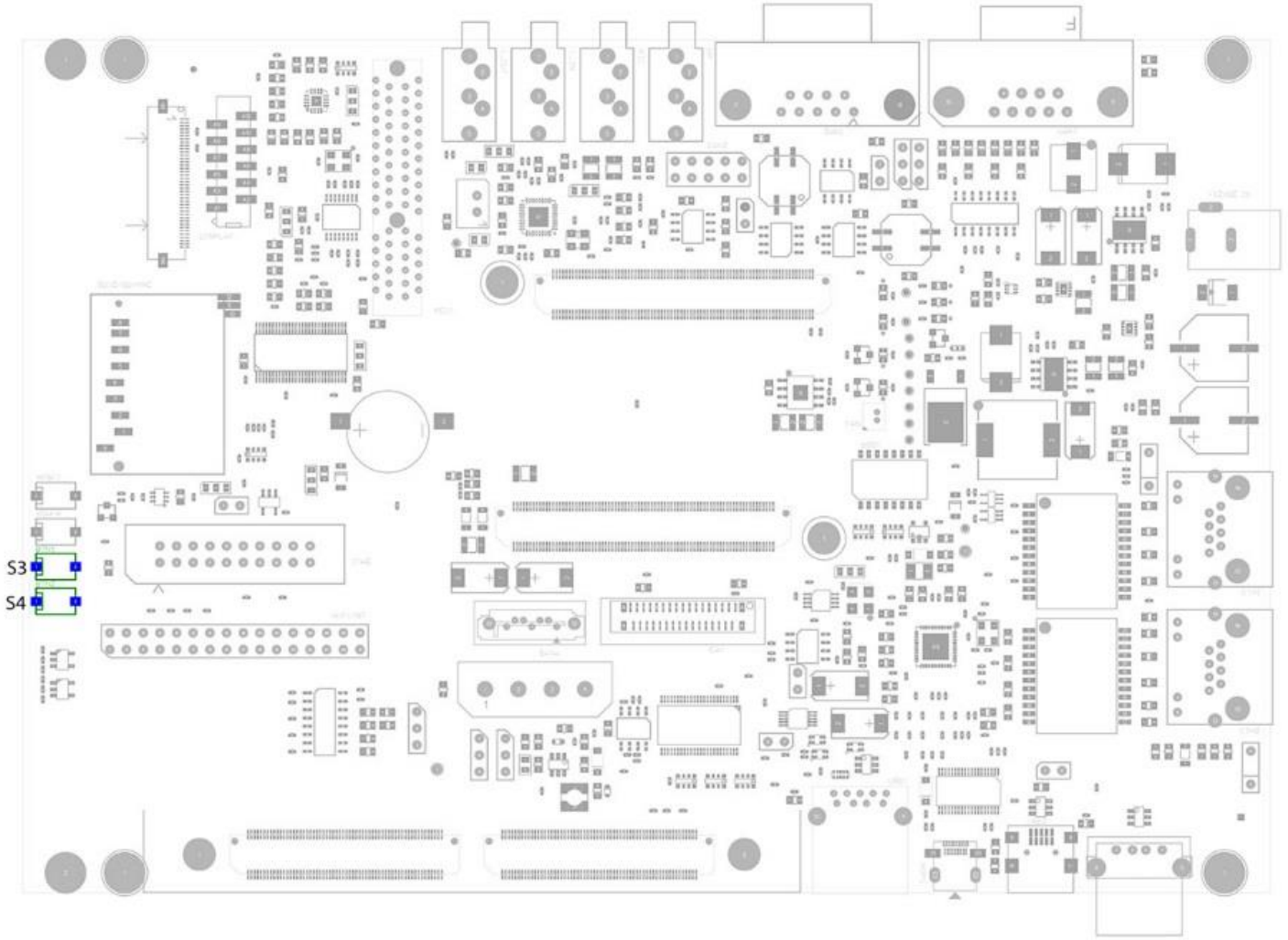

Figure 27. User Buttons

Two user buttons are provided for development. The location of the user buttons is shown in Figure 27. Detailed information regarding the user buttons is listed below.

S3 User button 1 (BTN1). Pressing this button generates a debounced, active-high signal to the processor. Holding this button will drive X_GPIO1_26 high. Releasing this button will pull the X_GPIO1_26 signal low.

S4 User button 2 (BTN2). Pressing this button generates a debounced, active-high signal to the processor. Holding this button will drive X_GPIO1_27 high. Releasing this button will pull the X_GPIO1_27 signal low.

32 User LEDs

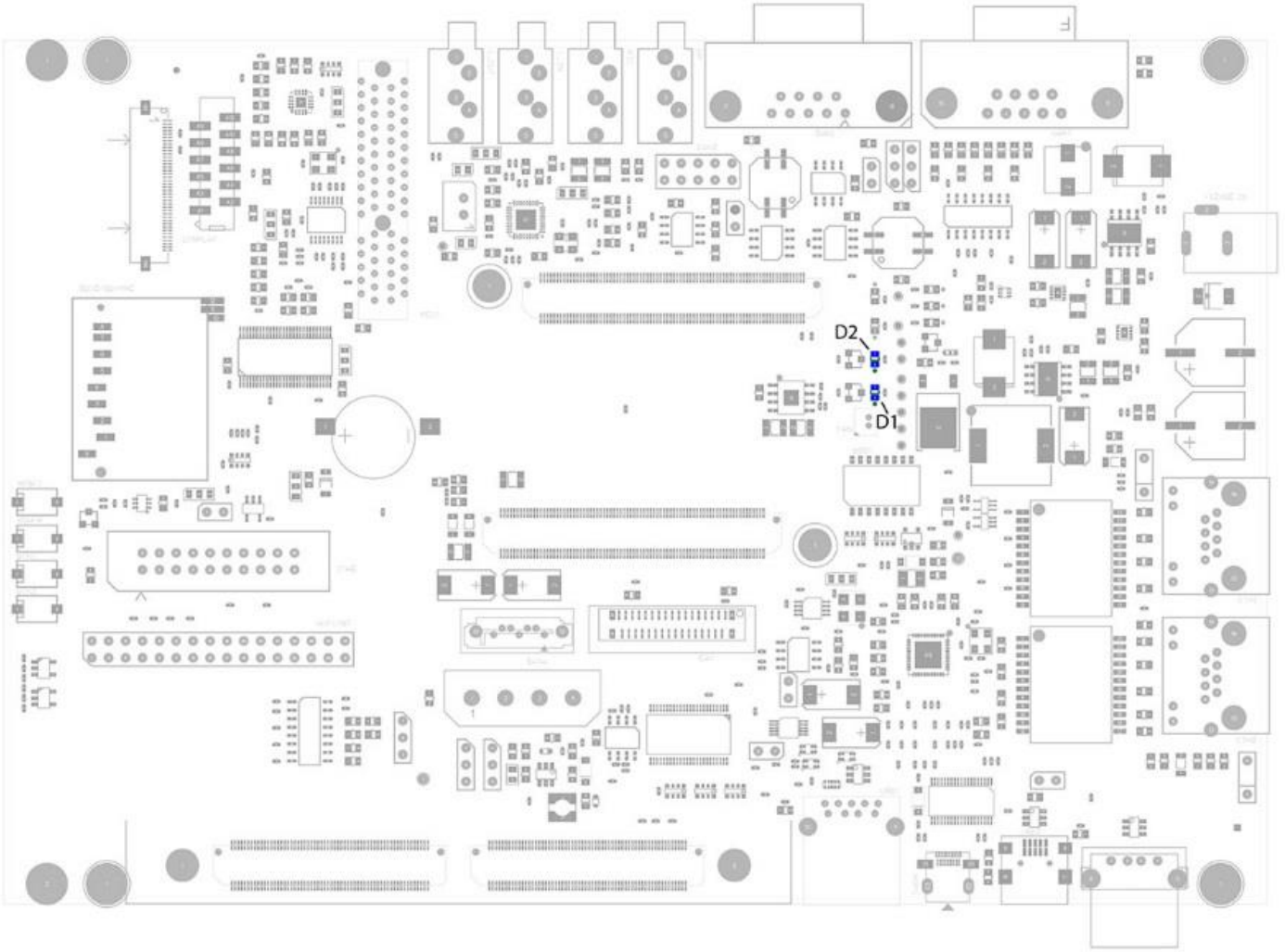

Figure 28. User LEDs

Two user LEDs are provided for development. The location of the user LEDs is shown in Figure 28. A detailed list of the user LEDs is provided below.

D1 Green user LED 1 (LED1). Drive X_GPIO1_28 high to turn this LED on. Drive X_GPIO1_28 low to turn this LED off.

D2 Green user LED 2 (LED2). Drive X_GPIO1_29 high to turn this LED on. Drive X_GPIO1_29 low to turn this LED off.

33 Boot Mode Selection

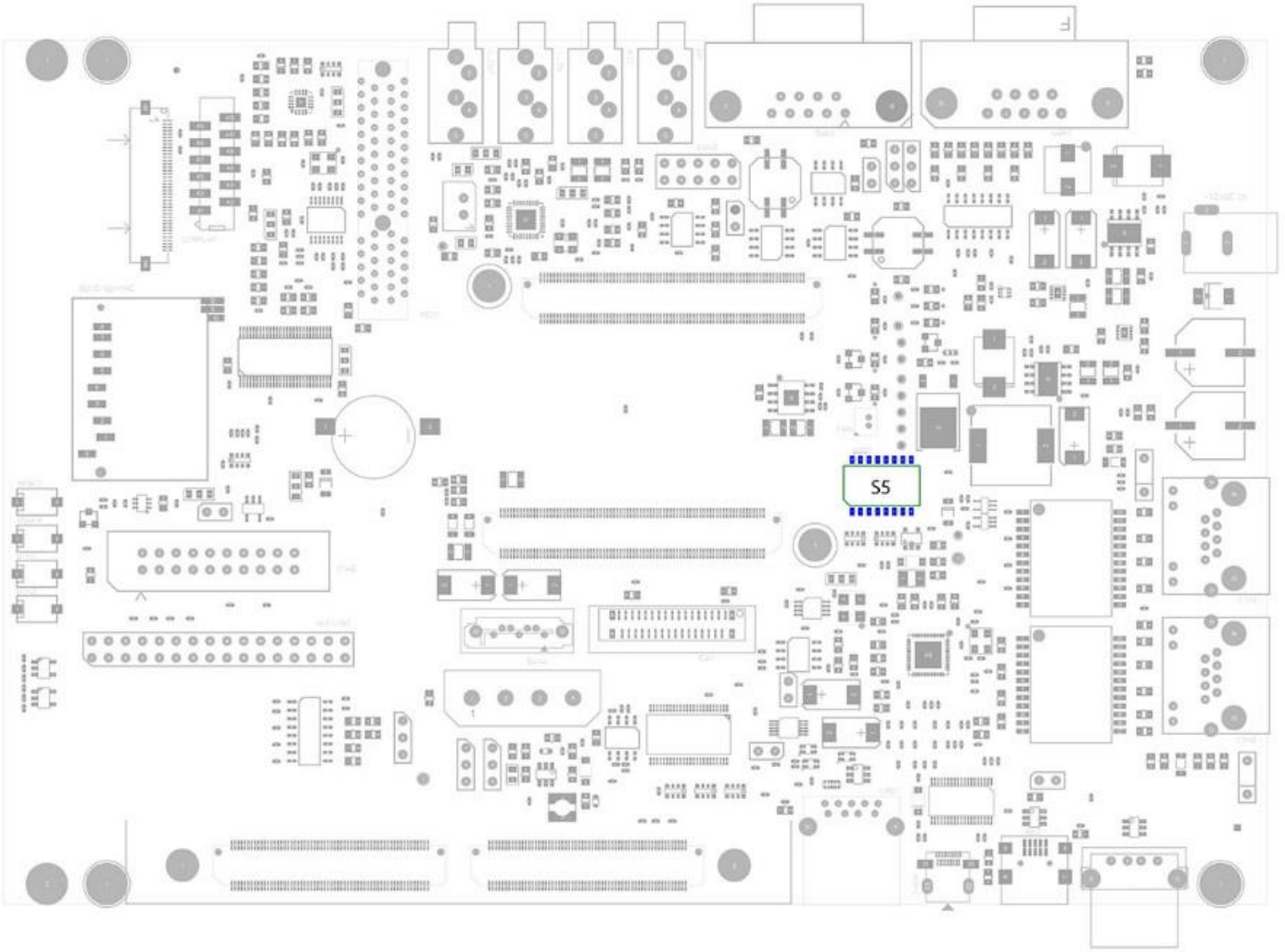

Figure 29. Boot Mode Selection

The boot mode on the phyCORE-AM57x is selected by the configuration of the SYSBOOT[5:0] signals after a power on reset or cold reset. The SYSBOOT[5:4] signals are set to 0b10 on the SOM by default; these signals are not configurable on the Carrier Board. The Carrier Board provides configuration of the SYSBOOT[3:0] signals through the S5 switch. Table 36 describes how the S5 switch settings drive the SYSBOOT[3:0] signals.

Table 36. Boot Switch SYSBOOT[3:0] Settings

Switch	Position	Description
S5-1 / S5-2	**Off/Off**	**SYSBOOT0 is determined by SOM default**
	On/Off	SYSBOOT0 is pulled high
	Off/On	SYSBOOT0 is pulled low
	On/On	Not supported, do NOT set both on at the same time. Unpredictable behavior.
S5-3 / S5-4	**Off/Off**	**SYSBOOT1 is determined by SOM default**
	On/Off	SYSBOOT1 is pulled high

	Off/On	SYSBOOT1 is pulled low
	On/On	Not supported, do NOT set both on at the same time. Unpredictable behavior.
S5-5 / S5-6	**Off/Off**	**SYSBOOT2 is determined by SOM default**
	On/Off	SYSBOOT2 is pulled high
	Off/On	SYSBOOT2 is pulled low
	On/On	Not supported, do NOT set both on at the same time. Unpredictable behavior.
S5-7 / S5-8	**Off/Off**	**SYSBOOT3 is determined by SOM default**
	On/Off	SYSBOOT3 is pulled high
	Off/On	SYSBOOT3 is pulled low
	On/On	Not supported, do NOT set both on at the same time. Unpredictable behavior.

By default S5-1 through S5-8 are set to OFF, so the processor boots based on the default boot configuration set with resistors on the phyCORE-AM57x SOM. The boot configuration resistors on the SOM are set to the default setting of SYSBOOT[3:0] = 0b0010. This configuration sets the boot sequence to SD, eMMC, and then USB. The AM57x will loop through the device order and boot from the first device that has a valid boot image.

Refer to Table 37 below for each of the possible boot configurations supported by the boot mode switch. The permanent booting devices are listed in bold typeface. A permanent booting device is the default memory booting device used after a warm reset if no software booting configuration is programmed.

Table 37. Boot Switch Configuration Description

S5 Switch Configuration	SYSBOOT Signals	Boot Device Order (Memory Preferred Booting)		
(1, 2, 3, 4, 5, 6, 7, 8)	**SYSBOOT[3:0]**	**First**	**Second**	**Third**
(off, on, off, on, off, on, off, on)	0b0000	**eMMC**	USB	-
(on, off, off, on, off, on, off, on)	0b0001	**NAND**	USB	-
(off, on, on, off, off, on, off, on)	0b0010	**SD**	**eMMC**	USB
(on, off, on, off, off, on, off, on)	0b0011	**SATA**	**SD**	USB
(off, on, off, on, on, off, off, on)	0b0100	**XIP**	USB	UART
(on, off, off, on, on, off, off, on)	0b0101	**XIP**	SD	USB
(off, on, on, off, on, off, off, on)	0b0110	**QSPI_1**	SD	USB
(on, off, on, off, on, off, off, on)	0b0111	**QSPI_4**	SD	USB

34 System Reset Button

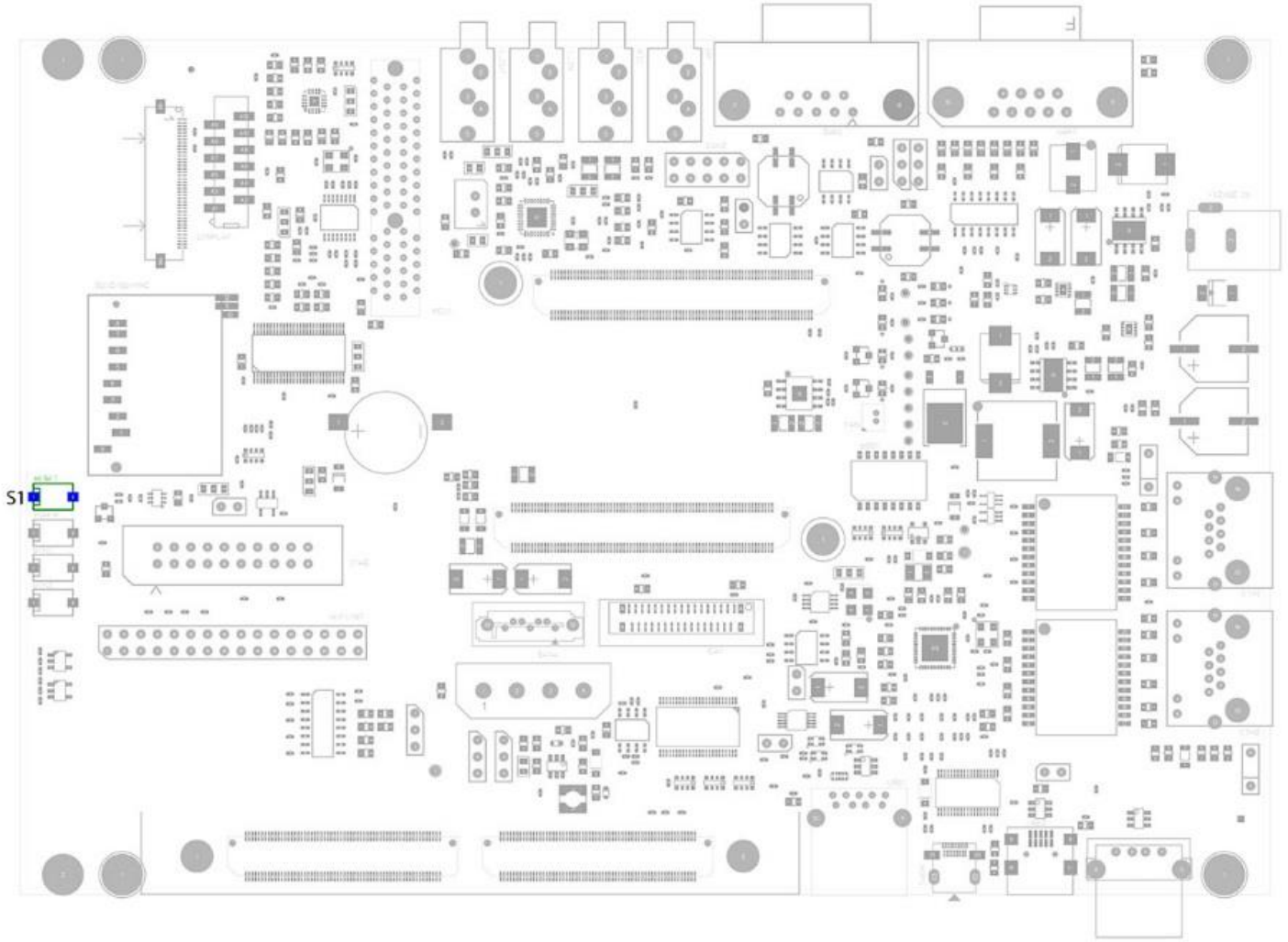

Figure 30. System Reset Button

A system reset button is provided to reset the processor and its peripherals. Refer to Figure 30 for the location of the reset button on the Carrier Board.

Momentarily pressing the S1 button will generate a system reset.

35 GPIO Expansion Connector

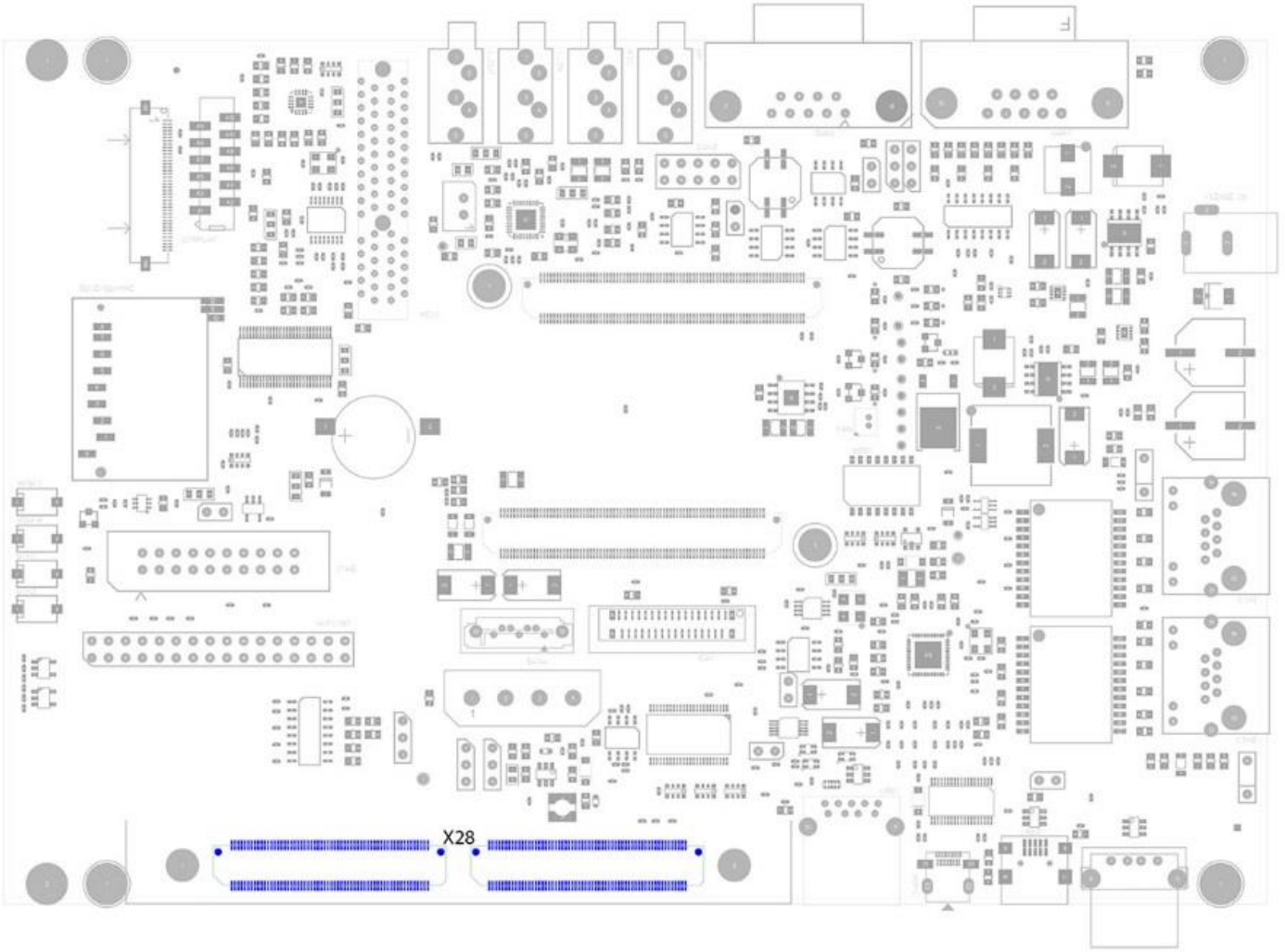

Figure 31. GPIO Expansion Connector

Figure 31 shows the location of the GPIO expansion port connector X28. The connector provides accessibility to many of the phyCORE-AM57x SOM signals. As an accessory, a GPIO Expansion Board (part # PCM-957) is made available through PHYTEC to mate with the X28 connector on the phyCORE-AM57x Carrier Board. This Expansion Board, provides a patch field for easy access to the signals, plus additional board space for testing and prototyping. A summary of the signal mappings between X28 and the SOM mating connectors X1/X3, and the patch field on the GPIO Expansion Board is provided in Part III.

Part III: PCM-957 GPIO Expansion Board

Part III of this manual provides detailed information on the GPIO Expansion Board and how it enables easy access to phyCORE-AM57x System on Module signals.

The information presented in this section is applicable to the 1351.0 PCB revision of the GPIO Expansion Board.

36 Introduction

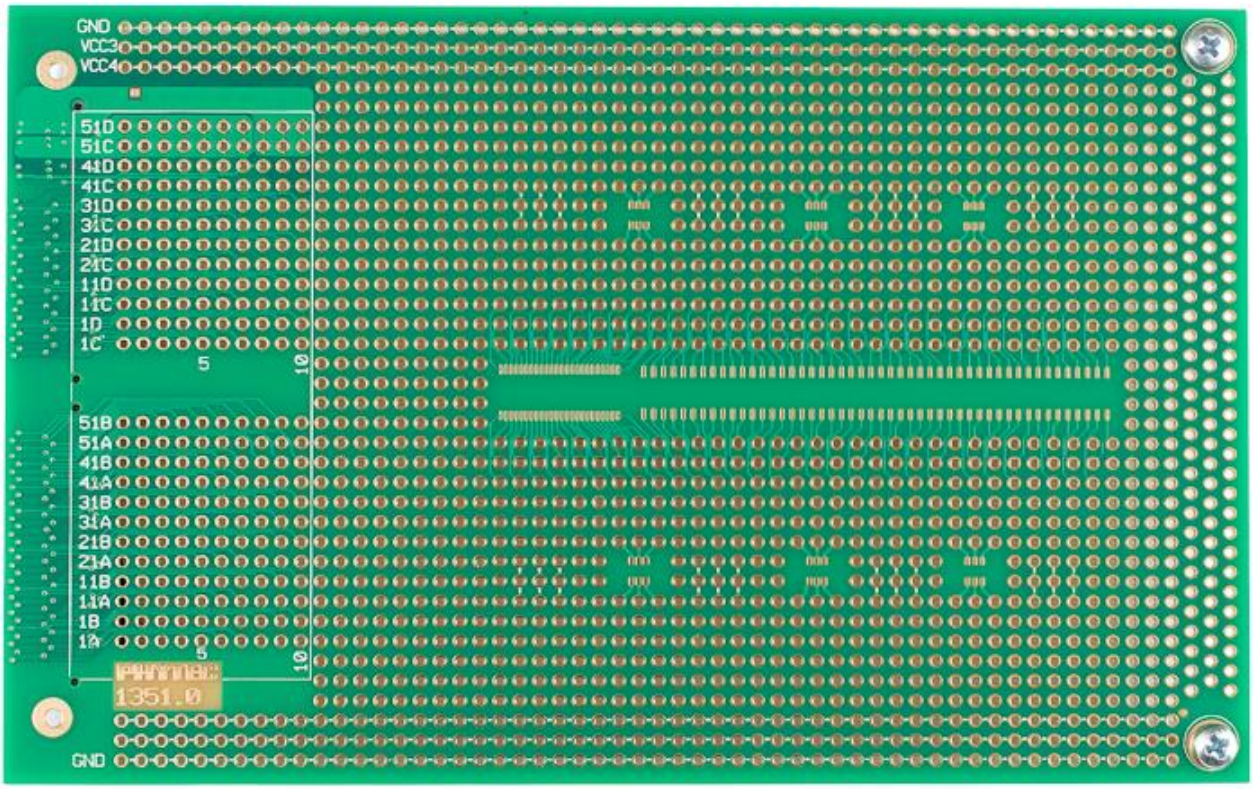

Figure 32. PCM-957/GPIO Expansion Board Patch Field

The optional PCM-957 GPIO Expansion Board add-on provides an easy means of accessing the phyCORE-AM57x SOM signals via a 2.54mm/0.1in spaced patch field. The Expansion Board also provides an empty prototyping area for soldering additional test circuits to interface with the phyCORE-AM57x SOM.

Refer to Figure 32 for the pin numbering scheme on the Expansion Board patch field. The patch field pin numbering is composed of a row letter and a column number: e.g. row 51D contains 51D, 52D, 53D, …, and 60D.

The following chapters and tables, arranged in functional groups, show the relationship between the phyCORE-AM57x signals, the location on the GPIO expansion bus connector, and where to access the signals on the Expansion Board patch field.

37 Power Signal Mapping

Table 38 provides signal mapping for the power signals.

The Signal column specifies the signal name used on the phyCORE-Connector and throughout the AM57x schematics. The SOM column specifies the pin number on the phyCORE-Connector on the SOM. The Expansion Bus/Patch Field column specifies the pin number on the GPIO expansion bus connector on the Carrier Board and the GPIO Expansion Board patch field.

Table 38. Power Signal Mapping

Signal	SOM	Expansion Bus / Patch Field
VDD_12V0	-	58C, 59C, 60C, 58D, 59D, 60D
VDD_5V0	X3-B6	55C, 56C, 57C, 55D, 56D, 57D
VDD_3V3	X3-A1, X3-A2, X3-A3, X3-B1, X3-B2, X3-B3	47C, 48C, 52C, 53C, 54C, 47D, 48D, 52D, 53D, 54D
VDD_1V8	-	49C, 50C, 51C, 49D, 50D, 51D
VBAT	X3-A6	46C
GND	X1 – A4, A9, A14, A19, A24, A29, A34, A39, A44, A49, A54, A59, A64, A69, A74, A79, B2, B7, B12, B17, B22, B27, B32, B37, B42, B47, B52, B57, B62, B67, B72, B77 X3 – A5, A10, A15, A20, A23, A26, A35, A40, A45, A50, A55, A60, A65, A70, A75, A80, B5, B11, B16, B19, B22, B25, B28, B31, B34, B37, B48, B53, B61, B66, B71, B76	1A, 6A, 11A, 16A, 21A, 26A, 31A, 1B, 6B, 12B, 15B, 18B, 20B, 25B, 30B, 1C, 4C, 7C, 10C, 13C, 22C, 27C, 42C, 43C, 44C, 45C, 1D, 7D, 12D, 18D, 23D, 28D, 32D, 42D, 43D, 44D, 45D, 46D

38 Control and Reset Signal Mapping

Table 39 provides signal mapping for various control and reset signals.

The Signal column specifies the signal name used on the phyCORE-Connector and throughout the AM57x schematics. The SOM column specifies the pin number on the phyCORE-Connector on the SOM. The Expansion Bus/Patch Field column specifies the pin number on the GPIO expansion bus connector on the Carrier Board and the GPIO Expansion Board patch field.

Table 39. Control and Reset Signal Mapping

Signal	SOM	Expansion Bus / Patch Field
X_PWRON	X3-A39	28C
X_nRESET_IN	X3-B9	29C
X_EXT_PWR_ON	X3-B10	31C
X_nRESET_OUT	X3-A9	32C

39 GPMC Signal Mapping

Table 40 provides signal mapping for the GPMC signals.

The Signal column specifies the signal name used on the phyCORE-Connector and throughout the AM57x schematics. The SOM column specifies the pin number on the phyCORE-Connector on the SOM. The Expansion Bus/Patch Field column specifies the pin number on the GPIO expansion bus connector on the Carrier Board and the GPIO Expansion Board patch field.

Table 40. GPMC Signal Mapping

Signal	SOM	Expansion Bus / Patch Field
X_GPMC_AD0/SYSBOOT0	X1-B13	2A
X_GPMC_AD1/SYSBOOT1	X1-B14	3A
X_GPMC_AD2/SYSBOOT2	X1-B15	4A
X_GPMC_AD3/SYSBOOT3	X1-B16	5A
X_GPMC_AD4/SYSBOOT4	X1-A10	7A
X_GPMC_AD5/SYSBOOT5	X1-A11	8A
X_GPMC_AD6/SYSBOOT6	X1-A12	9A
X_GPMC_AD7/SYSBOOT7	X1-A13	10A
X_GPMC_AD8/SYSBOOT8	X1-B18	12A
X_GPMC_AD9/SYSBOOT9	X1-B19	13A
X_GPMC_AD10/SYSBOOT10	X1-B20	14A
X_GPMC_AD11/SYSBOOT11	X1-B21	15A
X_GPMC_AD12/SYSBOOT12	X1-A15	17A
X_GPMC_AD13/SYSBOOT13	X1-A16	18A
X_GPMC_AD14/SYSBOOT14	X1-A17	19A
X_GPMC_AD15/SYSBOOT15	X1-A18	20A
X_GPMC_ADVN_ALE	X1-A20	22A
X_GPMC_OEN_REN	X1-A21	23A
X_GPMC_WAIT0	X1-A22	24A
X_GPMC_WEN	X1-A23	25A
X_GPMC_BEN0	X1-B8	27A
X_GPMC_BEN1	X1-B9	28A
X_GPMC_CLK	X1-B10	29A
X_GPMC_CS0	X1-B11	30A

40 GPIO Signal Mapping

Table 41 provides signal mapping for the GPIO signals.

The Signal column specifies the signal name used on the phyCORE-Connector and throughout the AM57x schematics. The SOM column specifies the pin number on the phyCORE-Connector on the SOM. The Expansion Bus/Patch Field column specifies the pin number on the GPIO expansion bus connector on the Carrier Board and the GPIO Expansion Board patch field.

Table 41. GPIO Signal Mapping

Signal	SOM	Expansion Bus / Patch Field
X_GPIO1_26	X1-A50	19D
X_GPIO1_27	X1-A51	20D
X_GPIO1_28	X1-A52	21D
X_GPIO1_29	X1-A53	22D
X_GPIO8_20	X1-A60	24D
X_GPIO8_21	X1-A61	25D
X_GPIO8_22	X1-A62	26D
X_GPIO8_23	X1-A63	27D
X_GPIO4_19	X1-A47	29D
X_GPIO2_2	X1-A55	30D
X_GPIO6_4	X1-A57	31D
X_GPIO8_2	X1-A58	33D
X_GPIO8_3	X1-B53	34D
X_GPIO8_4	X1-B54	35D
X_GPIO8_5	X1-B55	36D
X_GPIO8_6	X1-B56	37D
X_GPIO8_7	X1-B58	38D
X_GPIO7_5	X1-A56	39D
X_GPIO4_20	X1-B59	23C
X_GPIO4_21	X1-B60	24C
X_GPIO4_22	X1-B61	25C
X_GPIO4_23	X3-A49	26C
X_GPIO4_3	X1-A46	2B

41 VIN3A (Display) Signal Mapping

Table 42 provides signal mapping for the VIN3A signals.

The Signal column specifies the signal name used on the phyCORE-Connector and throughout the AM57x schematics. The SOM column specifies the pin number on the phyCORE-Connector on the SOM. The Expansion Bus/Patch Field column specifies the pin number on the GPIO expansion bus connector on the Carrier Board and the GPIO Expansion Board patch field.

Table 42. VIN3A Signal Mapping

Signal	SOM	Expansion Bus / Patch Field
X_VIN3A_D8	X1-B68	21B
X_VIN3A_D9	X1-B69	22B
X_VIN3A_D10	X1-B70	23B
X_VIN3A_D11	X1-B71	24B
X_VIN3A_D12	X1-A70	26B
X_VIN3A_D13	X1-A71	27B
X_VIN3A_D14	X1-A72	28B
X_VIN3A_D15	X1-A73	29B

42 SPI Signal Mapping

Table 43 provides signal mapping for the SPI signals.

The Signal column specifies the signal name used on the phyCORE-Connector and throughout the AM57x schematics. The SOM column specifies the pin number on the phyCORE-Connector on the SOM. The Expansion Bus/Patch Field column specifies the pin number on the GPIO expansion bus connector on the Carrier Board and the GPIO Expansion Board patch field.

Table 43. SPI Signal Mapping

Signal	SOM	Expansion Bus / Patch Field
X_SPI1_nCS0	X3-A33	2D
X_SPI1_nCS1	X3-A34	3D
X_SPI1_DIN	X3-A36	4D
X_SPI1_DOUT	X3-A37	5D
X_SPI1_CLK	X3-A38	6D
SPI2_nCS0	X1-B48	8D
SPI2_DIN	X1-B49	9D
X_SPI2_DOUT	X1-B50	10D
X_SPI2_CLK	X1-B51	11D
X_SPI3_nCS0	X1-A40	13D
X_SPI3_nCS1	X1-B41	14D
X_SPI3_DIN	X1-A42	15D
X_SPI3_DO	X1-A43	16D
X_SPI3_CLK	X1-A41	17D

43 I²C Signal Mapping

Table 44 provides signal mapping for the I²C signals.

The Signal column specifies the signal name used on the phyCORE-Connector and throughout the AM57x schematics. The SOM column specifies the pin number on the phyCORE-Connector on the SOM. The Expansion Bus/Patch Field column specifies the pin number on the GPIO expansion bus connector on the Carrier Board and the GPIO Expansion Board patch field.

Table 44. I²C Signal Mapping

Signal	SOM	Expansion Bus / Patch Field
X_I2C1_SCL	X3-A16	2C
X_I2C1_SDA	X3-A17	3C
X_I2C3_SCL	X3-A32	5C
X_I2C3_SDA	X3-A31	6C
X_I2C4_SCL	X1-A37	8C
X_I2C4_SDA	X1-A38	9C
X_I2C5_SCL	X1-B39	11C
X_I2C5_SDA	X1-B38	12C

44 QSPI1 Signal Mapping

Table 45 provides signal mapping for the QSPI1 signals.

The Signal column specifies the signal name used on the phyCORE-Connector and throughout the AM57x schematics. The SOM column specifies the pin number on the phyCORE-Connector on the SOM. The Expansion Bus/Patch Field column specifies the pin number on the GPIO expansion bus connector on the Carrier Board and the GPIO Expansion Board patch field.

Table 45. QSPI1 Signal Mapping

Signal	SOM	Expansion Bus / Patch Field
X_QSPI1_RTCLK	X1-A3	14C
X_QSPI1_D3	X1-A5	15C
X_QSPI1_D2	X1-A6	16C
X_QSPI1_D1	X1-A7	17C
X_QSPI1_D0	X1-A8	18C
X_QSPI1_SCLK	X1-B4	19C
X_QSPI1_CS0	X1-B5	20C
X_QSPI1_CS1	X1-B6	21C

45 KBD Signal Mapping

Table 46 provides signal mapping for the KBD signals.

The Signal column specifies the signal name used on the phyCORE-Connector and throughout the AM57x schematics. The SOM column specifies the pin number on the phyCORE-Connector on the SOM. The Expansion Bus/Patch Field column specifies the pin number on the GPIO expansion bus connector on the Carrier Board and the GPIO Expansion Board patch field.

Table 46. KBD Signal Mapping

Signal	SOM	Expansion Bus / Patch Field
X_KBD_COL0	X1-B35	3B
X_KBD_COL1	X1-B36	4B
X_KBD_COL2	X1-A35	5B
X_KBD_COL3	X1-A36	7B
X_KBD_ROW0	X1-B33	8B
X_KBD_ROW1	X1-B34	9B
X_KBD_ROW2	X1-A32	10B
X_KBD_ROW3	X1-A33	11B

46 PWM/Clock/Wakeup Signal Mapping

Table 47 provides signal mapping for the PWM/Clock/Wakeup signals.

The Signal column specifies the signal name used on the phyCORE-Connector and throughout the AM57x schematics. The SOM column specifies the pin number on the phyCORE-Connector on the SOM. The Expansion Bus/Patch Field column specifies the pin number on the GPIO expansion bus connector on the Carrier Board and the GPIO Expansion Board patch field.

Table 47. PWM/Clock/Wakeup Signal Mapping

Signal	SOM	Expansion Bus / Patch Field
X_EHRPWM1B	X1-B40	19B
X_WAKEUP2	X3-A48	13B
X_WAKEUP3	X1-A45	14B
X_XREF_CLK2	X3-A47	16B
X_XREF_CLK3	X1-A48	17B

Revision History

Table 48 Document Revision History

Date	Version Number	Changes in this Manual
2015/10/01	L-815e_0	Preliminary Release
2017/06/16	L-815e_1	Updated TBD power consumption values in Chapter 3 Updated TBD technical specifications in Table 14-15 Updated description for SYSBOOT[9:8] in Table 6 Added shunt resistor values to Section 16.5
2018/01/02	L-815e_2	Added descriptions for jumpers J6 and JP7