phyCORE-OMAP44xx

Hardware Manual

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Conventions, Abbreviations and Acronyms

This hardware manual describes the PCM-049 System on Module in the following referred to as phyCORE-OMAP44xx. The manual specifies the phyCORE-OMAP44xx's design and function. Precise specifications for the Texas Instruments OMAP44xx microcontrollers can be found in the enclosed microcontroller Data Sheet/User's Manual.

Conventions

The conventions used in this manual are as follows:

- Signals that are preceded by a "n", "/", or "#" character (e.g.: nRD, /RD, or #RD), or that have a dash on top of the signal name (e.g.: $\overline{RD}$) are designated as active low signals. That is, their active state is when they are driven low, or are driving low.
- A "0" indicates a logic zero or low-level signal, while a "1" represents a logic one or high-level signal.
- The hex-numbers given for addresses of I^2C devices always represent the 7 MSB of the address byte. The correct value of the LSB which depends on the desired command (read (1), or write (0)) must be added to get the complete address byte. E.g. given address in this manual 0x41 => complete address byte = 0x83 to read from the device and 0x82 to write to the device
  Tables which describe jumper settings show the default position in **bold, blue text**.
- Text in blue italic indicates a hyperlink within, or external to the document. Click these links to quickly jump to the applicable URL, part, chapter, table, or figure.
- References made to the phyCORE-Connector always refer to the high density Samtec connector on the undersides of the phyCORE-OMAP44xx System on Module.

Abbreviations and Acronyms

Many acronyms and abbreviations are used throughout this manual. Use the table below to navigate unfamiliar terms used in this document.

Abbreviation	Definition
BSP	Board Support Package (Software delivered with the Development Kit including an operating system (Windows, or Linux) preinstalled on the module and Development Tools).
CB	Carrier Board; used in reference to the phyCORE-OMAP44xx Development Kit Carrier Board.
DFF	D flip-flop
EMB	External memory bus
EMI	Electromagnetic interference
GPI	General purpose input
GPIO	General purpose input and output
GPO	General purpose output
IRAM	Internal RAM; the internal static RAM on the Texas Instruments OMAP44xx microcontroller.
J	Solder jumper; these types of jumpers require solder equipment to remove and place.
JP	Solderless jumper; these types of jumpers can be removed and placed by hand with no special tools.
PCB	Printed circuit board

Table 1: Abbreviations and Acronyms used in this Manual

Abbreviation	Definition
PDI	PHYTEC Display Interface; defined to connect PHYTEC display adapter boards, or custom adapters.
PEB	PHYTEC Extension Board
PMIC	Power management IC
PoE	Power over Ethernet
PoP	Package on Package
POR	Power-on reset
RTC	Real-time clock
SMT	Surface mount technology
SOM	System on Module; used in reference to the PCM-049 / phyCORE-OMAP44xx System on Module.
Sx	User button Sx (e.g. S1, S2, etc.) used in reference to the available user buttons, or DIP-Switches on the carrier board.
Sx_y	Switch y of DIP-Switch Sx; used in reference to the DIP-Switch on the carrier board.
VBAT	SOM standby voltage input

Table 1: Abbreviations and Acronyms used in this Manual

Note:

The BSP delivered with the phyCORE-OMAP44xx usually includes drivers and/or software for controlling all components such as interfaces, memory, etc.. Therefore programming close to hardware at register level is not necessary in most cases. For this reason, this manual contains no detailed description of the controller's registers, or information relevant for software development. Please refer to the OMAP44xx Reference Manual, if such information is needed to connect customer designed applications.

Preface

As a member of PHYTEC's phyCORE product family the phyCORE-OMAP44xx is one of a series of PHYTEC System on Modules (SOMs) that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports a variety of 8-/16- and 32-bit controllers in two ways:

1. as the basis for Rapid Development Kits which serve as a reference and evaluation platform
2. as insert-ready, fully functional phyCORE OEM modules, which can be embedded directly into the user's peripheral hardware design.

Implementation of an OEM-able SOM subassembly as the "core" of your embedded design allows you to focus on hardware peripherals and firmware without expending resources to "re-invent" microcontroller circuitry. Furthermore, much of the value of the phyCORE module lies in its layout and test.

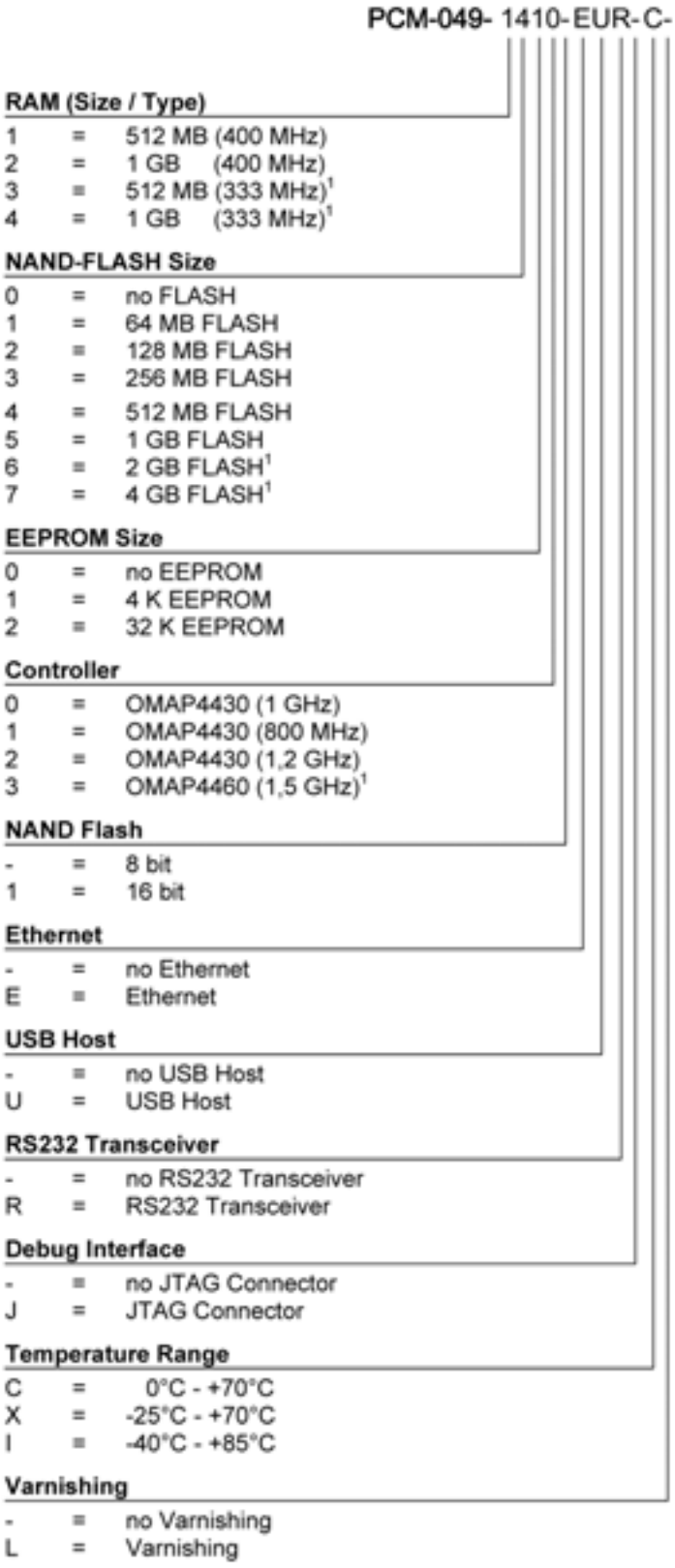
Production-ready Board Support Packages (BSPs) and Design Services for our hardware will further reduce your development time and risk and allow you to focus on your product expertise. Take advantage of PHYTEC products to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks. With this new innovative full system solution you will be able to bring your new ideas to market in the most timely and cost-efficient manner.

For more information go to:

http://www.phytec.de/de/leistungen/entwicklungsunterstuetzung.html or
http://www.phytec.eu/europe/oem-integration/evaluation-start-up.html

Ordering Information

The part numbering of the phyCORE has the following structur



In order to receive product specific information on changes and updates in the best way also in the future, we recommend to register at

http://www.phytec.de/de/support/registrierung.html or
http://www.phytec.eu/europe/support/registration.html

For technical support and additional information concerning your product, please visit the support section of our web site which provides product specific information, such as errata sheets, application notes, FAQs, etc.

http://www.phytec.de/de/support/faq/faq-phycore-omap44xx.html or
http://www.phytec.eu/europe/support/faq/faq-phycore-omap44xx.html

Declaration of Electro Magnetic Conformity of the PHYTEC phyCORE-OMAP44xx

PHYTEC System on Modules (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution:

PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header Rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header Row connectors, power connector and serial interface to a host-PC).

Caution:

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

Important information on POH (power-on hours) for the OMAP44xx

The OMAP44xx is a typical state-of-the-art microcontroller. It packs enormous processing power into a small space. The space requirements of the circuitry are optimized through the use of POP (package-on-package) memory.

This generation of processors lets you benefit from the latest developments in consumer electronics. These modern controllers are used in smartphones and other mobile devices with high performance requirements. The high-volume production brings down your costs, and you have the advantage of sophisticated, high-density architectures.

Precisely because of their compact dimensions and high level of integration, these controllers are subjected to elevated thermal loads. Their design does not permit continuous operation over many years when all internal units are working at 100%.

The total period during which a controller can operate reliably depends on the thermal load. The term used for this period is POH (power-on hours). It refers to the (minimum) service life.

The POH value of a controller varies according to its use. The tables show an analysis of typical consumer applications (smartphone). For these scenarios the lifetimes are 5 years and 7 years.

The POH value depends to a high degree on how the different cores of the controller are used. There is no simple formula for calculating POH values.

However, it is important to pay close attention to POH and plan your use of the controller in accordance with the technical conditions.

We will assist you in this and show you how to successfully use controllers of this kind in your industrial applications.

We can optimize software so that it automatically adjusts the clock frequency and voltage to the processing requirements of the application. In addition, we can send your typical application to Texas Instruments for calculation of the POH value for your particular scenario. The more accurate your description in terms of duration and use pattern, the more reliable the results of this calculation.

We will be glad to answer any questions. Please contact our sales team.

Generic Example (operating time 5 years)[1] [4][5]

OMAP4430 Device	Case	Voltage (V)[3]	Maximum Frequency (MHz)			T_J (°C)[2]	POH (h)
			MPU	IVA	CORE		
OMAP4430 – 1000 MHz	43830 Hours (5 years)	< OPPNT	1000	266	400	93	2641
		< OPP100	600	266	400	48	1377
		< OPP50	300	133	200	18	6467
		< OPP50	98	133	200	10	1381
		Retention	–	–	–	25	31045
				Total			43830

The above power on hour use case is based on a 5 year lifetime use profile for smartphones and other mobile devices. Other use cases can apply for other devices in other fields and for a lifetime up to 5 years.

1. For other use cases, contact TI for evaluation to determine if they can be supported.
2. T_J is the average operating junction temperature.
3. See the operating condition addendum for values.
4. With SmartReflex™ enabled.
5. The power on hour (POH) analysis is based on a typical use case with the following parameters:
   - The percentage (%) of activity by day for each application of the use case
   - The MPU, IVA and CORE voltages and frequencies by application (ideally the use of vdd_mpu, vdd_iva_audio, or vdd_core OPPs)
   - The average operating junction temperature
   - SmartReflex™ (power optimization techniques) use or not

Practical example of mobile applications (operating time 7 years)

Phone use profile		ETR (typical – with end-product ambient temperature at 25°C)			Worst case profile (with end-product ambient temperature up to 40°C)		
Mode number	Mode name	Lifetime % active	€PDH	Tj [°C]	Lifetime % active	€PDH	Tj [°C]
1	Cellular or VOIP Voice	5.60 %	2.41	45	5.60 %	2.41	60
2	Browsing using HSDPA or WLAN – Active phase (note 4)	1.20 %	0.77	80	1.90 %	1.13	100
2.1a	Browsing reading phase	3.80 %	1.75	55	4.40 %	2.66	90
3	Video playback (HD 16:9 > 30 fs)	1.20 %	0.75	75	3.10 %	1.83	95
3.1a	Stereo Video playback (HD 16:9 > 24 fs)	1.20 %	0.75	80	3.10 %	1.92	95
4	Video recording (HD 16:9 > 30 fs)	0.40 %	0.26	80	1.00 %	0.64	95
4.1a	Stereo Video recording (HD 16:9 > 30 fs)	0.40 %	0.26	85	1.00 %	0.64	100
5	Music playback	4.20 %	2.50	40	6.20 %	2.83	45
6	Messaging (SMS, email)	6.20 %	3.83	55	6.20 %	3.83	55
7	Navigation (A(G)PS)	0.80 %	0.66	75	0.80 %	0.66	90
8	Gaming (Online+local) (assume max thermal test case)	2.30 %	3	102	6.30 %	8.11	117
9	Standby	63.60 %	30.21	29	49.60 %	30.44	40
10	Still Image Capture	0.10 %	0.09	50	0.10 %	0.09	90
11	Fiddling (UI + other apps) + File Dn/Up	8.50 %	5.11	48	8.50 %	5.11	90
	Total	100.00 %	61.32		100.00 %	61.32	

1 Part I: PCM-049/phyCORE-OMAP44xx System on Module

Part 1 of this 2 part manual provides detailed information on the phyCORE-OMAP44xx System on Module (SOM) designed for custom integration into customer applications. The information in the following chapters is applicable to the 1347.1 PCB revision of the phyCORE-OMAP44xx SOM.

1.1 Introduction

The phyCORE-OMAP44xx belongs to PHYTEC's phyCORE System on Module family. The phyCORE SOMs represent the continuous development of PHYTEC System on Module technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

As independent research indicates that approximately 70% of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments, the phyCORE board design features an increased pin package. The increased pin package allows dedication of approximately 20% of all connector pins on the phyCORE boards to ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards even in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD components and laser-drilled microvias are used on the boards, providing phyCORE users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCORE-OMAP44xx is a subminiature (51 mm x 41 mm) insert-ready System on Module populated with the Texas Instruments OMAP44xx microcontroller. Its universal design enables its insertion in a wide range of embedded applications. All controller signals and ports extend from the controller to high-density pitch (0.5 mm) connectors aligning two sides of the board, allowing it to be plugged like a "big chip" into a target application.

Precise specifications for the controller populating the board can be found in the applicable controller Reference Manual or datasheet. The descriptions in this manual are based on the Texas Instruments OMAP44xx. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyCORE-OMAP44xx.

The phyCORE-OMAP44xx offers the following features:

- Insert-ready, sub-miniature (51 mm x 41 mm) System on Module (SOM) subassembly in low EMI design, achieved through advanced SMD technology
- Populated with the Texas Instruments OMAP44xx microcontroller (BGA547 packaging and package-on-package (PoP) memory)
- Improved interference safety achieved through multi-layer PCB technology and dedicated ground pins
- Controller signals and ports extend to two 120-pin high-density (0.5 mm) Samtec connectors aligning two sides of the board, enabling it to be plugged like a "big chip" into target application
- Max. 1.2 GHz core clock frequency
- Boot from NAND Flash
- 64 MB (up to 4 GB) on-board NAND Flash[1]
- PoP memory device with 512 MB (up to 1 GB) LP DDR2 SDRAM[1]
- 4 kB (up to 32 kB) I^2C EEPROM[1]
- Serial interface with 4 lines (RS-232) allowing simple hardware handshake[1]
- Three serial interfaces (TTL). One with 4 lines allowing simple hardware handshake

1. Please refer to the order options described in the Preface, or contact PHYTEC for more information about additional module configurations.

- High-Speed USB OTG interface
- High-Speed USB HOST interface provided by on-board USB transceiver[1]
- Full-Speed USB interface (USBC1) brought out to the phyCORE-Connector as additional USB-Host interface[1]
- 10/100 MBit Ethernet interface with HP Auto MDIX support[1]
- Single supply voltage of 3.3 V (max. 900 mA)
- All controller required supplies generated on board
- On-board power management IC with integrated RTC
- 24-bit parallel LCD interface
- HDMI interface
- 5 channel DSI LCD interface
- Support of standard 20 pin debug interface through JTAG connector
- Three I^2C interfaces
- One SPI interfaces
- Two SD/MMC card interfaces with DMA
- I^2S interface
- Multichannel audio serial interface (McASP)
- Keyboard interface with up to 6 rows and 6 columns
- Up to two LVDS camera interfaces
- Two user programmable LEDs
- Four dedicated GPIO/IRQ ports (additionally nearly all pins can be alternatively used as GPIOs)
- Industrial temperature range (-40°C...+85°C)

Caution:

Samtec connectors guarantee optimal connection and proper insertion of the phyCORE-OMAP44xx. Please make sure that the phyCORE-OMAP44xx is fully plugged into the matting connectors of the carrier board. Otherwise individual signals may have a bad, or no contact.

1. USBC1 is meant for USB Inter-Chip connectivity only. Please refer to the OMAP4430 Reference Manual for more information.

1.1.1 Block Diagram

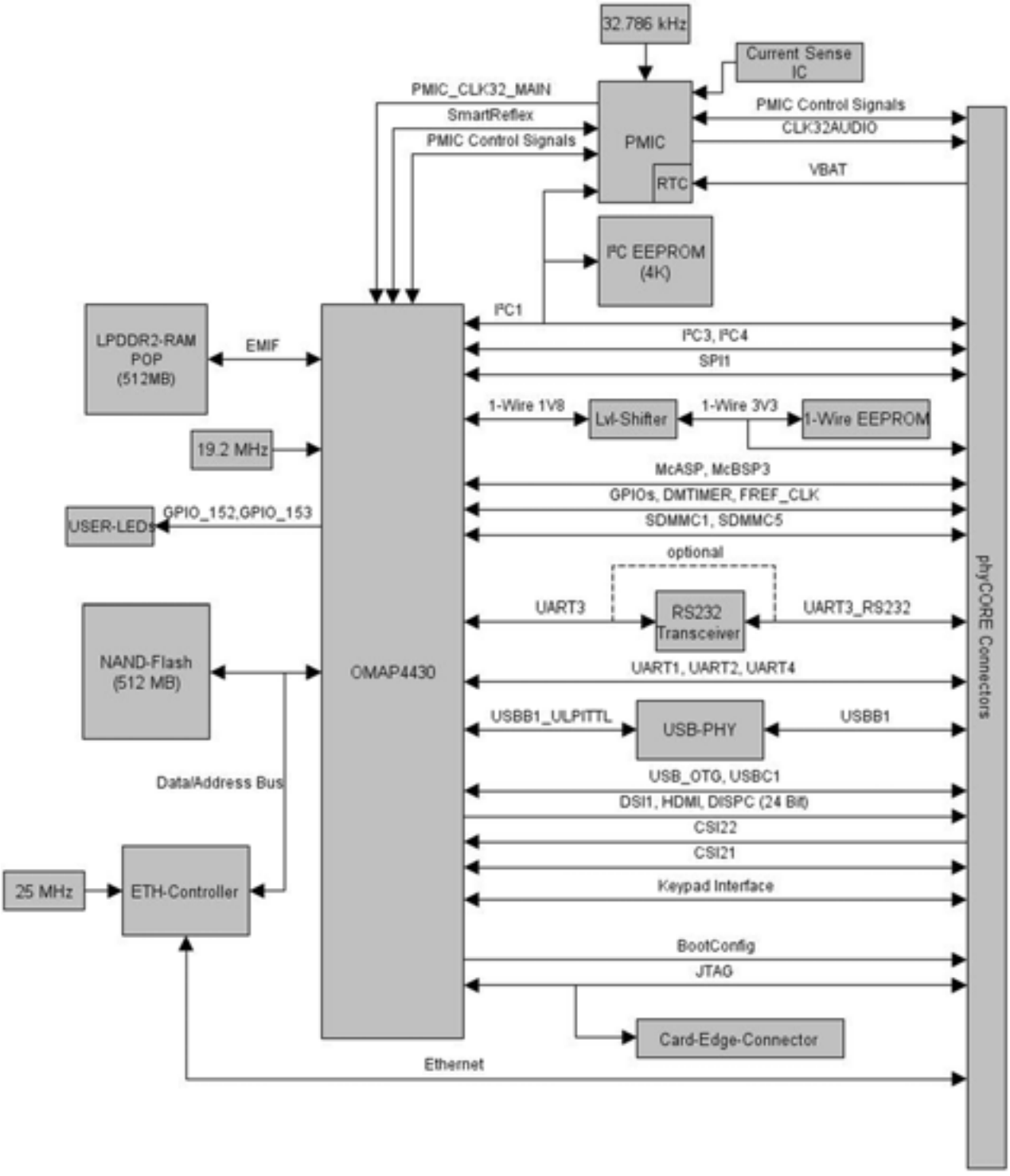


Figure 1: Block Diagram of the phyCORE-OMAP44xx

1.1.2 View of the phyCORE-OMAP44xx

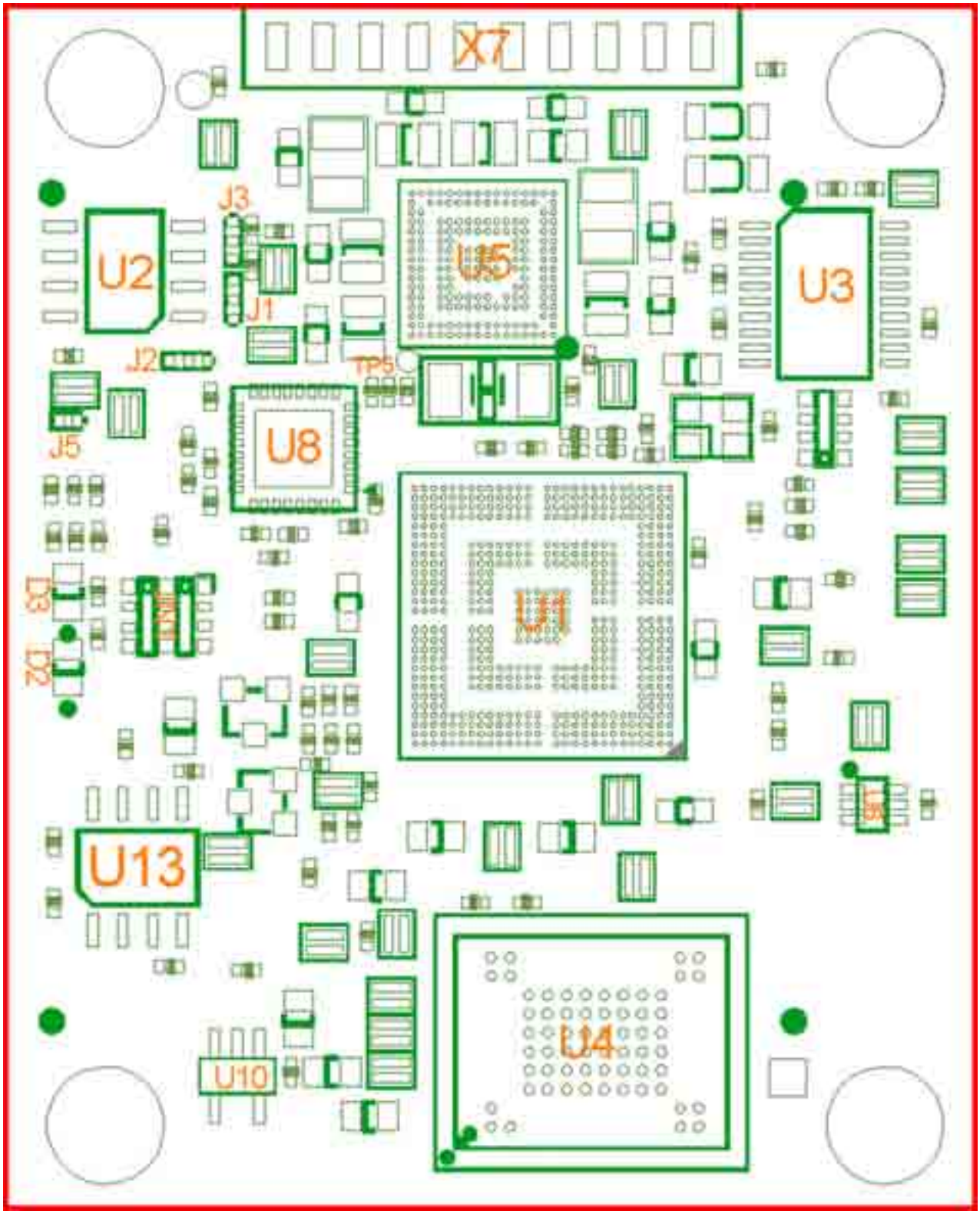


Figure 2: Top view of the phyCORE-OMAP44xx (controller side)

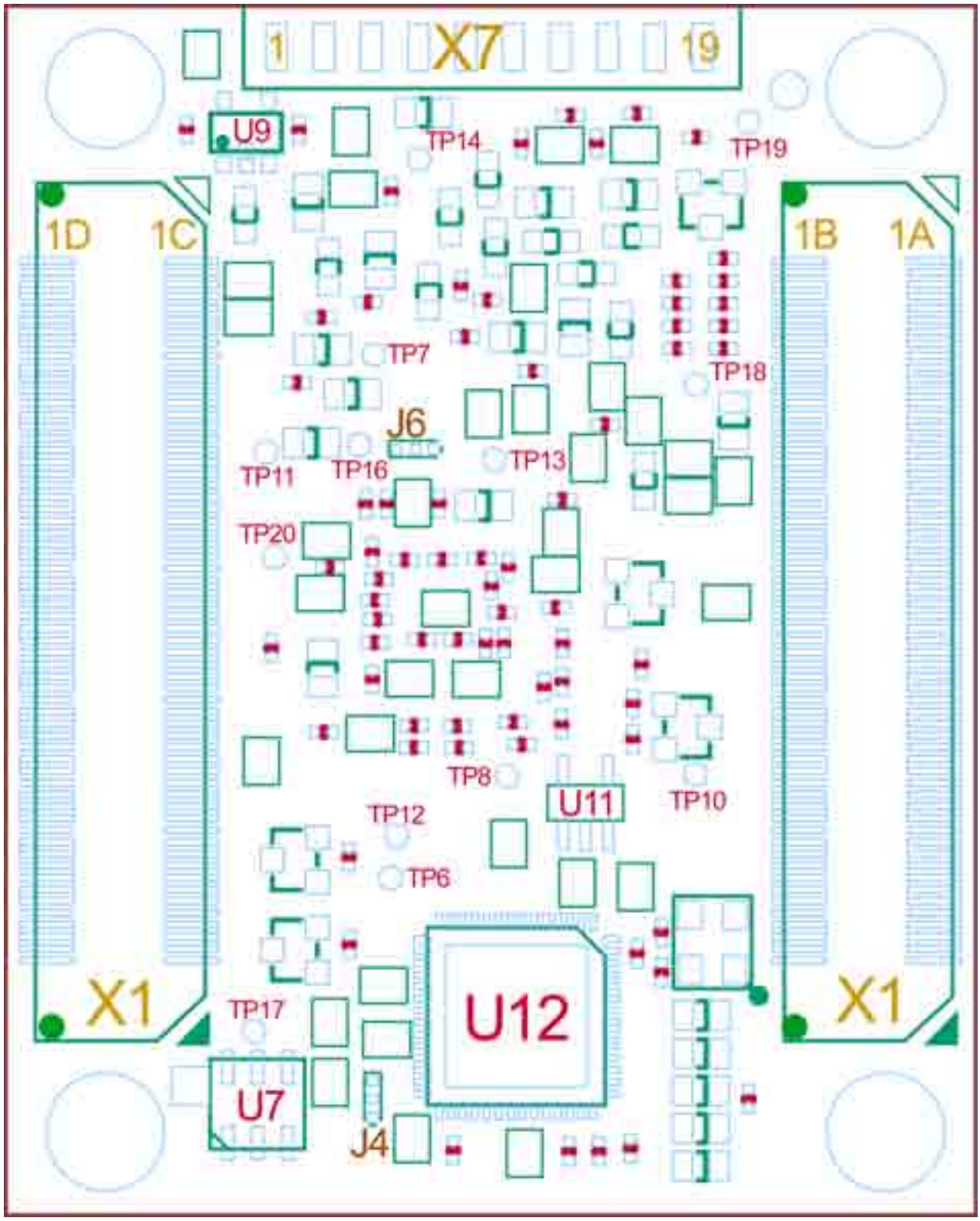


Figure 3: Bottom view of the phyCORE-OMAP44xx (connector side)

1.1.3 Minimum Requirements to Operate the phyCORE-OMAP44xx

Basic operation of the phyCORE-OMAP44xx only requires supply of a +3V3 input voltage with 1.0 A load and the corresponding GND connections.

These supply pins are located at the phyCORE-Connector X1:

VCC_3V3_IN: X1 1C, 2C, 3C, 4C, 5C, 1D, 2D, 3D, 4D, 5D

Connect all +3.3 V VCC input pins to your power supply and at least the matching number of GND pins.

Corresponding GND: X1 6C, 11C, 16C, 21C, 26C, 6D, 9D, 14D, 19D, 24D

Please refer to Section 1.2 for information on additional GND Pins located at the phyCORE-Connector X1.

Caution:

We recommend connecting all available +3V3 input pins to the power supply system on a custom carrier board housing the phyCORE-OMAP44xx and at least the matching number of GND pins neighboring the +3V3 pins. In addition, proper implementation of the phyCORE-OMAP44xx module into a target application also requires connecting all GND pins neighboring signals that are being used in the application circuitry. Please refer to Section 1.4 for more information.

1.2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

All controller signals extend to surface mount technology (SMT) connectors (0.5 mm) lining two sides of the module (referred to as the phyCORE-Connector). This allows the phyCORE-OMAP44xx to be plugged into any target application like a "big chip".

The numbering scheme for the phyCORE-Connector is based on a two dimensional matrix in which column positions are identified by a letter and row position by a number. Pin 1A, for example, is always located in the upper left hand corner of the matrix. The pin numbering values increase moving down on the board. Lettering of the pin connector rows progresses alphabetically from left to right (refer to Figure 4).

The numbered matrix can be aligned with the phyCORE-OMAP44xx (viewed from above; phyCORE-Connector pointing down) or with the socket of the corresponding phyCORE Carrier Board/user target circuitry. The upper left-hand corner of the numbered matrix (pin 1A) is thus covered with the corner of the phyCORE-OMAP44xx marked with a triangle. The numbering scheme is always in relation to the PCB as viewed from above, even if all connector contacts extend to the bottom of the module.

The numbering scheme is thus consistent for both the module's phyCORE-Connector as well as the mating connector on the phyCORE-OMAP44xx Carrier Board or target hardware, thereby considerably reducing the risk of pin identification errors.

Since the pins are exactly defined according to the numbered matrix previously described, the phyCORE-Connector is usually assigned a single designator for its position (X1 for example). In this manner the phyCORE-Connector comprises a single, logical unit regardless of the fact that it could consist of more than one physical socketed connector.

The following figure illustrates the numbered matrix system. It shows a phyCORE-OMAP44xx with SMT phyCORE-Connectors on its underside (defined as gray lines) mounted on a carrier board. In order to facilitate understanding of the pin assignment scheme, the diagram presents a cross-view of the phyCORE-module showing these phyCORE-Connectors mounted on the underside of the module's PCB.

Table 2 provides an overview of the Pin-out of the phyCORE-Connector with signal names and descriptions specific to the phyCORE-OMAP44xx. It also provides the appropriate signal level interface voltages listed in the SL (Signal Level) column and the signal direction.

Caution:

Most of the controller pins have multiple multiplexed functions. Because most of these pins are connected directly to the phyCORE-Connector the functions are also available there. Signal names and descriptions in Table 2, however, are in regard to the specification of the phyCORE-OMAP44xx and the functions defined therein. Please refer to the OMAP44xx Reference Manual, or the schematic to to get to know about alternative functions. In order to utilize a specific pin's alternative function the corresponding registers must be configured within the appropriate driver of the BSP. To support all features of the phyCORE-OMAP44xx Carrier Board a few changes have been made in the BSP delivered with the module. Table 42 lists all pins with functions different to what is described in Table 2.

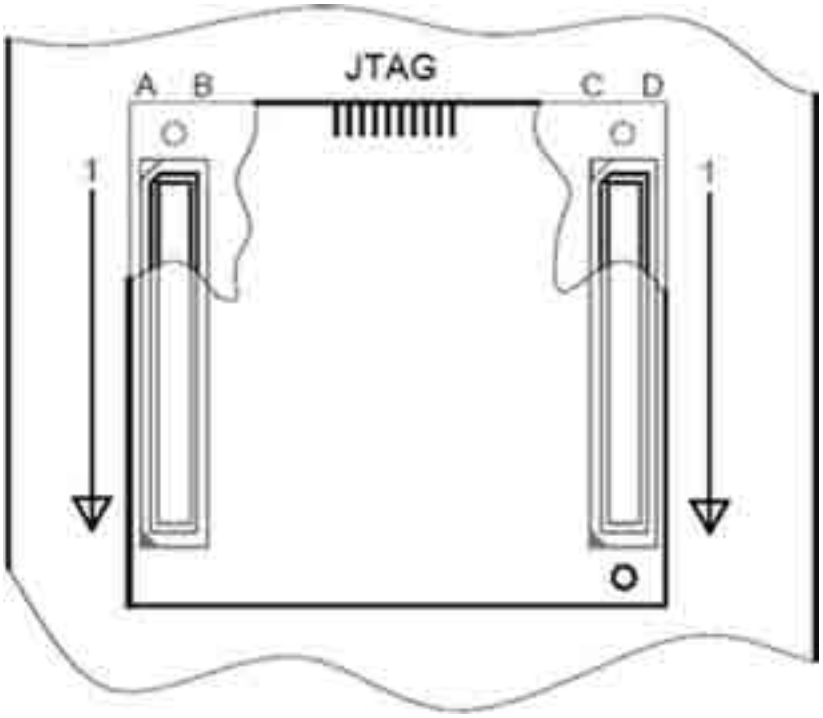


Figure 4: Pin-out of the phyCORE-Connector (top view, with cross section insert)

The Texas Instruments OMAP44xx is a multi-voltage operated microcontroller and as such special attention should be paid to the interface voltage levels to avoid unintentional damage to the microcontroller and other on-board components. Please refer to the Texas Instruments OMAP44xx Reference Manual for details on the functions and features of controller signals and port pins.

Note:

SL is short for Signal Level (V) and is the applicable logic level to interface a given pin. Those pins marked as "N/A" have a range of applicable values that constitute proper operation.

Pin Row X1A				
Pin #	**Signal**	**I/O**	**SL**	**Description**
1A	X_KPD_COL0	O	VCC_1V8_IO	Keyboard column 0 (open drain)
2A	GND	-	-	Ground 0V
3A	X_KPD_COL3	O	VCC_1V8_IO	Keyboard column 3 (open drain)
4A	X_KPD_ROW1	I	1.8 V	Keyboard row 1
5A	X_KPD_ROW2	I	1.8 V	Keyboard row 2
6A	X_KPD_ROW3	I	1.8 V	Keyboard row 3
7A	GND	-	-	Ground 0V
8A	X_CSI22_DX0	I	CSI	CSI2-B (CSI22) differential clock lane positive input
9A	X_CSI22_DY0	I	CSI	CSI2-B (CSI22) differential clock lane negative input
10A	X_CSI22_DX1	I	CSI	CSI2-B (CSI22) differential data lane positive input
11A	X_CSI22_DY1	I	CSI	CSI2-B (CSI22) differential data lane negative input
12A	GND	-	-	Ground 0V
13A	X_CSI21_DX0	I	CSI	CSI2-A (CSI21) differential clock positive input
14A	X_CSI21_DY0	I	CSI	CSI2-A (CSI21) differential clock negative input
15A	X_CSI21_DX1	I	CSI	CSI2-A (CSI21) differential data lane positive input 1
16A	X_CSI21_DY1	I	CSI	CSI2-A (CSI21) differential data lane negative input 1
17A	GND	-	-	Ground 0V
18A	X_I2C4_SDA	I/O	1.8 V / VCC_1V8_IO	I^2C4 data (open drain)
19A	X_SDMMC1_CMD	I/O	VCC_MMC1	SDMMC1 command
20A	X_SDMMC1_CLK	O	VCC_MMC1	SDMMC1 clock
21A	X_SDMMC1_DAT0	I/O	VCC_MMC1	SDMMC1 data bit 0
22A	GND	-	-	Ground 0V
23A	X_SDMMC1_DAT1	I/O	VCC_MMC1	SDMMC1 data bit 1
24A	X_SDMMC1_DAT2	I/O	VCC_MMC1	SDMMC1 data bit 2
25A	X_SDMMC1_DAT3	I/O	VCC_MMC1	SDMMC1 data bit 3
26A	X_SDMMC1_DAT4	I/O	VCC_MMC1	SDMMC1 data bit 4
27A	GND	-	-	Ground 0V

Table 2: Pin-out of the phyCORE-Connector X1, Row A

Pin Row X1A				
Pin #	**Signal**	**I/O**	**SL**	**Description**
28A	X_SDMMC1_DAT5	I/O	VCC_MMC1	SDMMC1 data bit 5
29A	X_SDMMC1_DAT6	I/O	VCC_MMC1	SDMMC1 data bit 6
30A	X_SDMMC1_DAT7	I/O	VCC_MMC1	SDMMC1 data bit 7
31A	X_SPI1_CS0	I/O	1.8 V / VCC_1V8_IO	McSPI1 chip select 0 (slave input, master output)
32A	GND	-	-	Ground 0V
33A	X_SPI1_CS3	O	VCC_1V8_IO	McSPI1 chip select 3
34A	X_SPI1_MISO	I/O	1.8 V / VCC_1V8_IO	McSPI1 master input/ slave output
35A	X_McASP_AXR	I/O	1.8 V / VCC_1V8_IO	ABE McASP serial data IO
36A	X_McASP_AFSX	O	VCC_1V8_IO	ABE McASP frame synchronization transmit
37A	GND	-	-	Ground 0V
38A	X_GPIO_115	I/O	1.8 V / VCC_1V8_IO	GPIO 115
39A	X_McASP_AMUTEIN	I	1.8 V	ABE McASP auto mute input
40A	X_McBSP3_DX	I/O	1.8 V / VCC_1V8_IO	ABE McBSP3 transmitted serial data
41A	X_McASP_ACLKX	O	VCC_1V8_IO	ABE McASP clock transmit
42A	GND	-	-	Ground 0V
43A	X_DMTIMER9	I/O	1.8 V / VCC_1V8_IO	DM timer event input or PWM output from pin AH24 of the OMAP44xx, or USBB2_ULPITTL_CLK output from pin AG12[1]
44A	X_DISPC_DATA22	O	VCC_1V8_IO	DISPC data bit 22
45A	X_DISPC_DATA20	O	VCC_1V8_IO	DISPC data bit 20
46A	X_DISPC_DATA19	O	VCC_1V8_IO	DISPC data bit 19
47A	GND	-	-	Ground 0V
48A	X_DISPC_DATA16	O	VCC_1V8_IO	DISPC data bit 16
49A	X_DISPC_DATA14	O	VCC_1V8_IO	DISPC data bit 14
50A	X_DISPC_DATA12	O	VCC_1V8_IO	DISPC data bit 12
51A	X_DISPC_DATA10	O	VCC_1V8_IO	DISPC data bit 10
52A	GND	-	-	Ground 0V
53A	X_DISPC_DATA8	O	VCC_1V8_IO	DISPC data bit 8
54A	X_DISPC_DATA6	O	VCC_1V8_IO	DISPC data bit 6

Table 2: Pin-out of the phyCORE-Connector X1, Row A

Pin Row X1A				
Pin #	**Signal**	**I/O**	**SL**	**Description**
55A	X_DISPC_DATA4	O	VCC_1V8_IO	DISPC data bit 4
56A	X_DISPC_DATA2	O	VCC_1V8_IO	DISPC data bit 2
57A	GND	-	-	Ground 0V
58A	X_DISPC_DATA0	O	VCC_1V8_IO	DISPC data bit 0
59A	X_DISPC_PCLK	O	VCC_1V8_IO	DISPC LCD pixel clock
60A	X_DISPC_DE	O	VCC_1V8_IO	DISPC data enable

Table 2: Pin-out of the phyCORE-Connector X1, Row A

1. configurable with J6

Pin Row X1B				
Pin #	**Signal**	**I/O**	**SL**	**Description**
1B	X_KPD_COL1	O	VCC_1V8_IO	Keyboard column 1 (open drain)
2B	X_KPD_COL2	O	VCC_1V8_IO	Keyboard column 2 (open drain)
3B	X_KPD_ROW0	I	1.8 V	Keyboard row 0
4B	GND	-	-	Ground 0V
5B	X_KPD_COL4_CSI21_DX3	O/I	VCC_1V8_IO / CSI	Keyboard column 4 (open drain) / CSI2-A (CSI21) differential data lane positive input 3[1]
6B	X_KPD_ROW4_CSI21_DY3	I	1.8 V / CSI	Keyboard row 4 / CSI2-A (CSI21) differential data lane negative input 3[1]
7B	X_KPD_COL5_CSI21_DX4	O/I	VCC_1V8_IO / CSI	Keyboard column 5 (open drain) / CSI2-A (CSI21) differential data lane positive input 4[1]
8B	X_KPD_ROW5_CSI21_DY4	I	1.8 V / CSI	Keyboard row 5 / CSI2-A (CSI21) differential data lane negative input 4[1]
9B	GND	-	-	Ground 0V
10B	X_CAM_SHUTTER	O	VCC_1V8_IO	Mechanical shutter control signal
11B	X_CAM_GLOBAL_RESET	I/O	1.8 V / VCC_1V8_IO	Camera sensor reset
12B	X_CAM_STROBE	O	VCC_1V8_IO	Camera flash activation trigger
13B	X_FREF_CLK1_OUT	O	VCC_1V8_IO	FREF clock 1 output
14B	GND	-	-	Ground 0V
15B	X_CSI21_DX2	I	CSI	CSI2-A (CSI21) differential data lane positive input 2

Table 3: Pin-out of the phyCORE-Connector X1, Row B

Pin Row X1B				
Pin #	**Signal**	**I/O**	**SL**	**Description**
16B	X_CSI21_DY2	I	CSI	CSI2-A (CSI21) differential data lane negative input 2
17B	X_I2C4_SCL	O	VCC_1V8_IO	I^2C4 clock (open drain)
18B	VCC_MMC1	O	1.8 V - 3.3 V	SDMMC1 reference voltage
19B	GND	-	-	Ground 0V
20B	X_SDMMC5_CMD	I/O	1.8 V / VCC_1V8_IO	SDMMC5 command
21B	X_SDMMC5_CLK	O	VCC_1V8_IO	SDMMC5 clock
22B	X_SDMMC5_DAT0	I/O	1.8 V / VCC_1V8_IO	SDMMC5 data bit 0
23B	X_SDMMC5_DAT1	I/O	1.8 V / VCC_1V8_IO	SDMMC5 data bit 1
24B	GND	-	-	Ground 0V
25B	X_SDMMC5_DAT2	I/O	1.8 V / VCC_1V8_IO	SDMMC5 data bit 2
26B	X_SDMMC5_DAT3	I/O	1.8 V / VCC_1V8_IO	SDMMC5 data bit 3
27B	X_PMIC_MMC1_CD	I	1.8 V	SDMMC1 card insertion and extraction detection
28B	X_McBSP3_CLKX	I/O	1.8 V / VCC_1V8_IO	ABE McBSP3 combined serial clock
29B	GND	-	-	Ground 0V
30B	VCC_1V8_IO	O	-	1.8 V IO reference voltage
31B	X_SPI1_CS1	O	VCC_1V8_IO	McSPI1 chip select 1
32B	X_SPI1_CS2	O	VCC_1V8_IO	McSPI1 chip select 2
33B	X_SPI1_MOSI	I/O	1.8 V / VCC_1V8_IO	McSPI1 master output / slave input
34B	X_SPI1_CLK	I/O	1.8 V / VCC_1V8_IO	McSPI1 clock master output / slave input
35B	GND	-	-	Ground 0V
36B	X_ABE_CLKS	I	1.8 V	ABE clock input
37B	X_McASP_AHCLKX	O	VCC_1V8_IO	ABE McASP high frequency clock output
38B	McASP_AMUTE	O	VCC_1V8_IO	ABE McASP auto mute output
39B	X_GPIO_114	I/O	1.8 V / VCC_1V8_IO	GPIO 114
40B	GND	-	-	Ground 0V
41B	X_McBSP3_FSX	I/O	1.8 V / VCC_1V8_IO	ABE McBSP3 combined frame synchronization
42B	X_McBSP3_DR	I	1.8 V	ABE McBSP3 received serial data
43B	X_DISPC_DATA23	O	VCC_1V8_IO	DISPC data bit 23

Table 3: Pin-out of the phyCORE-Connector X1, Row B

Pin Row X1B				
Pin #	**Signal**	**I/O**	**SL**	**Description**
44B	X_DISPC_DATA21	O	VCC_1V8_IO	DISPC data bit 21
45B	GND	-	-	Ground 0V
46B	X_DISPC_DATA18	O	VCC_1V8_IO	DISPC data bit 18
47B	X_DISPC_DATA17	O	VCC_1V8_IO	DISPC data bit 17
48B	X_DISPC_DATA15	O	VCC_1V8_IO	DISPC data bit 15
49B	X_DISPC_DATA13	O	VCC_1V8_IO	DISPC data bit 13
50B	X_DISPC_DATA11	O	VCC_1V8_IO	DISPC data bit 11
51B	GND	-	-	Ground 0V
52B	X_DISPC_DATA9	O	VCC_1V8_IO	DISPC data bit 9
53B	X_DISPC_DATA7	O	VCC_1V8_IO	DISPC data bit 7
54B	X_DISPC_DATA5	O	VCC_1V8_IO	DISPC data bit 5
55B	X_DISPC_DATA3	O	VCC_1V8_IO	DISPC data bit 3
56B	GND	-	-	Ground 0V
57B	X_DISPC_DATA1	O	VCC_1V8_IO	DISPC data bit 1
58B	X_DISPC_HSYNC	O	VCC_1V8_IO	DISPC horizontal synchronization
59B	X_DISPC_VSYNC	O	VCC_1V8_IO	DISPC vertical synchronization
60B	GND	-	-	Ground 0V

Table 3: Pin-out of the phyCORE-Connector X1, Row B

1. configurable with JN1

Pin Row X1C				
Pin #	**Signal**	**I/O**	**SL**	**Description**
1C	VCC_3V3_IN	I	Power	3.3 V Primary voltage supply input
2C	VCC_3V3_IN	I	Power	3.3 V Primary voltage supply input
3C	VCC_3V3_IN	I	Power	3.3 V Primary voltage supply input
4C	VCC_3V3_IN	I	Power	3.3 V Primary voltage supply input
5C	VCC_3V3_IN	I	Power	3.3 V Primary voltage supply input
6C	GND	-	-	Ground 0V
7C	VBAT	I	Power	Backup battery input
8C	X_nRESET_WARM	I	1.8 V	Warm Reset Input
9C	X_PMIC_PWRON	I	3.3 V	PMIC power on input
10C	X_UART1_TX	O	VCC_1V8_IO	Serial transmit signal UART 1
11C	GND	-	-	Ground 0V

Table 4: Pin-out of the phyCORE-Connector X1, Row C

Pin Row X1C				
Pin #	**Signal**	**I/O**	**SL**	**Description**
12C	X_UART3_RS232_CTS	I	RS-232	Serial clear to send UART 3
13C	X_UART3_RS232_RTS	O	RS-232	Serial request to send UART 3
14C	X_UART2_CTS	I	1.8 V	Serial clear to send UART2
15C	X_UART2_RTS	O	VCC_1V8_IO	Serial request to send UART2
16C	GND	-	-	Ground 0V
17C	X_USBC1_ICUSB_DP	I/O	USB	Interchip USB host data plus
18C	X_USBC1_ICUSB_DM	I/O	USB	Interchip USB host data minus
19C	X_USB_OTG_DP	I/O	USB	USB OTG data plus
20C	X_USB_OTG_DM	I/O	USB	USB OTG data minus
21C	GND	-	-	Ground 0V
22C	X_PMIC_USB_OTG_ID	I/O	USB	USB OTG connector identification signal
23C	X_PMIC_USB_OTG_VBUS	I	USB	USB OTG VBUS detection input
24C	X_ETH_TX+	O	VCC_3V3_S	Ethernet transmit positive output
25C	X_ETH_TX-	O	VCC_3V3_S	Ethernet transmit negative output
26C	GND	-	-	Ground 0V
27C	X_ETH_SPEED	O	VCC_3V3_S	Ethernet Speed Indicator (open drain)
28C	X_JTAG_TDO	O	VCC_1V8_IO	JTAG test data output
29C	X_JTAG_TMS	I/O	1.8 V / VCC_1V8_IO	JTAG test mode select
30C	X_JTAG_TCK	I	1.8 V	JTAG test clock input
31C	GND	-	-	Ground 0V
32C	X_JTAG_TDI	I	1.8 V	JTAG test data input
33C	X_DPM_EMU1	I/O	1.8 V / VCC_1V8_IO	Debug pin manager pin 1
34C	X_HDMI_HPD	I	1.8 V	HDMI display hot plug detect
35C	X_HDMI_DDC_SCL	I/O	1.8 V / VCC_1V8_IO	HDMI display data channel clock (open drain)
36C	GND	-	-	Ground 0V
37C	X_HDMI_DATA0X	O	HDMI	HDMI display data 0 differential positive or negative[1]
38C	X_HDMI_DATA0Y	O	HDMI	HDMI display data 0 differential positive or negative[1]
39C	X_HDMI_CLOCKX	O	HDMI	HDMI display clock differential positive or negative[1]

Table 4: Pin-out of the phyCORE-Connector X1, Row C

Pin Row X1C				
Pin #	**Signal**	**I/O**	**SL**	**Description**
40C	X_HDMI_CLOCKY	O	HDMI	HDMI display clock differential positive or negative[1]
41C	GND	-	-	Ground 0V
42C	X_PMIC_SYSEN	O	1.8 V	PMIC external system enable
43C	X_PMIC_PREQ3	I	1.8 V	PMIC peripheral 3 power request input
44C	X_PMIC_PREQ2A	I/O	1.8 V / VCC_1V8_IO	PMIC peripheral 2A power request input / Ethernet controller power management event signal (PME)
45C	GND	-	-	Ground 0V
46C	X_DSI1_DX0	O	DSI	DSI1 display lane 0 differential positive or negative[1]
47C	X_DSI1_DY0	O	DSI	DSI1 display lane 0 differential positive or negative[1]
48C	X_DSI1_DX2	O	DSI	DSI1 display lane 2 differential positive or negative[1]
49C	X_DSI_DY2	O	DSI	DSI1 display lane 2 differential positive or negative[1]
50C	GND	-	-	Ground 0V
51C	X_DSI1_DX4	O	DSI	DSI1 display lane 4 differential positive or negative[1]
52C	X_DSI1_DY4	O	DSI	DSI1 display lane 4 differential positive or negative[1]
53C	X_I2C1_SCL	O	VCC_1V8_IO	I^2C1 clock (open drain)
54C	X_I2C1_SDA	I/O	1.8 V / VCC_1V8_IO	I^2C1 data (open drain)
55C	GND	-	-	Ground 0V
56C	X_1-WIRE_3V3	I/O	3.3 V	Hardware Introspection Interface **For internal use only**
57C	X_BOOT0	I	1.8 V	System boot configuration pin 0
58C	X_BOOT2	I	1.8 V	System boot configuration pin 2
59C	X_BOOT4	I	1.8 V	System boot configuration pin 4
60C	GND	-	-	Ground 0V

Table 4: Pin-out of the phyCORE-Connector X1, Row C

1. Can be configured by setting the appropriate control register. Please refer to the OMAP44xx Reference manual for more information.

Pin Row X1D				
Pin #	**Signal**	**I/O**	**SL**	**Description**
1D	VCC_3V3_IN	I	Power	3.3 V Primary voltage supply input
2D	VCC_3V3_IN	I	Power	3.3 V Primary voltage supply input
3D	VCC_3V3_IN	I	Power	3.3 V Primary voltage supply input
4D	VCC_3V3_IN	I	Power	3.3 V Primary voltage supply input
5D	VCC_3V3_IN	I	Power	3.3 V Primary voltage supply input
6D	GND	-	-	Ground 0V
7D	X_nRESET_PWRON	I/O	1.8 V	System reset: output of PMIC, input of controller
8D	X_nRESET_PER	I/O	1.8 V	Peripheral reset: output of controller, input of Ethernet controller and USB PHY
9D	GND	-	-	Ground 0V
10D	X_UART1_RX	I	1.8 V	Serial receive signal UART 1
11D	X_UART3_RS232_TX	O	RS-232	Serial transmit signal UART 3
12D	X_UART3_RS232_RX	I	RS-232	Serial receive signal UART 3
13D	X_UART2_TX	O	VCC_1V8_IO	Serial transmit signal UART 2
14D	GND	-	-	Ground 0V
15D	X_UART2_RX	I	1.8 V	Serial receive signal UART 2
16D	X_UART4_TX	O	VCC_1V8_IO	Serial transmit signal UART 4
17D	X_UART4_RX	I	1.8 V	Serial receive signal UART 4
18D	X_USBB1_OC_GPIO_120	I	1.8 V	USB Host overcurrent signal input
19D	GND	-	-	Ground 0V
20D	X_USBB1_DP	I/O	USB	USB Host data plus
21D	X_USBB1_DM	I/O	USB	USB Host data minus
22D	X_USBB1_PWR	O	VCC_3V3_S	External USB bus voltage (5V) enable
23D	3V3_S Reference Voltage	O	VCC_3V3_S	3.3 V (VCC_3V3_S) reference voltage
24D	GND	-	-	Ground 0V
25D	X_ETH_RX+	I	VCC_3V3_S	Ethernet receive positive input
26D	X_ETH_RX-	I	VCC_3V3_S	Ethernet receive negative input
27D	X_ETH_LINK	O	VCC_3V3_S	Ethernet link indicator (open drain)
28D	X_GPIO_WK30	I/O	1.8 V / VCC_1V8_IO	GPIO WK30

Table 5: Pin-out of the phyCORE-Connector X1, Row D

Pin Row X1D				
Pin #	**Signal**	**I/O**	**SL**	**Description**
29D	X_FREF_CLK4_REQ	I	1.8 V	FREF clock request 4
30D	GND	-	-	Ground 0V
31D	X_JTAG_nTRST	I	1.8 V	JTAG test reset
32D	X_JTAG_RTCK	O	VCC_1V8_IO	JTAG ARM clock emulation
33D	X_DPM_EMU0	I/O	1.8 V / VCC_1V8_IO	Debug pin manager pin 0
34D	X_HDMI_CEC	I/O	1.8 V / VCC_1V8_IO	HDMI consumer electronic control
35D	X_HDMI_DDC_SDA	I/O	1.8 V / VCC_1V8_IO	HDMI display data channel data (open drain)
36D	GND	-	-	Ground 0V
37D	X_HDMI_DATA1X	O	HDMI	[1]HDMI display data 1 differential positive or negative[1]
38D	X_HDMI_DATA1Y	O	HDMI	HDMI display data 1 differential positive or negative[1]
39D	X_HDMI_DATA2X	O	HDMI	HDMI display data 2 differential positive or negative[1]
40D	X_HDMI_DATA2Y	O	HDI	HDMI display data 2 differential positive or negative[1]
41D	GND	-	-	Ground 0V
42D	X_SYS_NIRQ2	I	1.8 V	External interrupt
43D	X_FREF_CLK4_OUT	O	VCC_1V8_IO	FREF clock 4 output
44D	X_PMIC_CLK32KAUDIO	O	1.8 V	32-kHz digital gated output clock (for audio device)
45D	GND	-	-	Ground 0V
46D	X_DSI1_DX1	O	DSI	DSI1 display lane 1 differential positive or negative[1]
47D	X_DSI1_DY1	O	DSI	DSI1 display lane 1 differential positive or negative[1]
48D	X_DSI1_DX3	O	DSI	DSI1 display lane 3 differential positive or negative[1]
49D	X_DSI1_DY3	O	DSI	DSI1 display lane 3 differential positive or negative[1]
50D	GND	-	-	Ground 0V
51D	X_I2C3_SCL	O	VCC_1V8_IO	I^2C3 clock (open drain)
52D	X_I2C3_SDA	I/O	1.8 V / VCC_1V8_IO	I^2C3 data (open drain)
53D	X_PMIC_EXTCHRG_ENZ	O	1.8 V	Output control signal to an external VAC charger

Table 5: Pin-out of the phyCORE-Connector X1, Row D

Pin Row X1D				
Pin #	**Signal**	**I/O**	**SL**	**Description**
54D	X_PMIC_VAC	I	-	Input for external VAC charger detection
55D	GND	-	-	Ground 0V
56D	X_PMIC_CHRG_EXTCHRG_STATZ	I	1.8 V	External charger status pin
57D	X_BOOT1	I	1.8 V	System boot configuration pin 1
58D	X_BOOT3	I	1.8 V	System boot configuration pin 3
59D	GND	-	-	Ground 0V
60D	X_BOOT5	I	1.8 V	System boot configuration pin 5

Table 5: Pin-out of the phyCORE-Connector X1, Row D

1. Can be configured by setting the appropriate control register. Please refer to the OMAP44xx Reference manual for more information.

1.3 Jumpers

For configuration purposes, the phyCORE-OMAP44xx has 7 solder jumpers, some of which have been installed prior to delivery. Figure 5 illustrates the numbering of the solder jumper pads, while Figure 6 and Figure 7 indicate the location of the solder jumpers on the board. 5 solder jumpers are located on the top side of the module (opposite side of connectors) and 2 solder jumpers are located on the bottom side of the module (connector side). Table 6 below provides a functional summary of the solder jumpers which can be changed to adapt the phyCORE-OMAP44xx to your needs. It shows their default positions, and possible alternative positions and functions. A detailed description of each solder jumper can be found in the applicable chapter listed in the table.

Figure 5: Typical Jumper Pad Numbering Scheme

If manual jumper modification is required please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Please pay special attention to the "TYPE" column to ensure you are using the correct type of jumper (0 Ohms, 10 k Ohms, etc...). The jumpers are 0402 package with a 1/8 W or better power rating, while JN1 is a resistor array (1206).

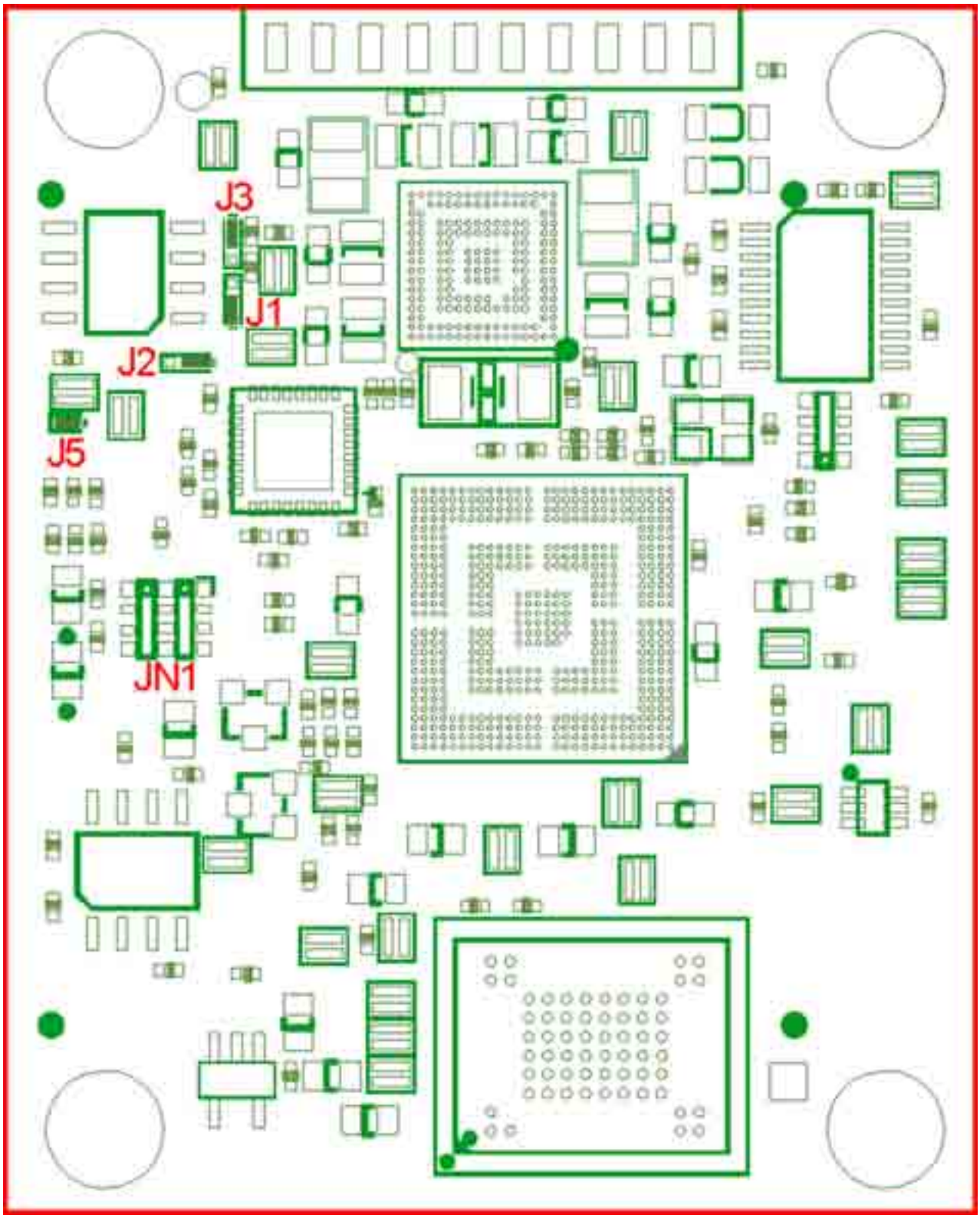


Figure 6: Jumper Locations (top view)

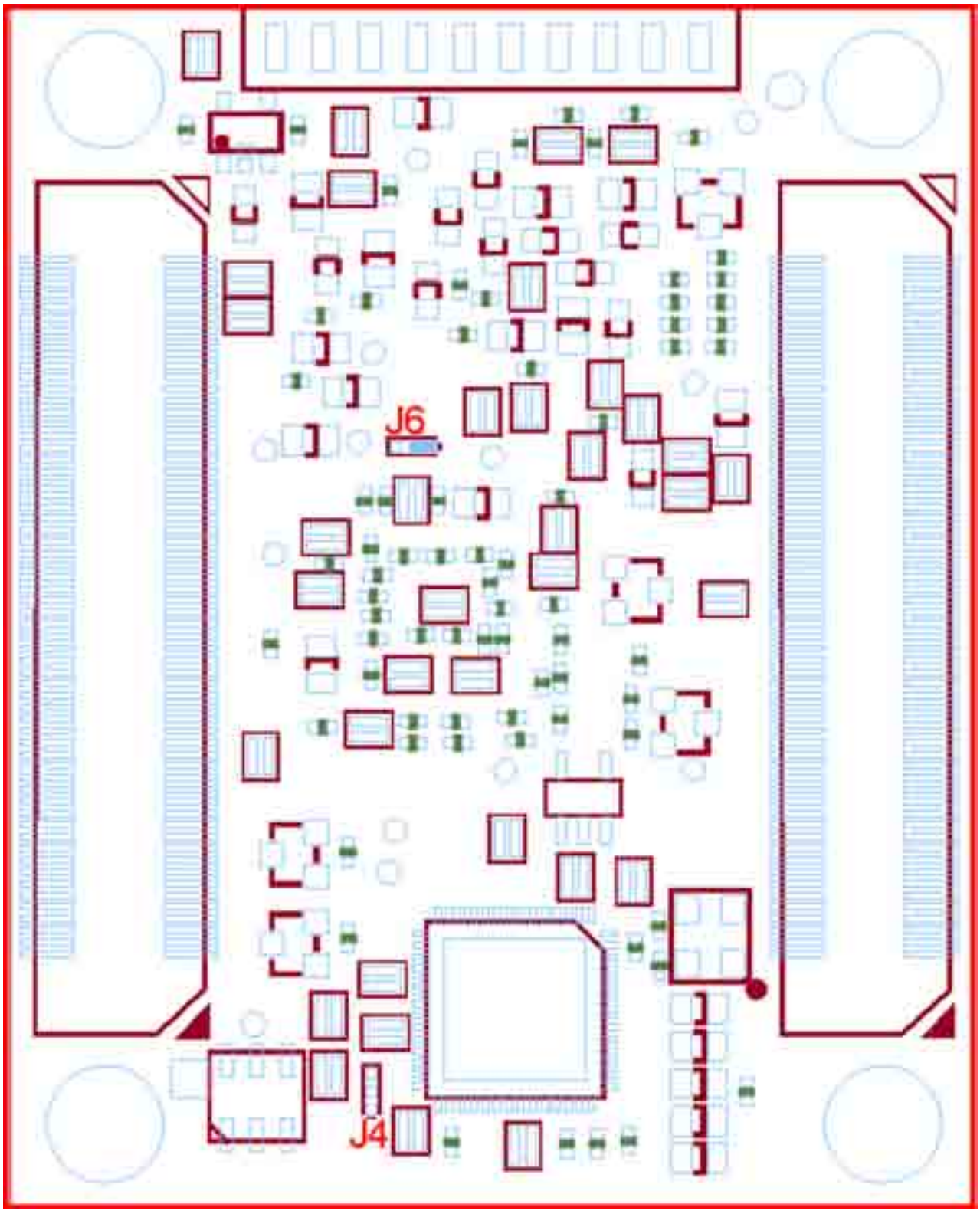


Figure 7: Jumper Locations (bottom view)

The jumpers (J = solder jumper) have the following functions:

Jumper	Description	Type	Chapter
J2, J1, J3	J2, J1 and J3 define the slave addresses (A0 to A2) of the serial memory U2 on the I^2C1 bus. In the high-nibble of the address, I^2C memory devices have the slave ID 0xA. The low-nibble is build from A2, A1, A0, and the R/W bit.	0R (0402)	Section 1.6.3.1
all 1+2	**A0 = 0, A1 = 0, A2= 0, => 0x0 / 0x1 (W/R) are selected as the low-nibble of the EEPROM's address**		
other settings	please refer to Table 13 to find alternative addresses resulting from other combinations of jumpers J1, J2, and J3		
J4	J4 connects pin G5 of the NAND-Flash at U4 to 1.8 V or GND. On many NAND memory devices pin G5 enables/disables the activation of the lock function. It is not guaranteed that the standard NAND memory populating the phyCORE-OMAP44xx will have this lock function. Please refer to the corresponding NAND memory data sheet for more detailed information.	0R (0402)	Section 1.6.2.1
1+2 or **open**	**NAND-Flash U4 not locked**		
2+3	NAND-Flash U4 locked		
J5	J5 connects pin 7 of the serial memory at U2 to GND. On many memory devices pin 7 enables/disables the activation of a write protect function. It is not guaranteed that the standard serial memory populating the phyCORE-OMAP44xx will have this write protection function. Please refer to the corresponding memory data sheet for more detailed information.	0R (0402)	Section 1.6.3.2
open	EEPROM U2 is write protected		
closed	**EEPROM U2 is not write protected**		
J6	J6 connects either pin AH24 (DMTIMER9) or pin AG12 (USBB2_ULPITLL_CLK) of the OMAP44xx controller U1 to pin 43A (X_DMTIMER9) of the phyCORE-Connector X1.	0R (0402)	Section 1.11.1
1+2	**Pin AH24 (DMTIMER9) of controller U1 is connected to phyCORE-Connector X1, which means that pin X1A43 can be used as PWM output for brightness control**		
2+3	Pin AG12 (USBB2_ULPITTL_CLK) of controller U2 is connected to phyCORE-Connector X1[1]		

Table 6: phyCORE-OMAP44xx Jumper Settings

Jumper	Description	Type	Chapter
JN1	JN1 allows to connect either the last 4 signals of the keyboard interface or lanes 3 and 4 of the primary camera interface CSI2-A (CSI21) to pins X1B5 to X1B8 of the phyCORE-Connector.	4 x 0R (resistor array 1206)	Section 1.12 Section 1.13
Position 1 (pins 1 + 2, 4 + 5, 7 + 8, and 10 + 11 connect pairwise)	**Last 4 signals of the keyboard interface (KPD_COL4, KPD_ROW4, KPD_COL5,KPD_ROW5) are connected to pins X1B5 to X1B8**		
Position 2 (pins 2 + 3, 5 + 6, 8 + 9, and 11 + 12 connect pairwise)	Last 4 lanes of the primary camera interface (CSI21_DX3, CSI21_DY3, CSI21_DX4, CSI21_DY4) extend to pins X1B5 to X1B8		

Table 6: phyCORE-OMAP44xx Jumper Settings

1. This option is intend for applications without display, but the need for the complete set of signals of the second ULPI interface.

1.4 Power

The phyCORE-OMAP44xx operates off of a single power supply voltage.

The following sections of this chapter discuss the primary power pins on the phyCORE-Connector X1 in detail.

1.4.1 Primary System Power (VCC_3V3_IN)

The phyCORE-OMAP44xx operates off of a primary voltage supply with a nominal value of +3.3 V. On-board switching regulators generate the 0.93V, 1.2 V, 1.8 V, 2.1 V and 3 V voltage supplies required by the OMAP44xx MCU and on-board components from the primary 3.3 V supplied to the SOM.

For proper operation the phyCORE-OMAP44xx must be supplied with a voltage source of 3.3 V ± 5% with 1.0 A load at the VCC pins on the phyCORE-Connector X1.

VCC_3V3_IN: X1 1C, 2C, 3C, 4C, 5C, 1D, 2D, 3D, 4D, 5D

Connect all +3.3 V VCC input pins to your power supply and at least the matching number of GND pins.

Corresponding GND: X1 6C, 11C, 16C, 21C, 26C, 6D, 9D, 14D, 19D, 24D

Please refer to Section 1.2 for information on additional GND Pins located at the phyCORE-Connector X1.

Caution:

As a general design rule we recommend connecting all GND pins neighboring signals which are being used in the application circuitry. For maximum EMI performance all GND pins should be connected to a solid ground plane.

1.4.2 Backup Voltage (VBAT)

To backup the RTC of the PMIC TWL6030 on the module, a secondary voltage source of 3.3 V can be attached to the phyCORE-OMAP44xx at pin X1C7. This voltage source is supplying the backup voltage domain VBACKUP of the PMIC which again supplies the RTC and some critical registers if the primary system power (VCC_3V3_IN) is removed. Applications not requiring a backup mode can connect the VBAT pin to the primary system power supply (VCC = 3.3 V), or can leave it open.

1.4.3 Power Management IC (U5)

The phyCORE-OMAP44xx provides an on-board Power Management IC (PMIC) TWL6030 at position U5 to source the different voltages required by the processor and on-board components. Figure 8 presents a graphical depiction of the powering scheme.

The TWL6030 supports many functions like on-chip RTC and different power management functionalities. It is connected to the OMAP44xx via the I2C1 bus and the OMAP44xx smart reflex bus. The I2C1 addresses of the TWL6030 are 0x48, 0x49 and 0x4A (7 MSB). The smart reflex address is 0x12 (7MSB).

Please refer to the Texas Instruments TWL6030 datasheet for further information.

1.4.3.1 Power domains

The PMIC has two input voltage rails as can be seen in Figure 8 VCC_3V3 and VBAT. VCC_3V3 is supplied from the primary voltage input pins VCC_3V3_IN of the phyCORE-OMAP44xx, whereas VBAT is supplied from the secondary voltage input pin X1C7. The following list summarizes the relation between the different voltage rails and the devices on the phyCORE-OMAP44xx:

External voltages: VCC_3V3_IN and VBAT (optional)

- VCC_3V3_IN: Voltage Regulator, 1-Wire Levelshifter, 1-Wire EEPROM (via current sense amplifier at U9)
- VBAT: Voltage Regulator

Internally generated voltages: VCC_CORE1 (0.93 V-1.1 V), VCC_CORE2 (0.93 V-1.1 V), VCC_CORE3 (0.93 V-1.1 V), VCC_1V8_IO (1.8 V), VCC_MEM (1.2 V), VCC_V1V29 (1.2 V), VCC_2V1 (2.1 V), VCC_CXIO (1.8 V), VCC_DAC (1.8 V), VCC_MMC1 (3 V/1.8 V), VCC_3V3_S (3.3 V), VCC_PP (3.3 V), VCC_USB_3V3 (3.3 V)

- VCC_CORE1 (0.93 V-1.1 V) OMAP44xx mpu (VDD_MPU)
- VCC_CORE2 (0.93 V-1.1 V) OMAP44xx iva audio (VDD_IVA_AUDIO)
- VCC_CORE3 (0.93 V-1.1 V) OMAP44xx core (VDD_CORE), dll (VDDA_DLL)
- VCC_PP (3.3 V) OMAP44xx eFuse prgr. module (VPP_CUST)
- VCC_USB_3V3 (3.3 V) OMAP44xx USB OTG 0 (VDDA_USBA0OTG_3P3V)
- VCC_1V8_IO (1.8 V) OMAP44xx IO, OMAP44xx LPDDR2 pop memory (POP_VDD1_LPDDR), USB PHY IO, Ethernet controller IO, EEPROM, NAND-Flash, MMC2, logic of the RS-232 transceiver, IO reference voltage at phyCORE-Connector X1B30, signal level of I^2C, SPI and JTAG interfaces
- VCC_MEM (1.2 V) OMAP44xx LPDDR2 pop memory (POP_VDD2_LPDDR)
- VCC_V1V29 (1.2 V) OMAP44xx LPDDR2 (VDDQ_LPDDR2, VDDCA_LPDDR2) and LDO (VDDA_LDO)
- VCC_2V1 (2.1 V) PMIC, used to generate VCC_CXIO and VCC_DAC via LDOs
- VCC_CXIO (1.8 V) OMAP44xx DSI (VDDA_DSI), CSI (VDDA_CSI), OTG (VDDA_USBA0OTG_1P8V), and DPLL (VDDA_DPLL)
- VCC_DAC (1.8 V) OMAP44xx HDMI (VDDA_HDMI)
- VCC_MMC1 (3 V/1.8 V) OMAP44xx MMC (VDDS_SDMMC1) and MMC1 reference voltage at phyCORE-Connector X1B18 (switchable between 3 V and 1.8 V via PMIC register, default 3 V)
- VCC_3V3_S (3.3 V) RS-232 Transceiver, USB PHY, Ethernet controller, User LEDs, 3V3_S reference voltage at phyCORE-Connector X1D23 (connected to main supply VCC_3V3 through FET Q3, switchable via PMIC REGEN1 output)

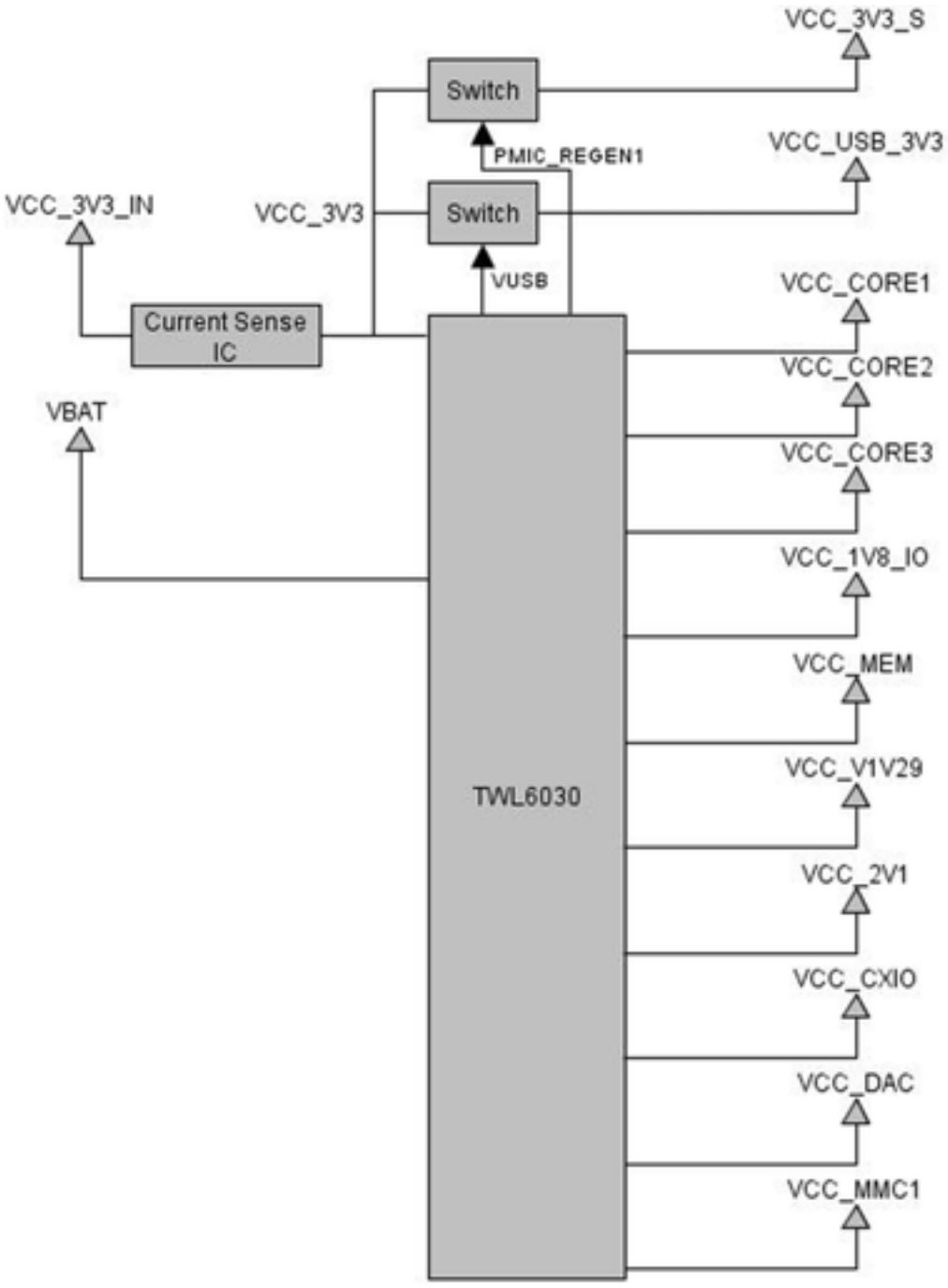


Figure 8: Power Supply Diagram

1.4.3.2 Real Time Clock (RTC)

The TWL6030 PMIC, which is populated on the module, provides a real time clock (RTC) with alarm and time- keeping functions. The RTC is supplied by the backup voltage VBAT if the main power supply VCC_3V3_IN is not applied.

The RTC stores the time (seconds/minutes/hours) and date (day/month/year/day of the week) information in binary-coded decimal (BCD) code up to year 2099. It can generate two programmable interrupts. The timer interrupt is a periodically generated interrupt (1s/1m/1h/1d period), while the alarm interrupt can be generated a precise time of the day to initiate a wake-up of the platform.[1]

1.4.3.3 Power Management

The TWL6030 PMIC provides different power management functions. These include, among others, alternating between different power groups and in further consequence switching the voltage domains. The peripheral power request inputs PREQ1. PREQ3 are responsible for switching the different power groups. Furthermore signals to control the power-on/off state of the system (X_PMIC_PWRON) and to control an external power supply (X_PMIC_SYSEN) are available.

The following table shows the power management signals and their functions.

Pin #	Signal name	Connected to	Description
-	PMIC_PREQ1	OMAP44xx (U1) signal SYS_PWR_REQ	Can be triggered by the controller to switch between power modes.[1]
X1C44	X_PMIC_PREQ2A	phyCORE-Connector (X1), Ethernet controller (U12) signal PME	This signal can be triggered from outside to switch power group 2. It can also be triggered in case of a wake-up event of the Ethernet controller.[1]
X1C43	X_PMIC_PREQ3	phyCORE-Connector (X1)	This signal can be triggered from outside to switch power group 3.[1]
X1C9	X_PMIC_PWRON	phyCORE-Connector (X1)	This signal can be triggered from outside to control system power on/off. A low-level signal of approx. 2 s initiates a power on, while a signal longer than 10 s causes a hardware switch-off.
X1C42	X_PMIC_SYSEN	phyCORE-Connector (X1)	This output is controlled by the power-management module and is activated during power-on/off sequence. SYSEN can be used to control an external power supply.

Table 7: Power Management Signals

1. All special functions of the PMIC such as use of power groups, etc. require the PMIC to be programmed via I^2C interface. At the time of delivery only the generation of the required voltages is implemented . Please refer to the TWL6030 Technical Ref. Man. for more information on how to program the PMIC.

Please refer to the Texas Instruments TWL6030 datasheet for further information

1. All special functions of the PMIC such as RTC interrupts, use of power groups, etc. require the PMIC to be programmed via I^2C interface. At the time of delivery only the generation of the required voltages is implemented . Please refer to the TWL6030 Technical Ref. Man. for more information on how to program the PMIC.

1.4.3.4 External Battery Charging

The TWL6030 PMIC can be interfaced with an auxiliary stand-alone charger device like the Texas Instruments BQ24156A. For this purpose three control signals are available on the phyCORE-Connector X1. Please refer to the TWL6030 data sheet for further information about the external charger IC signals and how to connect them.

The following table shows the external charger signals.

Pin #	Signal	I/O	SL	Description
X1D53	X_PMIC_EXTCHRG_ENZ	O	1.8 V	Control signal to an external VAC charger
X1D54	X_PMIC_VAC	I	-	Input for external VAC charger detection
X1D56	X_PMIC_CHRG_EXTCHRG_STATZ	I	1.8 V	External charger status pin

Table 8: Location of External Charger Signals

1.4.3.5 Voltage Level and Current Consumption Measuring

Besides the internal monitoring features of the TWL6030 PMIC, like thermal monitoring, the phyCORE-OMAP44xx allows for measuring the 3.3 V main supply voltage VCC_3V3, the 1.8 V IO voltage VCC_1V8_IO and the current consumption of the module. Thus it is possible to monitor these values in software, too.

The two voltages (VCC_3V3 and VCC_1V8_IO) can be measured by using the embedded general purpose ADCs (GPADC2 and GPADC3) of the TWL6030 PMIC. The current consumption of the module is converted to a proportional voltage by the Linear Technology current sense IC LT6106 (U9). The resulting voltage can be measured by reading the value of GPADC4 of the TWL6030. The current consumption is approximately 1.357 times the voltage measured by GPADC4. Please consider, because of system measuring errors the determined value doesn't equate exactly to the phyCORE's current consumption (measuring error ± 5%).

The GPADCs and the measured values can be read out via the I2C1 bus.

1.4.4 Reference Voltages

The voltage level of the phyCOREs logic circuitry is VCC_1V8_IO (1.8 V) which is generated on-board. In order to allow connecting external devices to the phyCORE-OMAP44xx without the need of another voltage source in addition to the primary supply this voltage is brought out at pin X1B30 of the phyCORE-Connector.

Use of level shifters supplied with VCC_1V8_IO allows converting the signals according to the needs on the custom target hardware. Alternatively signals can be connected to an open drain circuitry with a pull-up resistor attached to VCC_1V8_IO.

Further reference voltages are VCC_MMC1 and VCC_3V3_S:

VCC_MMC1 is needed because the MMC1 supply voltage can be switched between 1.8 V and the default 3 V by setting the corresponding register of the PMIC. The MMC1 reference voltage is brought out at pin X1B18.

VCC_3V3_S is the reference voltage of the switchable 3.3 V domain which provides the supply the voltages of the RS-232 transceiver, the Ethernet controller and the USB PHY. This reference voltage can be used e.g. to switching the center tap supply voltage of the Ethernet transformer to avoid non wanted back current to the module if 3V3_S is turned off during standby. The VCC_3V3_S reference voltage is brought out at pin X1D23.

Please take care not to load the reference voltage too heavily to avoid any disfunction or damage of the module. The following maximum loads are allowed:

- VCC_1V8_IO (1.8 V): 400 mA
- VCC_MMC1 (3 V/1.8 V): 150 mA
- VCC_3V3_S (3.3 V): 500 mA

1.5 System Configuration and Booting

Although most features of the OMAP44xx microcontroller are configured and/or programmed during the initialization routine, other features, which impact program execution, must be configured prior to initialization via pin termination.

The system start-up configuration includes:

- Clock configuration
- Boot device order configuration

During the reset cycle the operational system boot mode of the OMAP44xx processor is determined by the configuration of eight SYSBOOT pins sys_boot[7:0]. Pins sys_boot[5:0] are used to select interfaces or devices for the booting list, while pins sys_boot[7:6] select the OMAP clock source configuration. All eight pins are sampled and latched onto the SYSCTRL_GENERAL_CORE.CONTROL_STATUS[7:0] SYS_BOOT register bit field during the execution of the ROM code.

The internal ROM code is the first code executed during the initialization process of the OMAP44xx after POR. Besides the selection of the system clock source (based on the configuration of pins sys_boot[7:6]), the ROM code detects which boot devices the controller has to check by using the sys_boot[5:0] pin configuration. For peripheral boot devices, the ROM code polls the communication interface selected , initiates the download of the code into the internal RAM and triggers its execution from there. Peripheral booting is normally not applicable after a warm reset. For memory booting, the ROM code finds the bootstrap in permanent memories such as NAND-Flash or SD-Cards and executes it. Memory booting is normally applicable after a cold, or a warm reset. Please refer to the OMAP44xx Reference Manual for more information.

A configuration circuitry (pull-up and pull-down resistors connected to sys_boot[7:0]) is located on the phyCORE module, so no further settings are necessary. The boot configuration of pins sys_boot[5:0] on the standard phyCORE-OMAP44xx module with 512MB NAND Flash is '**0b111001**'. Consequently, the system tries to boot from NAND-Flash first, and, in case of a failure, successively from USB, UART and MMC1. Pins sys_boot[7:6] are factory-set to '**0b00**', meaning that the on-chip oscillator is selected as system clock source.

The on-board configuration circuitry of sys_boot[5:0] can be overwritten by pull-up, or pull-down resistors connected to the boot configuration pins (X1C57 - X1C59, X1D57, X1D58 and X1D60) of the phyCORE-OMAP44xx.

The following tables show the different boot device orders, which can be selected by configuring the six boot configuration pins, X_BOOT[5:0] of the phyCORE-OMAP44xx. Please note that only the useful configurations are listed in the tables. For a complete list of the OMAP44xx boot modes please refer to the Texas Instruments OMAP44xx Reference Manual.

The first table lists the booting device order when it is preferred to boot from memory type devices. This mode is selected when sys_boot[5] is tied high. The second table lists the booting device order when it is preferred to boot from peripheral-type devices. This mode is selected when sys_boot[5] is tied low.

Note:

Only permanent booting devices (marked in **bold**) are put on the booting list in case of a warm reset, as peripheral booting is normally not applicable after a warm reset.

Boot Mode Selection X_BOOT[5:0]	Booting Device Order			
	1st	2nd	3rd	4th
100011	**NAND**	USB		
100101	**MMC1**	USB		
101011	**NAND**	UART		
101101	**MMC1**	UART		
111001 (default)	**NAND**	USB	UART	MMC1
111010	**MMC2 (multiplexed with MMC5, only dat0-3)**	UART		
111011	**MMC1**	USB	UART	
111100	**MMC2 (multiplexed with MMC5, only dat0-3)**	USB		

Table 9: Boot Modes of the phyCORE-OMAP44xx (memory type devices preferred)[1]

1. Defaults are in **bold blue** text

Boot Mode Selection X_BOOT[5:0]	Booting Device Order			
	1st	2nd	3rd	4th
000011	USB	**NAND**		
000101	USB	**MMC1**		
001011	UART	**NAND**		
001101	UART	**MMC1**		
011001	USB	UART	MMC1	**NAND**
011010	UART	**MMC2 (multiplexed with MMC5, only dat0-3)**		
011011	USB	UART	**MMC1**	
011100	USB	**MMC2 (multiplexed with MMC5, only dat0-3)**		

Table 10: Boot Modes of the phyCORE-OMAP44xx (peripheral type devices preferred)

1.6 System Memory

The phyCORE-OMAP44xx provides three types of on-board memory:

1. LPDDR2 (PoP): 512 MB (up to 1 GB)
2. NAND Flash: 512 MB (up to 4 GB)
3. I^2C-EEPROM: 32 kB

The following sections of this chapter detail each memory type used on the phyCORE-OMAP44xx.

1.6.1 LPDDR2-SDRAM (U1, PoP Memory)

The RAM memory of the phyCORE-OMAP44xx is comprised of a 64-bit wide LPDDR2-SDRAM PoP (Package on Package) chip at U1 which is internal subdivided in two 32-bit wide LPDDR2-SDRAM dies. The chip is connected to the special LPDRR2 interface called extended memory interface (EMIF) of the OMAP44xx processor.

The LPDDR2-SDRAM memory is accessed via the second AHB port starting at 0x8000 0000.

Typically the LPDDR2-SDRAM initialization is performed by a boot loader or operating system following a power-on reset and must not be changed at a later point by any application code. When writing custom code independently of an operating system or boot loader, SDRAM must be initialized by accessing the appropriate SDRAM configuration registers on the OMAP44xx controller. Refer to the OMAP44xx Reference Manual for accessing and configuring these registers.

1.6.2 NAND Flash Memory (U4)

Use of Flash as non-volatile memory on the phyCORE-OMAP44xx provides an easily reprogrammable means of code storage. The following Flash device can be used on the phyCORE-OMAP44xx:

Manufacturer	NAND Flash P/N	Density	Bus Width
Micron	MT29F1G08ABBDAH4	128 MB	8 Bit
Micron	MT29F4G08ABBDAH4	512 MB	8 Bit
Micron	MT29F8G16ADBDAH4	1 GB	16 Bit

Table 11: Compatible NAND Flash Devices

Additionally, any parts that are footprint (VFBGA) and functionally compatible with the NAND Flash devices listed above may also be used with the phyCORE-OMAP44xx.

The Flash device is programmable with 1.8 V. No dedicated programming voltage is required.

As of the printing of this manual NAND Flash devices generally have a life expectancy of at least 100,000 erase/program cycles and a data retention rate of 10 years.

The NAND Flash memory is connected to the GPMC bus.

1.6.2.1 NAND Flash Lock Control (J4)

Jumper J4 controls the block lock feature of the NAND Flash (U4). Setting this jumper to position 2 + 3 enables the block lock commands and protects or locks all blocks of the device, while position 1 + 2 or removing this jumper will disable the block lock commands. Block lock feature can only enabled or disabled at power-on of the NAND Flash device. The following configurations are possible:

NAND Flash lock state	J4
Block lock commands disabled	**1 + 2 or not mounted**
Block lock commands enabled	2 + 3

Table 12: NAND Flash Lock Control via J4[1]

1. Defaults are in **bold blue** text

1.6.3 I²C EEPROM (U2)

The phyCORE-OMAP44xx is populated with a Catalyst 24WC32C[1] non-volatile 32 kB EEPROM with I²C interface at U2. This memory can be used to store configuration data or other general purpose data. This device is accessed through I²C port 1 on the OMAP44xx. The control registers for I²C port 1 are mapped between addresses 0x4807 0000 and 0x48071FFF. Please see the OMAP44xx Reference Manual for detailed information on the registers.

Three solder jumpers are provided to set the lower address bits: J1, J2 and J3. Refer to Section 1.6.3.1 for details on setting these jumpers.

Write protection to the device is accomplished via jumper J5. Refer to Section 1.6.3.2 for further details on setting this jumper.

1.6.3.1 Setting the EEPROM Lower Address Bits (J1, J2, J3)

The 32 kB I²C EEPROM populating U2 on the phyCORE-OMAP44xx module has the capability of configuring the lower address bits A0, A1, and A2. The four upper address bits of the device are fixed at '1010' (see CAT24WC32C data sheet). The remaining three lower address bits of the seven bit I²C are configurable using jumpers J1, J2 and J3. J2 sets address bit A0, J1 address bit A1, and J3 address bit A2.

Table 13 below shows the resulting seven bit I²C device address for the eight possible jumper configurations.

U2 I²C Device Address	J3	J1	J2
1010 000	**1 + 2**	**1 + 2**	**1 + 2**
1010 001	1 + 2	1 + 2	2 + 3
1010 010	1 + 2	2 + 3	1 + 2
1010 011	1 + 2	2 + 3	2 + 3
1010 100	2 + 3	1 + 2	1 +2
1010 101	2 + 3	1 + 2	2 + 3
1010 110	2 + 3	2 + 3	1 + 2
1010 111	2 + 3	2 + 3	2 + 3

Table 13: U2 EEPROM I²C Address via J1, J2, and J3[1]

1. Defaults are in **bold blue** text

1.6.3.2 EEPROM Write Protection Control (J5)

Jumper J5 controls write access to the EEPROM (U2) device. Closing this jumper allows write access to the device, while removing this jumper will cause the EEPROM to enter write protect mode, thereby disabling write access to the device.

The following configurations are possible:

EEPROM Write Protection State	J5
Write access allowed	**closed**
Write protected	open

Table 14: EEPROM Write Protection States via J5[1]

1. Defaults are in **bold blue** text
1. See the manufacturer's data sheet for interfacing and operation

1.6.4 Memory Model

There is no special address decoding device on the phyCORE-OMAP44xx, which means that the memory model is given according to the memory mapping of the OMAP44xx. Please refer to the OMAP44xx Reference Manual for more information on the memory mapping.

1.7 SD / MMC Card Interfaces

The phyCORE-OMAP44xx features two dedicated SD / MMC Card interface (SDMMC1 and SDMMC5). On the phyCORE-OMAP44xx the interface signals extend from the controllers first and fifth Secure Digital Host Controller to the phyCORE-Connector. Table 15 and Table 16 show the location of the different interface signals on the phyCORE-Connector. The Secure Digital Host Controllers are fully compatible with the SD Card Specification 2.0 and SD I/O Specification 2.0. The SDMMC1 host controller supports up to 8 data channels with a maximum data rate of 384 Mbps (768 Mbps in 8-bit MMC DDR mode), the SDMMC5 host controller supports up to 4 data channels with a maximum data rate of 384 Mbps (refer to the OMAP44xx Reference Manual for more information). The SDMMC1 host controller is supplied by the VCC_MMC1 voltage, which is generated by the PMIC TWL6030. Configuring the PMIC via I^2C interface I2C1 allows to switch VCC_MMC1 from 3 V (default) to 1.8 V.

VCC_MMC1 is also available as reference voltage on pin X1B18 of the phyCORE-Connector. Please consider the maximum load allowed for the reference voltage VCC_MMC1 to avoid any disfunction or damage of the module. The maximum load is 150 mA.

Because of compatibility reasons a card detect signal (X_PMIC_MMC1_CD) is added to the SDMMC1 Card Interface. This signal connects to the MMC input pin of the PMIC TWL6030 (U5), which can control the state of the SDMMC1 supply voltage VCC_MMC1.

Pin #	Signal	I/O	SL	Description
X1A19	X_SDMMC1_CMD	I/O	VCC_MMC1	SDMMC1 command
X1A20	X_SDMMC1_CLK	O	VCC_MMC1	SDMMC1 clock
X1A21	X_SDMMC1_DAT0	I/O	VCC_MMC1	SDMMC1 data bit 0
X1A23	X_SDMMC1_DAT1	I/O	VCC_MMC1	SDMMC1 data bit 1
X1A24	X_SDMMC1_DAT2	I/O	VCC_MMC1	SDMMC1 data bit 2
X1A25	X_SDMMC1_DAT3	I/O	VCC_MMC1	SDMMC1 data bit 3
X1A26	X_SDMMC1_DAT4	I/O	VCC_MMC1	SDMMC1 data bit 4
X1A28	X_SDMMC1_DAT5	I/O	VCC_MMC1	SDMMC1 data bit 5
X1A29	X_SDMMC1_DAT6	I/O	VCC_MMC1	SDMMC1 data bit 6
X1A30	X_SDMMC1_DAT7	I/O	VCC_MMC1	SDMMC1 data bit 7
X1B27	X_PMIC_MMC1_CD	I	1.8 V	SDMMC1 card insertion and extraction detection
X1B18	VCC_MMC1	-	-	SDMMC1 reference voltage

Table 15: Location of SD/ MMC Card Interface Signals (SDMMC1)

Pin #	Signal	I/O	SL	Description
X1B20	X_SDMMC5_CMD	I/O	1.8 V / VCC_1V8_IO	SDMMC5 command
X1B21	X_SDMMC5_CLK	O	VCC_1V8_IO	SDMMC5 clock
X1B22	X_SDMMC5_DAT0	I/O	1.8 V / VCC_1V8_IO	SDMMC5 data bit 0
X1B23	X_SDMMC5_DAT1	I/O	1.8 V / VCC_1V8_IO	SDMMC5 data bit 1
X1B25	X_SDMMC5_DAT2	I/O	1.8 V / VCC_1V8_IO	SDMMC5 data bit 2
X1B26	X_SDMMC15_DAT3	I/O	1.8 V / VCC_1V8_IO	SDMMC5 data bit 3

Table 16: Location of SD/ MMC Card Interface Signals (SDMMC5)

Note:

The signal level of the SD / MMC card interface SDMMC5 is 1.8 V. Thus integration of an SD / MMC card slot on custom target hardware requires level shifters supplied with VCC_1V8_IO (X1B30) at one of the supply rails. Please take care to not load the reference voltage VCC_1V8_IO too heavily to avoid any disfunction or damage of the module. The maximum load is 400 mA.

1.8 Serial Interfaces

The phyCORE-OMAP44xx provides numerous serial interfaces some of which are equipped with a transceiver to allow direct connection to external devices:

1. Three high speed UART interfaces (UART1, UART2 and UART4) with up to 3.6 Mbps at TTL level. One of them (UART2) provides hardware flow control (RTS and CTS signals)
2. One high speed UART interfaces (UART3) connected to an on-board RS-232 transceiver and thus available at RS-232 level. It also provides hardware flow control (RTS and CTS signals)
3. High speed USB OTG transceiver supporting the OMAP44xx USB OTG interface
4. High speed USB HOST transceiver supporting the OMAP44xx USB Host interface
5. Full speed IC-USB HOST controller supporting the OMAP44xx USB Host interchip interface
6. Auto-MDIX enabled 10/100 Ethernet interface implemented with an Ethernet controller attached to the OMAP44xx GPMC interface
7. ThreeI^2C interfaces
8. One Serial Peripheral Interface (SPI) interface
9. One Multichannel buffered serial port (McBSP) interface
10. One Multichannel audio serial port (McASP) interface

The following sections of this chapter detail each of these serial interfaces and any applicable configuration jumpers.

Caution:

Please pay special attention to the Signal Level (SL) column in the following tables. Some of the serial interfaces signal level is VCC_1V8_IO, which is 1.8 V and which is not identical with the voltage level of the primary supply voltage of the phyCORE-OMAP44xx. When connecting these interfaces to external devices level shifters supplied with VCC_1V8_IO (X1B30) at one of the supply rails should be used. Please take care to not load the reference voltage VCC_1V8_IO too heavily to avoid any disfunction or damage of the module. The maximum load is 400 mA.

1.8.1 Universal Asynchronous Interface

The phyCORE-OMAP44xx provides four high speed universal asynchronous interfaces with up to 3.6 Mbps. Two of them (UART2 and UART 3) support hardware flow control (RTS and CTS signals).

The signals of UART1, UART2 and UART4 extend directly to the phyCORE-Connector providing signals at TTL level.

UART3 of the OMAP44xx is connected to an RS-232 transceiver at U3. Thus it is possible to connect RS-232 compliant devices directly to the phyCORE-OMAP44xx. The configuration of the transceiver on the phyCORE-OMAP44xx allows for error detection by having the inputs FORCEON and /FORCEOFF connected to the /INVALID output. The transceiver is thus shut down when no valid receiver level is detected. For custom configurations which do not require RS-232 level translation, the RS-232 transceiver at U3 can be removed and 0 Ohm resistor network RN1 can be populated. In this configuration there is a direct short between the TTL level signal name (e.g. UART3_RX) and RS-232 level signal name (e.g. X_UART3_RS232_RX), leaving the RS-232 level signal names operating at TTL levels. The following table shows the location of the signals on the phyCORE-Connector.

Pin #	Signal	I/O	SL	Description
X1C10	X_UART1_TX	O	VCC_1V8_IO	Serial transmit signal UART1
X1D10	X_UART1_RX	I	1.8 V	Serial data receive signal UART 1
X1D11	X_UART3_RS232_TX	O	RS-232	Serial transmit signal UART 3
X1D12	X_UART3_RS232_RX	I	RS-232	Serial data receive signal UART 3
X1C12	X_UART3_RS232_CTS	I	RS-232	Serial clear to send UART 3
X1C13	X_UART3_RS232_RTS	O	RS-232	Serial request to send UART 3
X1D13	X_UART2_TX	O	VCC_1V8_IO	Serial transmit signal UART 2
X1D15	X_UART2_RX	I	1.8 V	Serial data receive signal UART 2
X1C14	X_UART2_CTS	I	1.8 V	Serial clear to send UART 2
X1C15	X_UART2_RTS	O	VCC_1V8_IO	Serial request to send UART 2
X1D16	X_UART4_TX	O	VCC_1V8_IO	Serial transmit signal UART 4
X1D17	X_UART4_RX	I	1.8 V	Serial data receive signal UART 4

Table 17: Location of the UART Signals

1.8.2 USB OTG Interface

The phyCORE-OMAP44xx provides a high speed USB OTG interface which uses the OMAP44xx embedded HS USB OTG PHY. Since the integrated PHY does not support the OTG features ID pin detection and V_{BUS} detection, these features are implemented using the on-board PMIC TWL6030. An external USB Standard-A (for USB host), USB Standard-B (for USB device), or USB mini-AB (for USB OTG) connector is all that is needed to interface the phyCORE-OMAP44xx USB OTG functionality. The applicable interface signals can be found on the phyCORE-Connector as shown in Table 18.

Pin #	Signal	I/O	SL	Description
X1C19	X_USB_OTG_DP	I/O	USB	USB OTG data plus
X1C20	X_USB_OTG_DM	I/O	USB	USB OTG data minus
X1C22	X_PMIC_USB_OTG_ID	I/O	USB	USB OTG connector identification signal
X1C23	X_PMIC_USB_OTG_VBUS	I	USB	USB OTG V_{BUS} detection input

Table 18: Location of the USB OTG Signals

1.8.3 USB Host Transceiver (U8)

The phyCORE-OMAP44xx is populated with an SMSC USB3320 USB High-Speed transceiver (U8) supporting the high speed data rates of the OMAP44xx. The USB3320 is connected to the first Host Controller's ULPI interface (USBB1) on the OMAP44xx. An external USB Standard-A (for USB host) connector is all that is needed to interface the phyCORE-OMAP44xx USB Host functionality. The applicable interface signals (D+/D-/ PWR/OC) can be found on the phyCORE-Connector. Since the USB3320 doesn't have an overcurrent input, this signal is connected to GPIO 120 of the OMAP44xx.

Pin #	Signal	I/O	SL	Description
X1D18	X_USBB1_OC_GPIO_120	I	1.8 V	USB Host overcurrent signal input
X1D20	X_USBB1_DP	I/O	USB	USB Host data plus
X1D21	X_USBB1_DM	I/O	USB	USB Host data minus
X1D22	X_USBB1_PWR	O	3.3 V (VCC_3V3_S)	External USB supply voltage (5 V) enable (to control an external power switch)

Table 19: Location of the USB Host Signals

The USB3320 USB High-Speed transceiver (U8) is supplied by the switchable 3.3 V voltage domain (VCC_3V3_S) which is also available at the reference voltage output pin X1D23 on the phyCORE-Connector.

To fully support V_{BUS} power control using an external V_{BUS} switch the phyCORE-OMAP44xx provides the control signal X_USBB1_PWR (X1D22). It can be used to switch an external V_{BUS} power supply and is derived from the USB High-Speed transceiver's CPEN signal[1] (refer to the USB3320 datasheet for more information).

1. Removing R34 and mounting Q5 and R21 allows to also generate this signal by GPIO 119 of the OMAP44xx if needed. Please contact our sales team for more details.

1.8.4 Full-Speed IC USB Host interface

The full-speed IC USB Host interface of the phyCORE-OMAP44xx is directly connected to the embedded full-speed USB host controller (USBC1) of the OMAP44xx which supports a single universal serial bus (USB) host port with an USB interchip intended for direct chip to chip communication. It complies with the USB 2.0 standard. The IC USB Host controller supports USB 2.0 full-speed and low-speed operations. As only two of the four signals are brought out on the phyCORE-Connector, only the 2-pin mode is usable. The applicable interface signals can be found on the phyCORE-Connector X1 as shown in Table 20.

Pin #	Signal	I/O	SL	Description
X1C17	X_USBC1_ICUSB_DP	I/O	USB	Interchip USB host data plus
X1C18	X_USBC1_ICUSB_DM	I/O	USB	Interchip USB host data minus

Table 20: Location of the IC USB Host Signals

1.8.5 Ethernet Interface

Connection of the phyCORE-OMAP44xx to the world wide web or a local area network (LAN) is possible using the on-board FEC (Fast Ethernet Controller) SMSC LAN9221 at U12. It is connected to the GPMC interface of the OMAP44xx. The FEC operates with a data transmission speed of 10 Mbit/s or 100 Mbit/s.

1.8.5.1 Ethernet Controller (U12)

With an Ethernet controller mounted at U12 the phyCORE-OMAP44xx has been designed for use in 10Base-T and 100Base-T networks. The 10/100Base-T interface with its LED signals extends to phyCORE-Connector X1.

Pin #	Signal	I/O	SL	Description
X1C24	X_ETH_TX+	O	3.3 V (VCC_3V3_S)	Ethernet transmit positive output
X1C25	X_ETH_TX-	O	3.3 V (VCC_3V3_S)	Ethernet transmit negative output
X1C27	X_ ETH_SPEED	O	3.3 V (VCC_3V3_S)	Ethernet Speed Indicator (open drain)
X1D25	X_ETH_RX+	I	3.3 V (VCC_3V3_S)	Ethernet receive positive input
X1D26	X_ETH_RX-	I	3.3 V (VCC_3V3_S)	Ethernet receive negative input
X1D27	X_ETH_LINK	O	3.3 V (VCC_3V3_S)	Ethernet link indicator (open drain)
X1C44	X_PEMIC_PREQ2A	O/I	VCC_1V8_IO / 1.8 V	Ethernet controller power management event signal (PME) / PMIC peripheral 2A power request input

Table 21: Location of the Ethernet Signals

The Ethernet controller's integrated PHY supports HP Auto-MDIX technology, eliminating the need for the consideration of a direct connect LAN cable, or a cross-over patch cable. It detects the TX and RX pins of the

connected device and automatically configures the PHY TX and RX pins accordingly. The Ethernet controller also provides wake on LAN and other power management modes. To integrate the power management features of the Ethernet controller into the application's power management concept the power management event signal (PME) of the LAN9221 is available at pin X1C44 of the phyCORE-Connector (please refer to the SMSC LAN9221 datasheet for further information on this signal). Utilization of this signal allows to wake-up the application by a power management circuitry on the custom target hardware. The PEM signal is also connected to the Peripheral 2A Power Request input (PREQ2A) of the PMIC TWL6030. Consequently it is also possible to interpret the signal on the phyCORE-OMAP44xx without the need to design an external power management circuitry [1]. If pin X1C44 of the phyCORE-OMAP44xx, or the Peripheral 2A Power Request input (PREQ2A) of the PMIC TWL6030 are intend for a different function de-soldering of resistor R69 and mounting of resistor R70 disconnects the PME signal from the phyCORE-Connector and PREQ2A and connects it to the Peripheral 2B Power Request input (PREQ2B) of the PMIC TWL6030 instead.

The Ethernet controller is connected to chip select CS5 of the General-Purpose Memory Controller (GPMC). The start address for CS5 is configurable (e.g. for the Phytec Linux BSP the start address is set to 0x2C00 0000). Please refer to the OMAP44xx Reference Manual for more information on how to configure the address space for CS5 etc.

Connecting the phyCORE-OMAP44xx to an existing 10/100Base-T network involves adding an RJ45 and appropriate magnetic devices in your design. The required 49,9 Ohm +/-1% termination resistors on the analog signals (ETH_RX±, ETH_TX±) are already populated on the module. Connection to an external Ethernet magnetics should be done using very short signal traces. The TPI+/TPI- and TPO+/TPO- signals should be routed as 100 Ohm differential pairs. The same applies for the signal lines after the transformer circuit. The carrier board layout should avoid any other signal lines crossing the Ethernet signals.

If a power management is implemented which allows to turn off the Ethernet controller's supply voltage VCC_3V3_S special care must be taken to avoid a reverse current over the terminating resistors. In this case the reference voltage VCC_3V3_S which is available at pin X1D23 of the phyCORE-Connector should be used to switch off any supply voltage attached to the center tap of the magnetics located on the target hardware. Please consult the phyCORE-OMAP44xx Carrier Board schematics as a reference.

If you are using the applicable carrier board for the phyCORE-OMAP44xx (part number PCM-959), the external circuitry mentioned above is already integrated on the board (refer to Section 2.1.3.4).

Caution:

Please see the datasheet of the Ethernet controller when designing the Ethernet transformer circuitry.

1.8.5.2 MAC Address EEPROM (U13)

In a computer network such as a local area network (LAN), the MAC (Media Access Control) address is a unique computer hardware number. For a connection to the Internet, a table is used to convert the assigned IP number to the hardware's MAC address.

In order to guarantee that the MAC address is unique, all addresses are managed in a central location. PHYTEC has acquired a pool of MAC addresses. The MAC address of the phyCORE-OMAP44xx is located on the bar code sticker attached to the module. This number is a 12-digit HEX value.

An EEPROM at U13 is used to store the MAC address.

1. All special functions of the PMIC such as use of PREQ2A, etc. require the PMIC to be programmed via I^2C interface. At the time of delivery only the generation of the required voltages is implemented . Please refer to the TWL6030 Technical Ref. Man. for more information on how to program the PMIC.

1.8.6 I²C Interface

The Inter-Integrated Circuit (I²C) interface is a two-wire, bidirectional serial bus that provides a simple and efficient method for data exchange among devices. The OMAP44xx contains 4 identical and independent I²C modules. The interface of the first, third and fourth module are available on the phyCORE-Connector. The first module connects also to the on-board EEPROM (refer to Section 1.6.3) and to the PMIC TWL6030 (refer to Section 1.4.3). The following table lists the I²C ports on the phyCORE-Connector.

Pin #	Signal	I/O	SL	Description
X1C53	X_I2C1_SCL	O	VCC_1V8_IO	I2C1 clock (open drain)
X1C54	X_I2C1_SDA	I/O	1.8 V / VCC_1V8_IO	I2C1 data (open drain)
X1D51	X_I2C3_SCL	O	VCC_1V8_IO	I2C3 clock (open drain)
X1D52	X_I2C3_SDA	I/O	1.8 V / VCC_1V8_IO	I2C3 data (open drain)
X1A18	X_I2C4_SDA	I/O	1.8 V / VCC_1V8_IO	I2C4 data (open drain)
X1B17	X_I2C4_SCL	O	VCC_1V8_IO	I2C4 clock (open drain)

Table 22: I²C Interface Signal Location

To avoid any conflicts when connecting external I²C devices to the first I²C module of the OMAP44xx the addresses of the on-board I²C devices must be considered. Table 23 lists the addresses already in use. The addresses of the EEPROM can be configured by jumpers. The table shows only the default addresses. Please refer to Section 1.6.3.1 for alternative address settings.

I²C Interface	Connected Devices	I²C Address (standard) (7 MSB)	Maximum Speed
I2C1	EEPROM	0x50	400 kHz
I2C1	PMIC	0x48, 0x49, 0x4A	400 kHz

Table 23: I²C Addresses in Use

1.8.7 SPI Interface

The Serial Peripheral Interface (SPI) interface is a four-wire, bidirectional synchronous serial bus that provides a simple and efficient method for data exchange among devices. The multichannel serial port interfaces (McSPI) of the OMAP44xx has four separate modules (SPI1, SPI2, SPI3, and SPI4). The interface signals of the first module (McSPI1) are made available on the phyCORE-Connector. This module is Master/Slave configurable and supports up to four peripherals. The following table lists the SPI signals on the phyCORE-Connector:

Pin #	Signal	I/O	SL	Description
X1A31	X_SPI1_CS0	I/O	1.8 V / VCC_1V8_IO	McSPI1 chip select 0 (slave input, master output)
X1B31	X_SPI1_CS1	O	VCC_1V8_IO	McSPI1 chip select 1
X1B32	X_SPI1_CS2	O	VCC_1V8_IO	McSPI1 chip select 2
X1A33	X_SPI1_CS3	O	VCC_1V8_IO	McSPI1 chip select 3
X1B33	X_SPI1_MOSI	I/O	1.8 V / VCC_1V8_IO	McSPI1 master output / slave input
X1A34	X_SPI1_MISO	I/O	1.8 V / VCC_1V8_IO	McSPI1 master input/ slave output
X1B34	X_SPI1_CLK	I/O	1.8 V / VCC_1V8_IO	McSPI1 clock master output/ slave input

Table 24: SPI Interface Signal Location

1.8.8 Multichannel Buffered Serial Port (McBSP)

The Multichannel Buffered Serial Port (McBSP) interface of the phyCORE-OMAP44xx is a full-duplex, serial port that allows to communicate with a variety of serial devices in a system such as other application chips (digital base band), audio and voice codecs,etc. The McBSP supports a direct interface to industry-standard codecs, analog interface chips (AICs) and other serially connected A/D and D/A devices, such as Inter-IC sound (I^2S) compliant devices, pulse code modulation (PCM) devices and time devision multiplexed (TDM) bus devices. The OMAP44xx controller offers four instances of the McBSP module. The interface signals of the third module (McBSP3) are brought out to the phyCORE-Connector. The following table shows the location of the McBSP signals on the phyCORE-Connector.

Pin #	Signal	I/O	SL	Description
X1B28	X_McBSP3_CLKX	I/O	1.8 V / VCC_1V8_IO	ABE McBSP3 combined serial clock
X1A40	X_McBSP3_DX	I/O	1.8 V / VCC_1V8_IO	ABE McBSP3 transmitted serial data
X1B41	X_McBSP3_FSX	I/O	1.8 V / VCC_1V8_IO	ABE McBSP3 combined frame synchronization
X1B42	X_McBSP3_DR	I	1.8 V	ABE McBSP3 received serial data

Table 25: McBSP Signal Location

1.8.9 Multichannel Audio Serial Port (McASP)

The multichannel audio serial port (McASP) interface of the phyCORE-OMAP44xx is a general audio serial port optimized for the requirements of various audio applications. The McASP is useful for intercomponent digital audio interface transmission (DIT). It has the flexibility to gluelessly connect to a Sony/Philips digital interface (S/PDIF) transmit physical layer component. The McASP module operates in transmit mode only; it has no receive capabilities.

Pin #	Signal	I/O	SL	Description
X1A35	X_McASP_AXR	O	VCC_1V8_IO	ABE McASP serial data IO
X1A36	X_McASP_AFSX	O	VCC_1V8_IO	ABE McASP frame synchronization transmit
X1B37	X_McASP_AHCLKX	O	VCC_1V8_IO	ABE McASP high frequency clock output
X1B38	X_McASP_AMUTE	O	VCC_1V8_IO	ABE McASP auto mute output
X1A39	X_McASP_AMUTEIN	I	1.8 V	ABE McASP auto mute input
X1A41	X_McASP_ACLKX	O	VCC_1V8_IO	ABE McASP clock transmit

Table 26: Multichannel Audio Serial Port (McASP) Signal Location

1.9 General Purpose I/Os

The phyCORE-OMAP44xx provides 3 GPIOs[1]. Beside these 3 dedicated GPIOs, most of the OMAP44xx signals which are connected directly to the module connector can be configured to act as GPIOs, due to the multiplexing functionality of most controller pins. The GPIO pins can be used as data input with an optional and configurable debounce cell or data output. Furthermore the pins support an interrupt generation in active mode and wake-up request generation in idle mode upon the detection of external events. With the pad configuration feature of the OMAP44xx, you can also configure the GPIO to optionally have a pull-up or pull-down. Table 27 shows the location of the dedicated GPIO pins on the phyCORE-Connector, as well as the corresponding ports of the OMAP44xx.

Pin #	Signal	I/O	SL	Description
X1A38	X_GPIO_115	I/O	1.8 V / VCC_1V8_IO	GPIO 115
X1B39	X_GPIO_114	I/O	1.8 V / VCC_1V8_IO	GPIO 114
X1D28	X_GPIO_WK30	I/O	1.8 V / VCC_1V8_IO	GPIO WK30

Table 27: Location of Dedicated GPIO Pins

As can be seen in the table above the voltage level is VCC_1V8_IO. To avoid mismatch of different voltage levels external devices connected to these pins should be supplied by the reference voltage VCC_1V8_IO. The IO reference voltage (VCC_1V8_IO) is available at X1B30 (refer to Section 1.4.4). Alternatively an open drain circuit with a pull-up resistor attached to VCC_1V8_IO can be connected to the GPIOs of the phyCORE-OMAP44xx.

Caution:

Please take care to not load the reference voltage VCC_1V8_IO too heavily to avoid any disfunction or damage of the module. The maximum load is 400 mA.

1. To support all features of the phyCORE-OMAP44xx Carrier Board special functions have been assigned to the GPIOs in the BSP delivered with the module. In order to otherwise utilize the GPIOs the software must be changed. Table 42 lists the functions assigned to the GPIO pins.

1.10 Debug Interface (X7)

The phyCORE-OMAP44xx is equipped with a JTAG interface for downloading program code into the external flash, internal controller RAM or for debugging programs currently executing. The JTAG interface extends to a 2.0 mm pitch pin header at X7 on the edge of the module PCB and also to the phyCORE-Connector X1. Figure 9 and Figure 10 show the position of the debug interface (JTAG connector X7) on the phyCORE-OMAP44xx module. Even numbered pins are on the top of the module, starting with 2 on the right to 20 on the left, while odd number pins are on the bottom, starting from (as viewed from the top) 1 on the right to 19 on the left.

The JTAG edge card connector X7 provides an easy means of debugging the phyCORE-OMAP44xx in your target system via an external JTAG probe.

Note:

The JTAG connector X7 only populates phyCORE-OMAP44xx modules with order code PCM-049-xxxxxxxJxx. This version of the phyCORE module must be special ordered. The JTAG connector X7 is not populated on phyCORE modules included in the Rapid Development Kit. All JTAG signals are accessible from the carrier board. The JTAG signals are also accessible at the phyCORE-Connector X1 (Samtec connectors). We recommend integration of a standard (2.54 mm pitch) pin header connector in the user target circuitry to allow easy program updates via the JTAG interface. See Table 29 for details on the JTAG signal pin assignment.

Table 28 shows the pin assignment of the JTAG connector X7. The location of the JTAG signals on the phyCORE-Connector X1 is shown in Table 29.
PHYTEC offers a JTAG-Emulator adapter (order code JA-002) for connecting the phyCORE-OMAP44xx to a standard emulator. The JTAG-Emulator adapter extends the signals of the module's JTAG connector to a standard ARM connector with 2 mm pin pitch. The JA-002 therefore functions as an adapter for connecting the module's non-ARM-compatible JTAG connector X7 to standard Emulator connectors.

Signal	Pin Row[1]		Signal
	A	B	
VCC_1V8_IO	2	1	TREF (VCC_1V8_IO via 100 Ohm)
GND	4	3	X_JTAG_nTRST
GND	6	5	X_JTAG_TDI
GND	8	7	X_JTAG_TMS
GND	10	9	X_JTAG_TCK
GND	12	11	X_JTAG_RTCK
GND	14	13	X_JTAG_TDO
GND	16	15	X_nRESET_WARM
GND	18	17	X_DPM_EMU0
GND	20	19	X_DPM_EMU1

Table 28: JTAG Connector X7 Signal Assignment
1. Note: Row A is on the controller side of the module and Row B is on the connector side of the module

Pin #	Signal	I/O	SL	Description
X1C28	X_JTAG_TDO	O	VCC_1V8_IO	JTAG test data output
X1C29	X_JTAG_TMS	I/O	1.8 V / VCC_1V8_IO	JTAG test mode select
X1C30	X_JTAG_TCK	I	1.8 V	JTAG test clock input
X1D31	X_JTAG_nTRST	I	1.8 V	JTAG test reset
X1C32	X_JTAG_TDI	I	1.8 V	JTAG test data input
X1D32	X_JTAG_RTCK	O	VCC_1V8_IO	JTAG ARM clock emulation
X1C33	X_DPM_EMU1	I/O	1.8 V / VCC_1V8_IO	Debug pin manager pin 1
X1D33	X_DPM_EMU0	I/O	1.8 V / VCC_1V8_IO	Debug pin manager pin 0

Table 29: Location of the JTAG Signals on the phyCORE-Connector X1

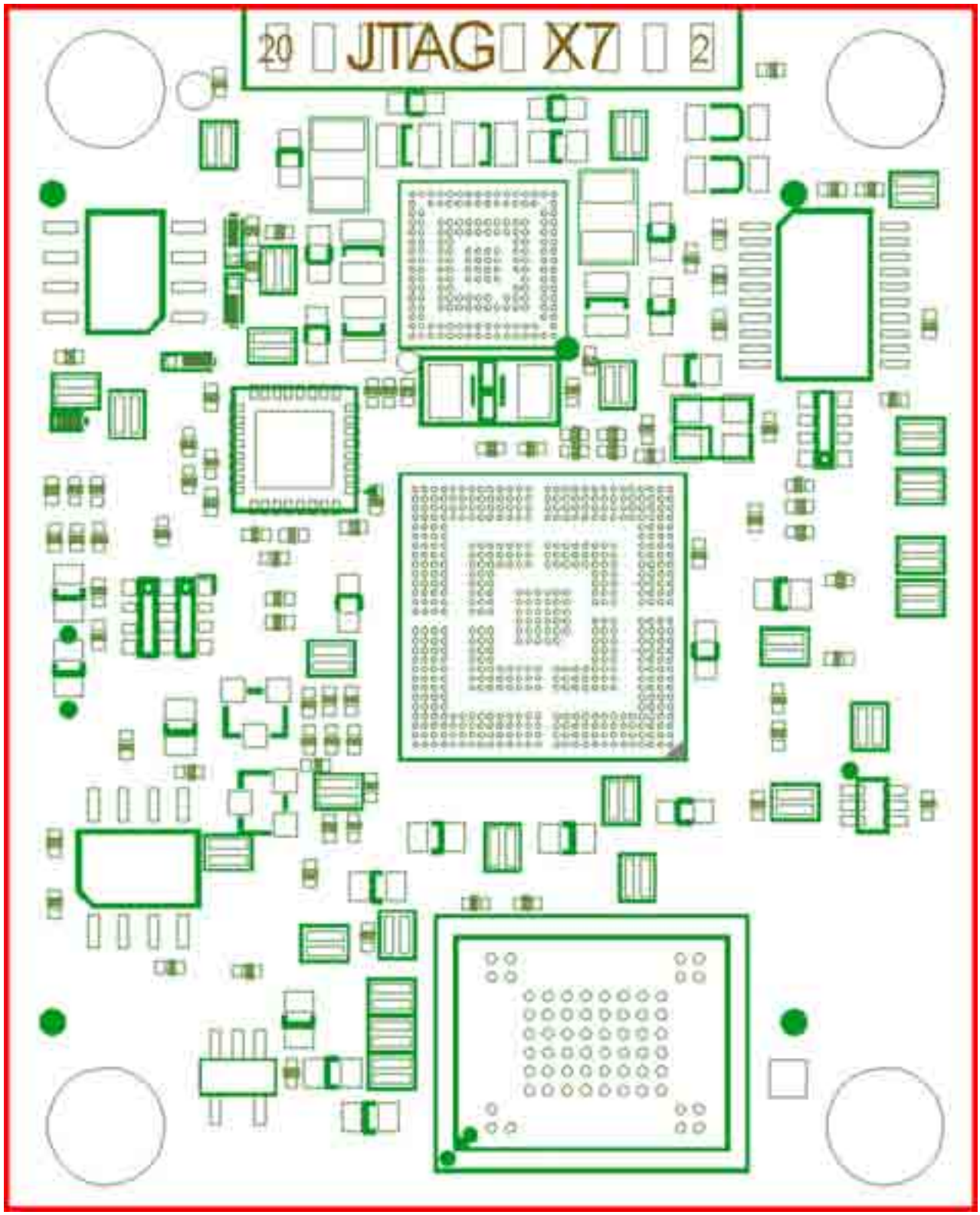


Figure 9: JTAG Interface at X7 (top view)

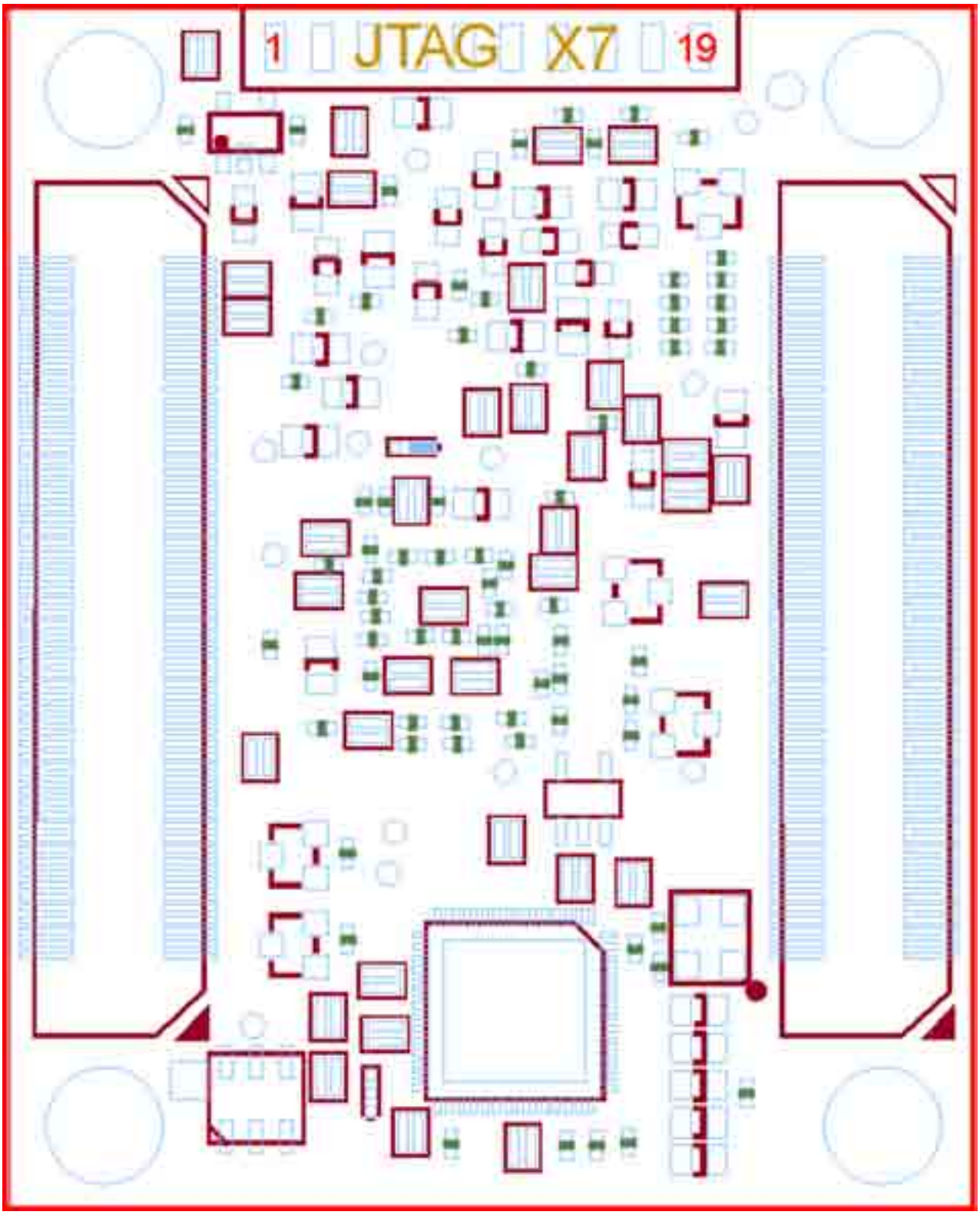


Figure 10: JTAG Interface at X7 (bottom view)

1.11 Display Interfaces

The phyCORE-OMAP44xx provides three different display interfaces:

1. Parallel Display Interface
2. MIPI® Display Serial Interface (DSI)
3. High-Definition Multimedia Interface (HDMI)

1.11.1 Parallel Display Interface

The 24-bit parallel display interface (DISPC) of the OMAP44xx is directly connected to the phyCORE-Connector. The location of the applicable interface signals can be found in the table below. Signal X_DMTIMER9 can be used as PWM output to control the display brightness. In order to use the PWM output jumper J6 must be closed in the default position at 1+2. Refer also to Section 1.3.

Pin #	Signal	I/O	SL	Description
X1A43	X_DMTIMER9	O	VCC_1V8_IO	PWM output (can be used for display brightness control)
X1B43	X_DISPC_DATA23	O	VCC_1V8_IO	DISPC data bit 23
X1A44	X_DISPC_DATA22	O	VCC_1V8_IO	DISPC data bit 22
X1B44	X_DISPC_DATA21	O	VCC_1V8_IO	DISPC data bit 21
X1A45	X_DISPC_DATA20	O	VCC_1V8_IO	DISPC data bit 20
X1A46	X_DISPC_DATA19	O	VCC_1V8_IO	DISPC data bit 19
X1B46	X_DISPC_DATA18	O	VCC_1V8_IO	DISPC data bit 18
X1B47	X_DISPC_DATA17	O	VCC_1V8_IO	DISPC data bit 17
X1A48	X_DISPC_DATA16	O	VCC_1V8_IO	DISPC data bit 16
X1B48	X_DISPC_DATA15	O	VCC_1V8_IO	DISPC data bit 15
X1A49	X_DISPC_DATA14	O	VCC_1V8_IO	DISPC data bit 14
X1B49	X_DISPC_DATA13	O	VCC_1V8_IO	DISPC data bit 13
X1A50	X_DISPC_DATA12	O	VCC_1V8_IO	DISPC data bit 12
X1B50	X_DISPC_DATA11	O	VCC_1V8_IO	DISPC data bit 11
X1A51	X_DISPC_DATA10	O	VCC_1V8_IO	DISPC data bit 10
X1B52	X_DISPC_DATA9	O	VCC_1V8_IO	DISPC data bit 9
X1A53	X_DISPC_DATA8	O	VCC_1V8_IO	DISPC data bit 8
X1B53	X_DISPC_DATA7	O	VCC_1V8_IO	DISPC data bit 7
X1A54	X_DISPC_DATA6	O	VCC_1V8_IO	DISPC data bit 6
X1B54	X_DISPC_DATA5	O	VCC_1V8_IO	DISPC data bit 5
X1A55	X_DISPC_DATA4	O	VCC_1V8_IO	DISPC data bit 4
X1B55	X_DISPC_DATA3	O	VCC_1V8_IO	DISPC data bit 3
X1A56	X_DISPC_DATA2	O	VCC_1V8_IO	DISPC data bit 2
X1B57	X_DISPC_DATA1	O	VCC_1V8_IO	DISPC data bit 1
X1A58	X_DISPC_DATA0	O	VCC_1V8_IO	DISPC data bit 0
X1B58	X_DISPC_HSYNC	O	VCC_1V8_IO	DISPC horizontal synchronization
X1A59	X_DISPC_PCLK	O	VCC_1V8_IO	DISPC LCD pixel clock
X1B59	X_DISPC_VSYNC	O	VCC_1V8_IO	DISPC vertical synchronization
X1A60	X_DISPC_DE	O	VCC_1V8_IO	DISPC data enable

Table 30: Parallel Display Interface Signal Location

1.11.2 MIPI Display Serial Interface (DSI)

The phyCORE-OMAP44xx provides a MIPI® display serial interface (DSI1) module, which connects to a DSI display module directly or through an external DSI bridge like the Toshiba TC358764/65 DSI2LVDS (D2L) bridge chip. DSI is a protocol based bidirectional differential serial interface. The phyCORE-OMAP44xx provides up to 4 data lanes with a maximum data rate of 824 Mbps and one clock lane.

Pin #	Signal	I/O	SL	Description
X1C46	X_DSI1_DX0	O	DSI	DSI1 display lane 0 differential positive or negative [1]
X1C47	X_DSI1_DY0	O	DSI	DSI1 display lane 0 differential positive or negative [1]
X1D46	X_DSI1_DX1	O	DSI	DSI1 display lane 1 differential positive or negative[1]
X1D47	X_DSI1_DY1	O	DSI	DSI1 display lane 1 differential positive or negative [1]
X1C48	X_DSI1_DX2	O	DSI	DSI1 display lane 2 differential positive or negative [1]
X1C49	X_DSI1_DY2	O	DSI	DSI1 display lane 2 differential positive or negative [1]
X1D48	X_DSI1_DX3	O	DSI	DSI1 display lane 3 differential positive or negative [1]
X1D49	X_DSI1_DY3	O	DSI	DSI1 display lane 3 differential positive or negative [1]
X1C51	X_DSI1_DX4	O	DSI	DSI1 display lane 4 differential positive or negative [1]
X1C52	X_DSI1_DY4	O	DSI	DSI1 display lane 4 differential positive or negative [1]

Table 31: DSI Signal Location

1. Can be configured by setting the appropriate control register. Please refer to the OMAP44xx Reference manual for more information.

1.11.3 High-Definition Multimedia Interface (HDMI)

The High-definition multimedia interface (HDMI) of the phyCORE-OMAP44xx module is compliant to HDMI 1.3, HDCP 1.2 and DVI 1.0. It supports a maximum pixel clock of 148.5 MHz for a resolution of up to 1920 x 1080 @ 60 MHz. Please refer to the OMAP44xx Reference Manual for more information.

Pin #	Signal	I/O	SL	Description
X1C34	X_HDMI_HPD	I	1.8 V	HDMI display hot plug detect
X1D34	X_HDMI_CEC	I/O	1.8 V / VCC_1V8_IO	HDMI consumer electronic control
X1C35	X_HDMI_DDC_SCL	I/O	1.8 V / VCC_1V8_IO	HDMI display data channel clock (open drain)
X1D35	X_HDMI_DDC_SDA	I/O	1.8 V / VCC_1V8_IO	HDMI display data channel data (open drain)
X1C37	X_HDMI_DATA0X	O	HDMI	HDMI display data 0 differential positive or negative [1]
X1C38	X_HDMI_DATA0Y	O	HDMI	HDMI display data 0 differential positive or negative[1]
X1D37	X_HDMI_DATA1X	O	HDMI	HDMI display data 1 differential positive or negative[1]
X1D38	X_HDMI_DATA1Y	O	HDMI	HDMI display data 1 differential positive or negative [1]
X1D39	X_HDMI_DATA2X	O	HDMI	HDMI display data 2 differential positive or negative [1]
X1D40	X_HDMI_DATA2Y	O	HDMI	HDMI display data 2 differential positive or negative [1]
X1C39	X_HDMI_CLOCKX	O	HDMI	HDMI display clock differential positive or negative [1]
X1C40	X_HDMI_CLOCKY	O	HDMI	HDMI display clock differential positive or negative [1]

Table 32: HDMI Signal Location

1. Can be configured by setting the appropriate control register. Please refer to the OMAP44xx Reference manual for more information.

1.12 Camera Interfaces

The phyCORE-OMAP44xx provides two serial camera interfaces:

1. Primary camera interface (CSI2-A/CSI21)
2. Secondary camera interface (CSI2-B/CSI22)

The control signals shown in the following table can be used for both camera interface independently. Please refer to the Texas Instruments OMAP44xx Reference Manual for more information.

Pin #	Signal	I/O	SL	Description
X1B10	X_CAM_SHUTTER	O	VCC_1V8_IO	Mechanical shutter control signal
X1B11	X_CAM_GLOBAL_RESET	I/O	1.8 V / VCC_1V8_IO	Camera sensor reset
X1B12	X_CAM_STROBE	O	VCC_1V8_IO	Camera flash activation trigger

Table 33: Camera Interface Control Signal Location

1.12.1 Primary Camera Interface (CSI2-A/CSI21)

The primary camera interface (CSI2-A/CSI21) is compatible to the MIPI® Camera Serial Interface (CSI2) specification and supports 4 data lanes.

The following table shows the location of the applicable interface signals of the primary camera interfaces on the phyCORE-Connector.

Pin #	Signal	I/O	SL	Description
X1A13	X_CSI21_DX0	I	CSI	CSI2-A (CSI21) differential clock positive input
X1A14	X_CSI21_DY0	I	CSI	CSI2-A (CSI21) differential clock negative input
X1A15	X_CSI21_DX1	I	CSI	CSI2-A (CSI21) differential data lane positive input 1
X1A16	X_CSI21_DY1	I	CSI	CSI2-A (CSI21) differential data lane negative input 1
X1B15	X_CSI21_DX2	I	CSI	CSI2-A (CSI21) differential data lane positive input 2
X1B16	X_CSI21_DY2	I	CSI	CSI2-A (CSI21) differential data lane negative input 2
X1B5	X_KPD_COL4_CSI21_DX3	O/I	VCC_1V8_IO / CSI	Keyboard column 4 (open drain) / CSI2-A (CSI21) differential data lane positive input 3 (see note below)
X1B6	X_KPD_ROW4_CSI21_DY3	I	1.8 V / CSI	Keyboard row 4 / CSI2-A (CSI21) differential data lane negative input 3 (see note below)
X1B7	X_KPD_COL5_CSI21_DX4	O/I	VCC_1V8_IO / CSI	Keyboard column 5 (open drain) / CSI2-A (CSI21) differential data lane positive input 4 (see note below)
X1B8	X_KPD_ROW5_CSI21_DY4	I	1.8 V / CSI	Keyboard row 5 / CSI2-A (CSI21) differential data lane negative input 4 (see note below)

Table 34: Primary Camera Interface (CSI2-A/CSI21) Signal Location

Note:

Pins X1B5 to X1B8 on the phyCORE-Connector provide either signals of the keyboard interface, or camera lanes 3 and 4 of the primary camera interface. The resistor array JN1 allows to choose which signals are brought out at these pins. In order to use lanes 3 and 4 of the primary camera interface JN1 must be set to position 2. Please refer to Figure 6 to see where JN1 is located.

1.12.2 Secondary Camera Interface (CSI2-B/CSI22)

The secondary camera interface (CSI2-B/CSI22) supports 1 data lane and is compatible to the MIPI® Camera Serial Interface (CSI2) as well as to the SMIA Compact Camera Port 2 specification (CCP2 v1.0).

The following table shows the location of the applicable interface signals of the secondary camera interfaces on the phyCORE-Connector.

Pin #	Signal	I/O	SL	Description
X1A8	X_CSI22_DX0	I	CSI	CSI2-B (CSI22) differential clock lane positive input
X1A9	X_CSI22_DY0	I	CSI	CSI2-B (CSI22) differential clock lane negative input
X1A10	X_CSI22_DX1	I	CSI	CSI2-B (CSI22) differential data lane positive input
X1A11	X_CSI22_DY1	I	CSI	CSI2-B (CSI22) differential data lane negative input

Table 35: Secondary Camera Interface (CSI2-B/CSI22) Signal Location

1.13 Keyboard Interface

The keyboard interface of the phyCORE-OMAP44xx can handle up to 6 x 6 keys. It supports features like debouncing, wake-up event generation, multikey-press detection, programmable interrupt generation and much more. Table 36 shows the location of the keyboard signals on the phyCORE-Connector.

Pin #	Signal	I/O	SL	Description
X1A1	X_KPD_COL0	O	VCC_1V8_IO	Keyboard column 0 (open drain)
X1B1	X_KPD_COL1	O	VCC_1V8_IO	Keyboard column 1 (open drain)
X1B2	X_KPD_COL2	O	VCC_1V8_IO	Keyboard column 2 (open drain)
X1A3	X_KPD_COL3	O	VCC_1V8_IO	Keyboard column 3 (open drain)
X1B3	X_KPD_ROW0	I	1.8 V	Keyboard row 0
X1A4	X_KPD_ROW1	I	1.8 V	Keyboard row 1
X1A5	X_KPD_ROW2	I	1.8 V	Keyboard row 2
X1A6	X_KPD_ROW3	I	1.8 V	Keyboard row 3
X1B5	X_KPD_COL4_CSI21_DX3	O/I	VCC_1V8_IO / CSI	Keyboard column 4 (open drain) / CSI2-A (CSI21) differential data lane positive input 3 (see note below)
X1B6	X_KPD_ROW4_CSI21_DY3	I	1.8 V / CSI	Keyboard row 4 / CSI2-A (CSI21) differential data lane negative input 3 (see note below)
X1B7	X_KPD_COL5_CSI21_DX4	O/I	VCC_1V8_IO / CSI	Keyboard column 5 (open drain) / CSI2-A (CSI21) differential data lane positive input 4 (see note below)
X1B8	X_KPD_ROW5_CSI21_DY4	I	1.8 V / CSI	Keyboard row 5 / CSI2-A (CSI21) differential data lane negative input 4 (see note below)

Table 36: Keyboard Interface Signal Location

Note:

Pins X1B5 to X1B8 on the phyCORE-Connector provide either signals of the keyboard interface, or camera lanes 3 and 4 of the primary camera interface. The resistor array JN1 allows to choose which signals are brought out at these pins. The default setting of JN1 at position 1 allows to use the keyboard interface without changes. Please refer to Table 6 for more information on JN1.

1.14 User LEDs

The phyCORE-OMAP44xx provides two user LEDs on board, a red (D2) and a green (D3). The LEDs can be controlled by setting GPIO 152 (D2) and GPIO 153 (D3) to the desired output level. A high-level turns the LED on, a low-level turns it off.

1.15 Technical Specifications

The physical dimensions of the phyCORE-OMAP44xx are represented in Figure 11 . The module's profile is max. **5.0 mm** thick, with a maximum component height of **1.5 mm** on the bottom (connector) side of the PCB and approximately **2.0 mm** on the top (microcontroller) side. The board itself is approximately **1.5 mm** thick.

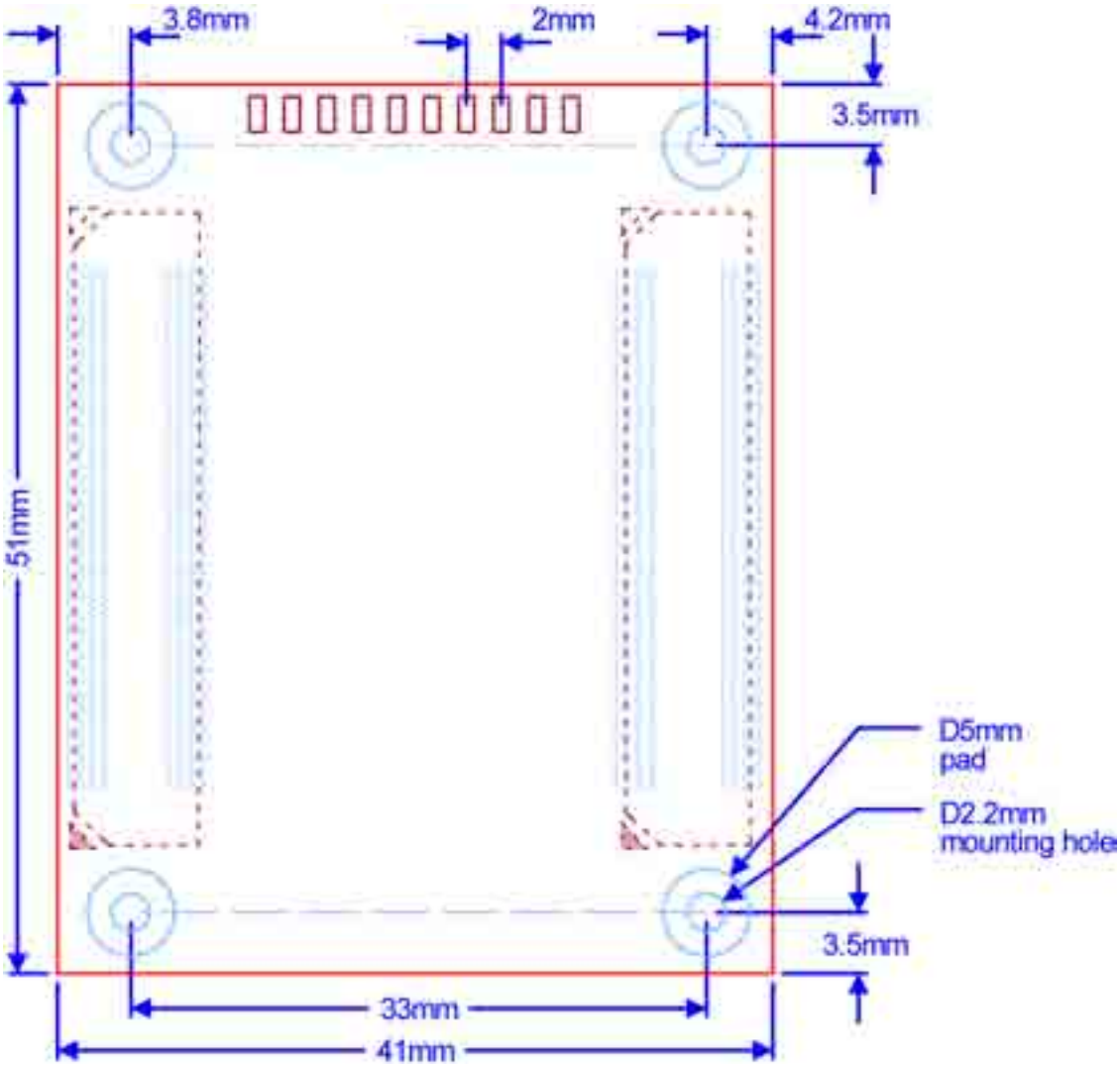


Figure 11: Physical Dimensions

Note:

To facilitate the integration of the phyCORE-OMAP44xx into your design, the footprint of the phyCORE-OMAP44xx is available (see also Section 1.16.1).

Additional specifications:

Dimensions:	51 mm x 41 mm
Weight:	approximately 16 g with all optional components mounted on the circuit board
Storage temperature:	-40°C to +125°C
Operating temperature:	0°C to +70°C (commercial) -40°C to +85°C (industrial)[1]
Humidity:	95 % r.F. not condensed
Operating voltage:	VCC 3.3 V
Power consumption: VCC 3.3 V/1A typical	Typ. 3.3 watts Conditions: **VCC = 3.3 V, VBAT = 0 V**,512MB LP-DDR-RAM, 512MB NAND Flash, Ethernet, 1 GHz CPU frequency at 20°C

1. In order to guarantee reliable functioning of the SOM up to the maximum temperature appropriate cooling measures must be provided. Use of the SOM at high temperature has big impact on the SOM's life span (refer also to "**Important information on POH (power-on hours)**" in the Preface for more information).

These specifications describe the standard configuration of the phyCORE-OMAP44xx as of the printing of this manual.

Connectors on the phyCORE-OMAP44xx:

Manufacturer Samtec

Number of pins per contact Rows 120 (2 Rows of 60 pins each)

Samtec part number (lead free) BSH-060-01-L-D-A (receptacle)

Mating connectors on the phyCORE-OMAP44xx Carrier Board:

Mated height 5 mm

Manufacturer Samtec

Number of pins per contact Row 120 (2 Rows of 60 pins each)

Samtec part number (lead free) BTH-060-01-L-D-A (header)

PHYTEC part number (lead free) VM240

Different heights are offered for the receptacle sockets that correspond to the connectors populating the underside of the phyCORE-OMAP44xx. The connector height given above indicates the distance between the two connected PCBs when the module is mounted on the corresponding carrier board. In order to get the exact spacing, the maximum component height (1.5 mm) on the bottom side of the phyCORE must be subtracted.

Please refer to the corresponding data sheets and mechanical specifications provided by Samtec (www.samtec.com).

1.16 Hints for Integrating and Handling the phyCORE-OMAP44xx

1.16.1 Integrating the phyCORE-OMAP44xx

Successful integration in user target circuitry greatly depends on the adherence to the layout design rules for the GND connections of the phyCORE module. As a general design rule we recommend connecting all GND pins neighboring signals which are being used in the application circuitry. Just for the power supply of the module at least 10 GND pins corresponding to the VCC pins must be connected (refer to Section 1.1.3). For maximum EMI performance all GND pins should be connected to a solid ground plane.

Besides this hardware manual much information is available to facilitate the integration of the phyCORE-OMAP44xx into customer applications.

- the design of the standard phyCORE Carrier Board can be used as a reference for any customer application.
- many answers to common questions can be found at http://www.phytec.de/de/support/faq/faq-**phyCORE-OMAP44xx**.html, or http://www.phytec.eu/europe/support/faq/faq-**phyCORE-OMAP44xx**.html.
- the link "Carrier Board" within the category Dimensional Drawing leads to the layout data as shown in Figure 12 . It is available in different file formats.
- different support packages are available to support you in all stages of your embedded development. Please visit http://www.phytec.de/de/support/support-pakete.html, or http://www.phytec.eu/europe/support/support-packages.html, or contact our sales team for more details.

1.16.2 Handling the phyCORE-OMAP44xx

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Caution:

If any modifications to the module are performed, regardless of their nature, the manufacturer guarantee is voided.

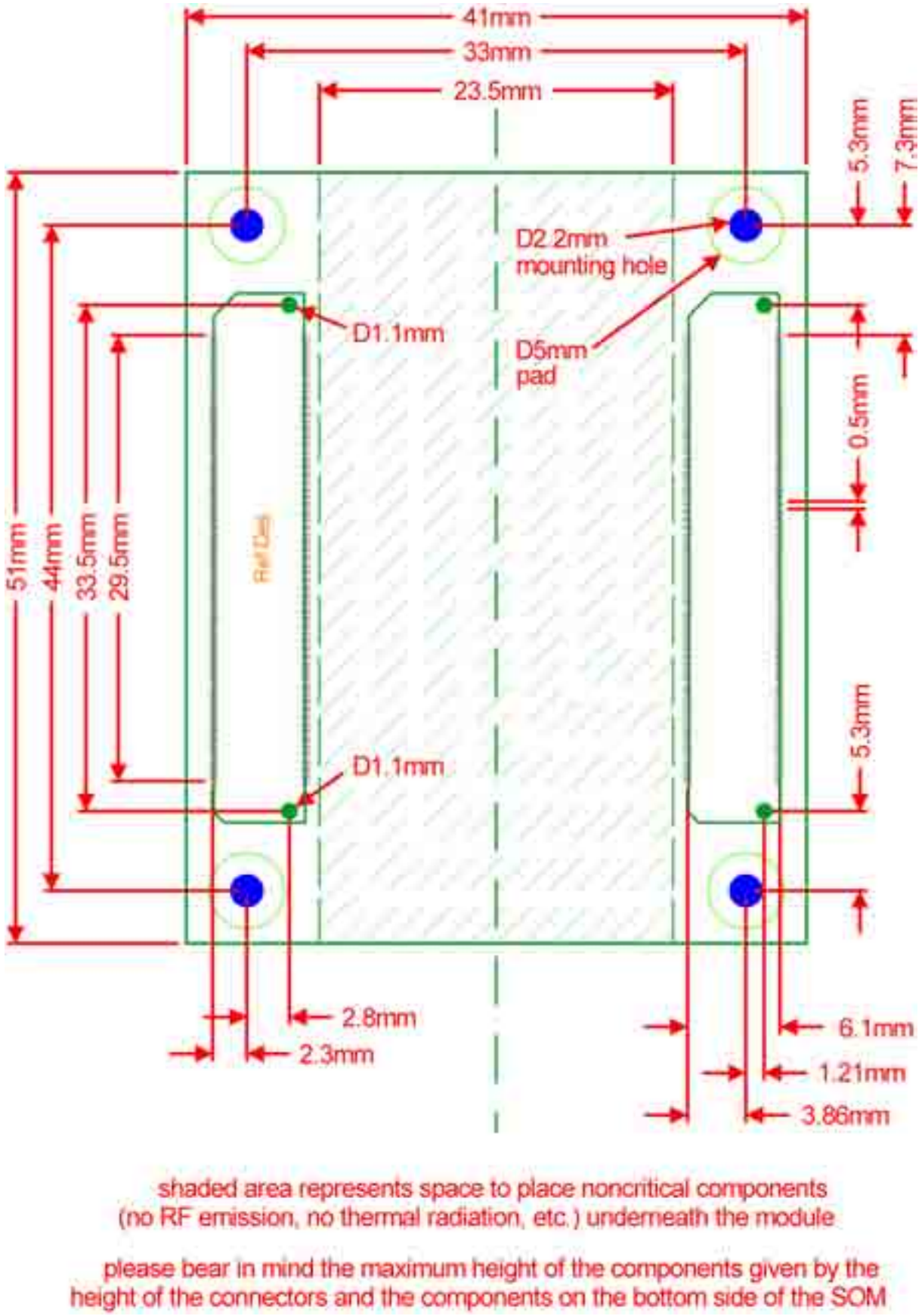


Figure 12: Footprint of the phyCORE-OMAP44x

1.17 Component Placement Diagram

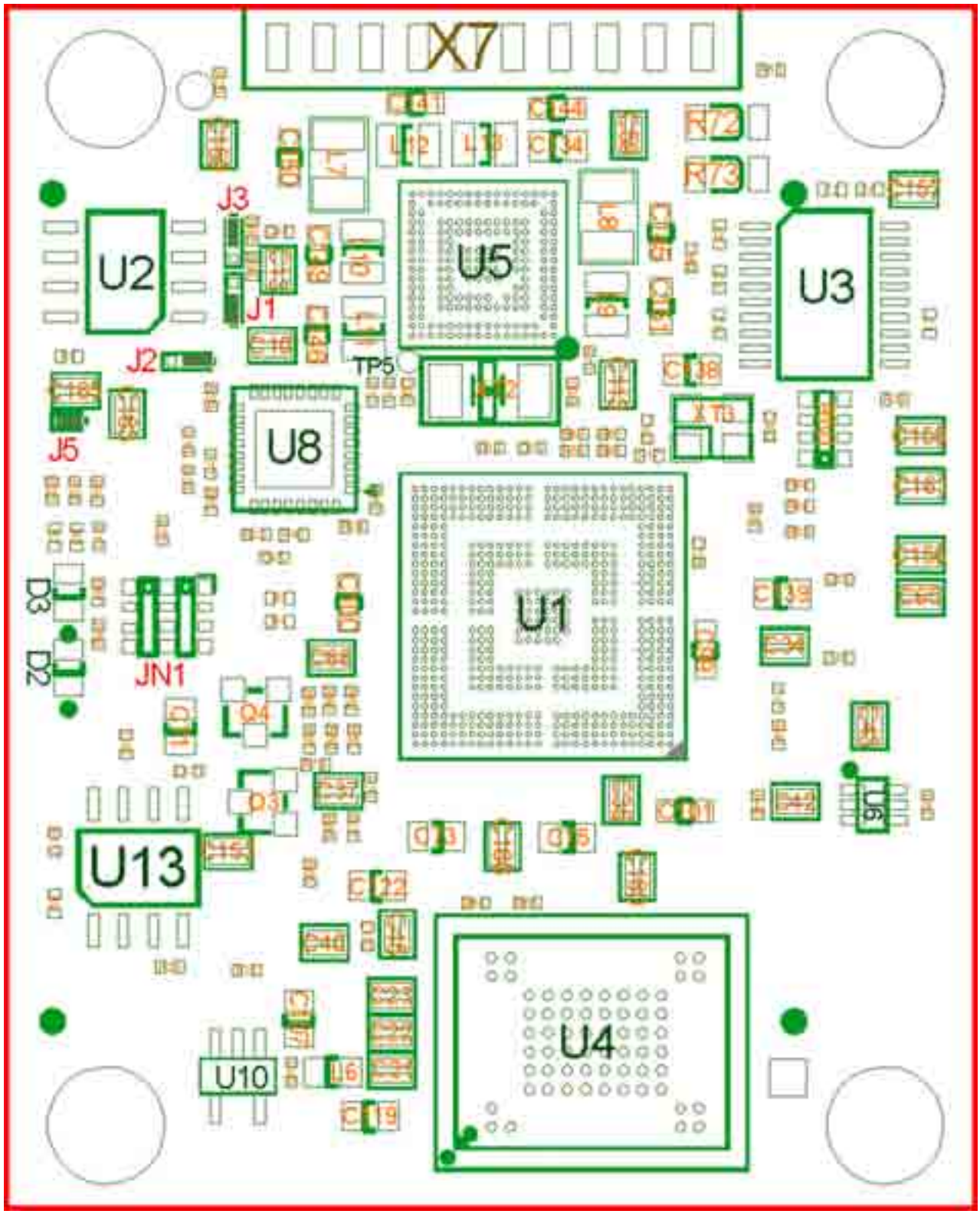


Figure 13: phyCORE-OMAP44xx Component Placement (top view)

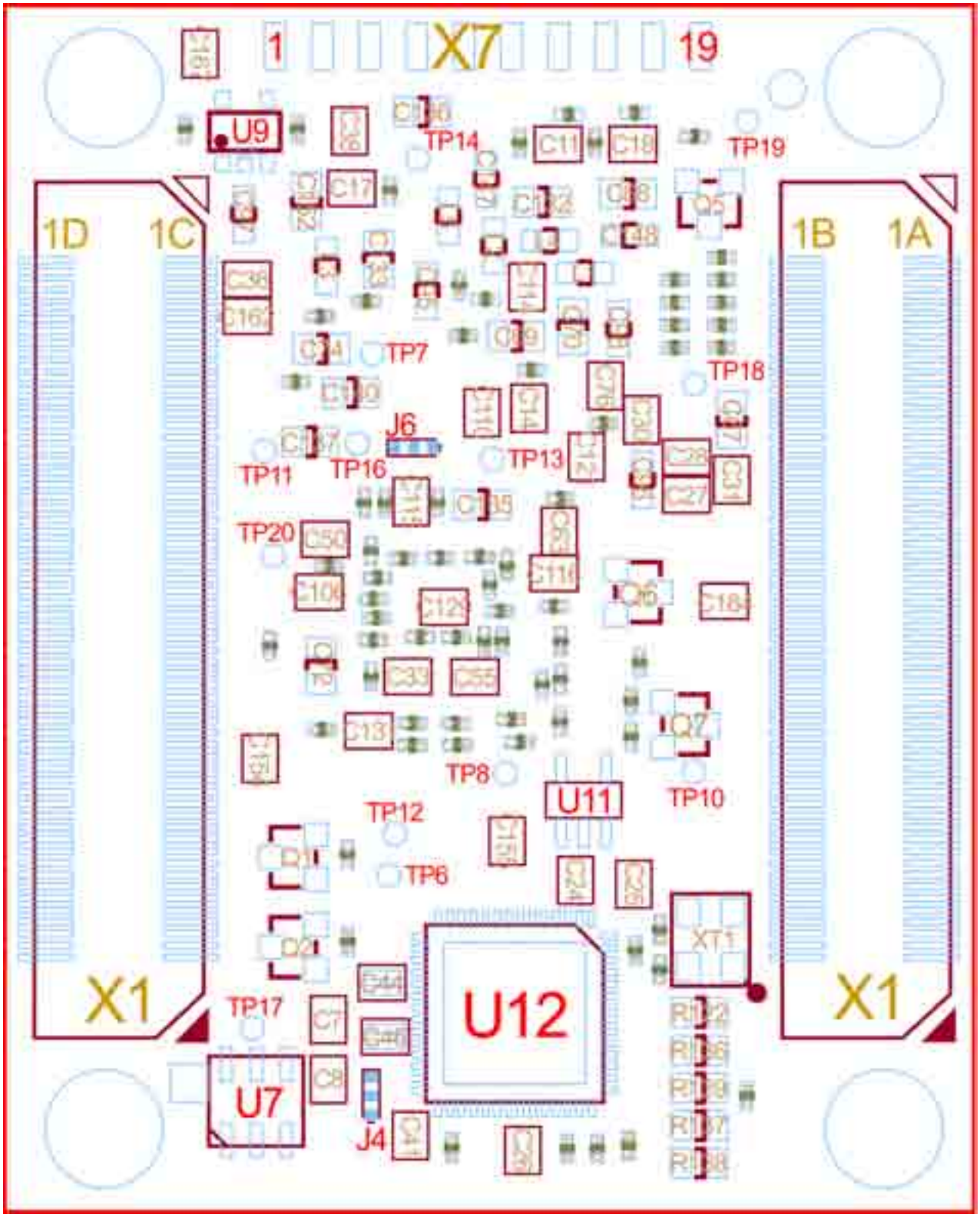


Figure 14: phyCORE-OMAP44xx Component Placement (bottom view)

2 Part II: PCM-959/phyCORE-OMAP44xx Carrier Board

Part 2 of this 2 part manual provides detailed information on the phyCORE-OMAP44xx Carrier Board and its usage with the phyCORE-OMAP44xx SOM. The information and all board images in the following chapters are applicable to the 1348.2 PCB revision of the phyCORE-OMAP44xx Carrier Board.

The carrier board can also serve as a reference design for development of custom target hardware in which the phyCORE SOM is deployed. Carrier Board schematics with BoM are available under a Non Disclosure Agreement (NDA). Re-use of carrier board circuitry likewise enables users of PHYTEC SOMs to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks.

2.1 Introduction

PHYTEC phyCORE-OMAP44xx Carrier Boards are fully equipped with all mechanical and electrical components necessary for the speedy and secure start-up and subsequent communication to and programming of applicable PHYTEC System on Module (SOM) modules. phyCORE-OMAP44xx Carrier Boards are designed for evaluation, testing and prototyping of PHYTEC System on Modules in laboratory environments prior to their use in customer designed applications.

The phyCORE-OMAP44xx Carrier Board provides a flexible development platform enabling quick and easy start-up and subsequent programming of the phyCORE-OMAP44xx System on Module. The carrier board design allows easy connection of additional expansion boards featuring various functions that support fast and convenient prototyping and software evaluation.

The phyCORE-OMAP44xx Carrier Board supports the following features for the phyCORE-OMAP44xx modules:

- Power supply circuits to supply the phyCORE-OMAP44xx and the peripheral devices of the carrier board
- Power over Ethernet (PoE)
- Full featured 4 line RS-232 transceiver supporting UART2 of the phyCORE-OMAP44xx with data rates of up to 120 kbps, hardware handshake and RS-232 connector
- Second RS-232 connector providing the signals of the RS-232 transceiver on the phyCORE-OMAP44xx and thus allowing communication via UART3 of the OMAP44xx at RS-232 level
- Four USB Host interfaces available at a standard USB A connector, as well as at the display and PEB connectors
- USB OTG interface brought out to a standard USB Mini-AB connector
- 10/100 Mbps Ethernet interface with Power over Ethernet
- Complete Audio interface available at three 3.5 mm audio jacks
- Phytec Display Interface (PDI) (LVDS display interface with separate connectors for data lines and display / backlight supply voltage) supporting either the Display Serial Interface (DSI), or the parallel display interface of the OMAP44xx
- Circuitry to allow dimming of a backlight
- Touchscreen interface for use of 4 wire resistive touch screens
- Two parallel camera interface connectors compatible to PHYTEC's phyCAM-P camera interface standard including an I^2C bus for camera control. One connector providing connectivity to the secondary camera interface (CSI2-B/CSI22) of the OMAP44xx for 8-bit-wide camera signals. Second connector to connect to the parallel camera interface of the OMAP4460 which supports selection between 8-bit and 10-bit-wide data signals
- Additional 30-pin pin header row for development purposes, connecting to the parallel camera interface of the OMAP4460
- Two Secure Digital Memory / MultiMedia Card slots
- Two extension connectors for customer prototyping purposes. Both compatible with PHYTEC's extension board (PEB) interface standard featuring one USB, one I^2C and one SPI interface, as well as one GPIO/IRQ at either connector
- DIP-Switch to configure the boot options for the phyCORE-OMAP44xx module
- Holder for backup battery to keep alive the real-time clock and other secure registers of the PMIC on the phyCORE-OMAP44xx

- HDMI - DVI interface
- Keypad interface for matrix with 6 columns and 6 rows
- Four user programmable LEDs
- Three push buttons for Power On, Reset and Wake Up
- Expansion connector with additional interfaces not used on the carrier board such as differential Class-D speaker output, UART1, McASP, etc., and options to connect custom circuitry directly to selected interfaces of the phyCORE-OMAP44xx
- JTAG interface for programming and debugging

2.1.1 Concept of the phyCORE-OMAP44xx Carrier Board

The phyCORE-OMAP44xx Carrier Board provides a flexible development platform enabling quick and easy start-up and subsequent programming of the phyCORE System on Module. The carrier board design allows easy connection of additional expansion boards featuring various functions that support fast and convenient prototyping and software evaluation.

This modular development platform concept includes the following components:

- the **phyCORE-OMAP44xx module** populated with the OMAP44xx processor and all applicable SOM circuitry such as DDR2 SDRAM, Flash, PHYs, and transceivers to name a few.
- the **phyCORE-OMAP44xx Carrier Board** which offers all essential components and connectors for start-up including: a power socket which enables connection to an **external power adapter**, interface connectors such as **DB-9**, **USB** and **Ethernet** allowing for use of the SOM's interfaces with standard cable.

The following sections contain specific information relevant to the operation of the phyCORE-OMAP44xx mounted on the phyCORE-OMAP44xx Carrier Board.

2.1.2 Overview of the phyCORE-OMAP44xx Carrier Board Peripherals

The phyCORE-OMAP44xx Carrier Board is depicted in Figure 15 and Figure 16 . It is equipped with the components and peripherals listed in Table 37, Table 38, Table 40 and Table 41. For a more detailed description of each peripheral, refer to the appropriate chapter listed in the applicable table. Figure 15 and Figure 16 highlight the location of each peripheral for easy identification.

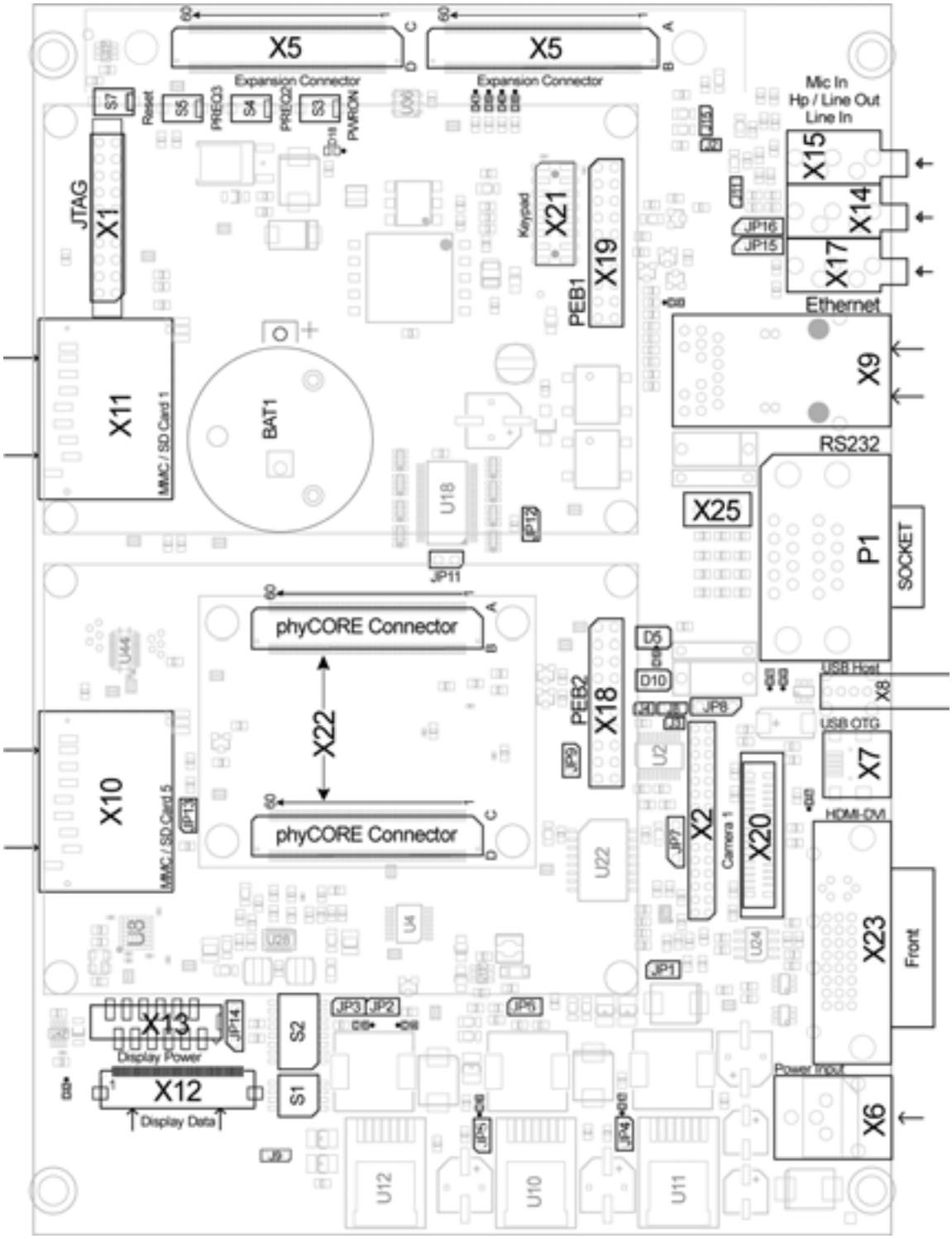


Figure 15: phyCORE-OMAP44xx Carrier Board Overview of Connectors, LEDs and Buttons (top view)

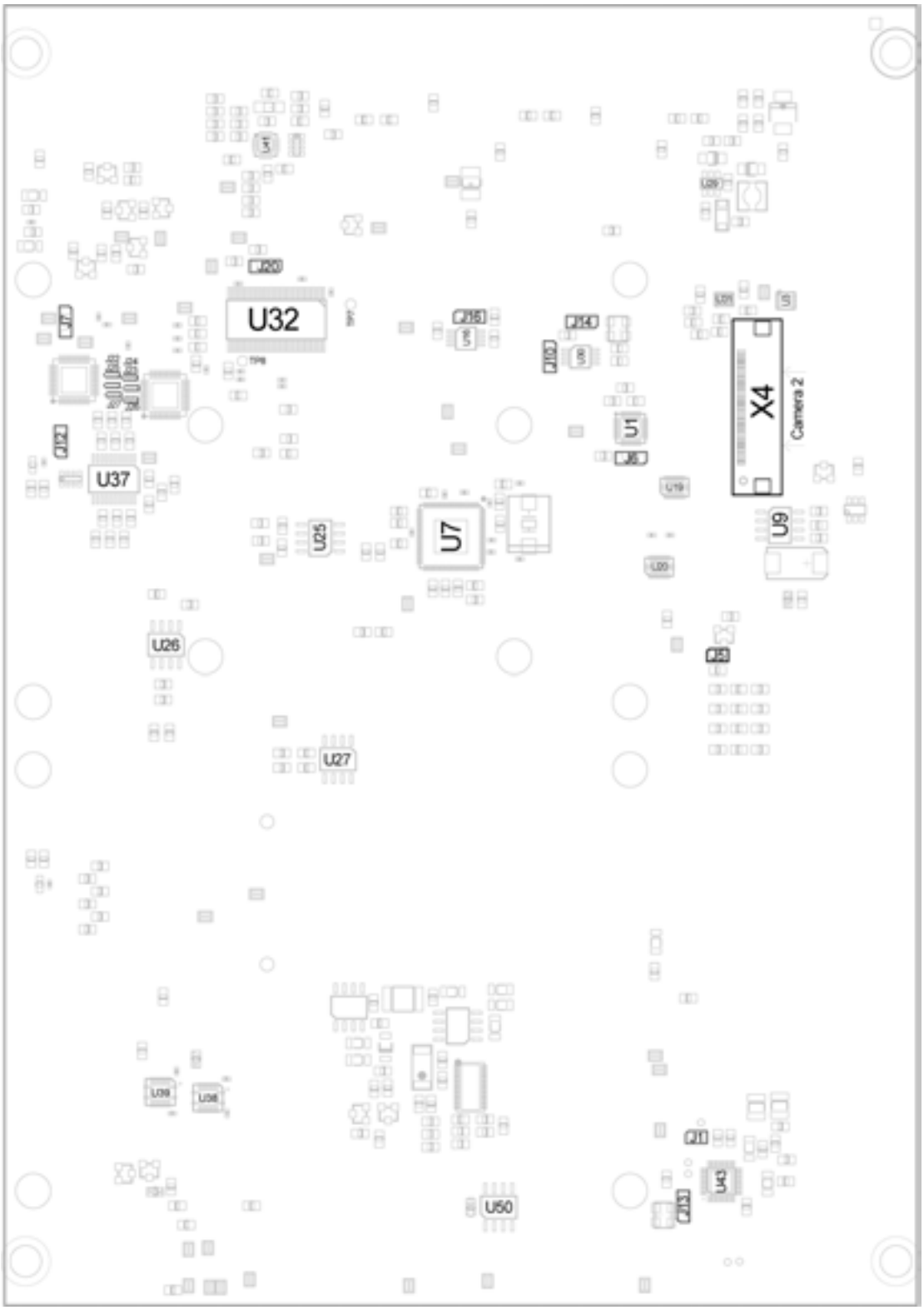


Figure 16: phyCORE-OMAP44xx Carrier Board Overview of Connectors, LEDs and Buttons (bottom view)

2.1.2.1 Connectors and Pin Header

Table 37 lists all available connectors on the phyCORE-OMAP44xx Carrier Board. Figure 15 and Figure 16 highlight the location of each connector for easy identification.

Reference Designator	Description	See Chapter
X1	JTAG connector	Section 2.1.3.19
X2	Reserved for future use	
X4	Secondary camera interface (compatible to phyCAM-P camera interface standard)	Section 2.1.3.9.2
X5	Expansion connector	Section 2.1.3.21
X6	Wall adapter input power jack to supply main board power (+12 - +24 V)	Section 2.1.3.2.1
X7	USB On-The-Go connector (USB Mini AB)	Section 2.1.3.6
X8	USB Host connector (USB 2.0 Standard-A)	Section 2.1.3.5
X9	Ethernet connector, RJ45 with speed and link led	Section 2.1.3.4
X10	Secure Digital Memory / MultiMedia Card slot	Section 2.1.3.16
X11	Secure Digital Memory /MultiMedia Card slot	Section 2.1.3.16
X12	Display data connector	Section 2.1.3.7.1
X13	Display / Backlight supply voltage connector	Section 2.1.3.7.2
X14	Headphone output connector / Stereo Line Out connector (3,5 mm audio jack)	Section 2.1.3.10
X15	Stereo Microphone input connector (3,5 mm audio jack)	Section 2.1.3.10
X17	Stereo Line In connector (3,5 mm audio jack)	Section 2.1.3.10
X18	PEB2 connector	Section 2.1.3.15
X19	PEB1 connector	Section 2.1.3.15
X20	Reserved for future use	
X21	Keypad connector	Section 2.1.3.20
X22	phyCORE-Connector for phyCORE-OMAP44xx SOM connectivity	Section 2.1.3.1
X23	HDMI-DVI connector	Section 2.1.3.8
P1	Serial Interfaces, 2 x DB-9 female	Section 2.1.3.3
BAT1	Battery holder for standard CR 2032 lithium coin cell	Section 2.1.3.18

Table 37: phyCORE-OMAP44xx Carrier Board Connectors and Pin Headers

Note:

The signal levels of the I^2C and SPI interface are shifted from VCC_1V8_IO (1.8 V) at the phyCORE Connector to VCC3V3 (3.3 V) by level shifters on the phyCORE Carrier Board.
Ensure that all module connections are not to exceed their expressed maximum voltage or current.
Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets.
As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

2.1.2.2 Switches

The phyCORE-OMAP44xx Carrier Board is populated with some switches which are essential for the operation of the phyCORE-OMAP44xx module on the carrier board. Figure 15 shows the location of the switches and push buttons.

Button	Description	See Chapter
S3	Power button – to power on and off main supply voltages of the phyCORE-OMAP44xx	Section 2.1.3.2.1 and Section 2.1.3.2.2
S4	Wake-up button – to issue a wake-up signal at pin X1C44 (X_PMIC_PREQ2A) of the phyCORE-OMAP44xx	Section 1.4.3.3
S5	Wake-up button – to issue a wake-up signal at pin X1C43 (X_PMIC_PREQ3) of the phyCORE-OMAP44xx	Section 1.4.3.3
S7	System Reset Button – system reset signal generation	Section 2.1.3.18

Table 38: phyCORE-OMAP44xx Carrier Board Push Buttons Descriptions

S3 Issues a **power on/off** event. Pressing this button approx. 2 seconds will toggle the PWRON pin of the phyCORE-OMAP44xx PMIC device LOW, causing the PMIC to turn on the supply voltages. Pressing this button for more than 10 seconds causes the PMIC to turn off the supply voltages.

Additionally two DIP-Switches are available at S1 and S2. These DIP-switches allow to change the booting device order of the OMAP44xx which is predefined by a resistor network on the phyCORE-OMAP44xx. The default booting device order is 1st: NAND, 2nd: USB, 3rd: UART, 4th: MMC1 (please refer to Section 2.1.3.17 for more information).

Button	Description	See Chapter
S1	Configuration of pins X_BOOT[0] and X_BOOT[1]	Section 2.1.3.17
S2	Configuration of pins X_BOOT[2:5]	

Table 39: phyCORE-OMAP44xx Carrier Board DIP-Switch Descriptions

2.1.2.3 LEDs

The phyCORE-OMAP44xx Carrier Board is populated with numerous LEDs to indicate the status of the various USB-Host interfaces, as well as the different supply voltages. Figure 15 shows the location of the LEDs. Their function is listed in the table below:

LED	Color	Description	See Chapter
D5	green	Hi-Speed indicator LED for USB hub's upstream port connection speed	Section 2.1.3.5
D10	red	Active/Suspend status LED of the USB hub at U7	
D19	green	Downstream port 3 (USB3) green led	
D20	green	Downstream port 2 (USB2) green led	
D21	green	Downstream port 1 (USB1) green led	
D22	green	Downstream port 4 (USB4) green led	
D23	yellow	Downstream port 1 (USB1) amber led	
D27	green	Indicates presence of VBUS at the USB OTG interface	Section 2.1.3.6
D14	green	VCC_1V8 - 1.8 V supply voltage	Section 2.1.3.2
D15	green	VCC_1V2 - 1.2 V supply voltage for the DSI2LVDS Bridge Chip	
D16	green	VCC_3V3 - 3.3 V supply voltage for the phyCORE-OMAP44xx and various peripherals on the phyCORE-OMAP44xx Carrier Board	
D17	green	VCC_5V - 5 V supply voltage	
D18	green	Indicates presence of 12 V for POE	Section 2.1.3.2.2
D38	green	User LED 1	Section 2.1.3.14
D39	yellow	User LED 2	
D40	yellow	User LED 3	
D41	red	User LED 4	

Table 40: phyCORE-OMAP44xx Carrier Board LEDs Descriptions

Note:

Detailed descriptions of the assembled connectors, jumpers and switches can be found in the following chapters.

2.1.2.4 Jumpers

The phyCORE Carrier Board comes pre-configured with 15 removable jumpers (JP) and 22 solder jumpers (J). The jumpers allow the user flexibility of configuring a limited number of features for development purposes. Table 41 below lists the jumpers, their default positions, and their functions in each position. Figure 17 depicts the jumper pad numbering scheme for reference when altering jumper settings on the development board.

Figure 18 provides a detailed view of the phyCORE-OMAP44xx Carrier Board jumpers and their default settings. In this diagrams a beveled edge indicates the location of pin 1.

Before making connections to peripheral connectors it is advisable to consult the applicable section in this manual for setting the associated jumpers.

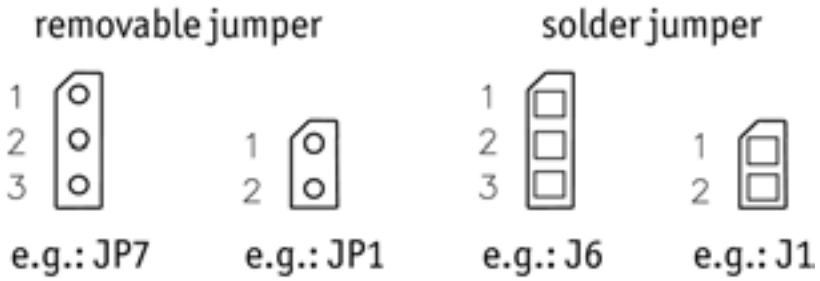


Figure 17: Typical Jumper Numbering Scheme

Table 41 provides a comprehensive list of all carrier board jumpers. The table only provides a concise summary of jumper descriptions. For a detailed description of each jumper see the applicable chapter listed in the right hand column of the table.

Note:

Jumpers not listed should not be changed as they are installed with regard to the configuration of the phyCORE-OMAP44xx.

If manual modification of the solder jumpers is required please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the board inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

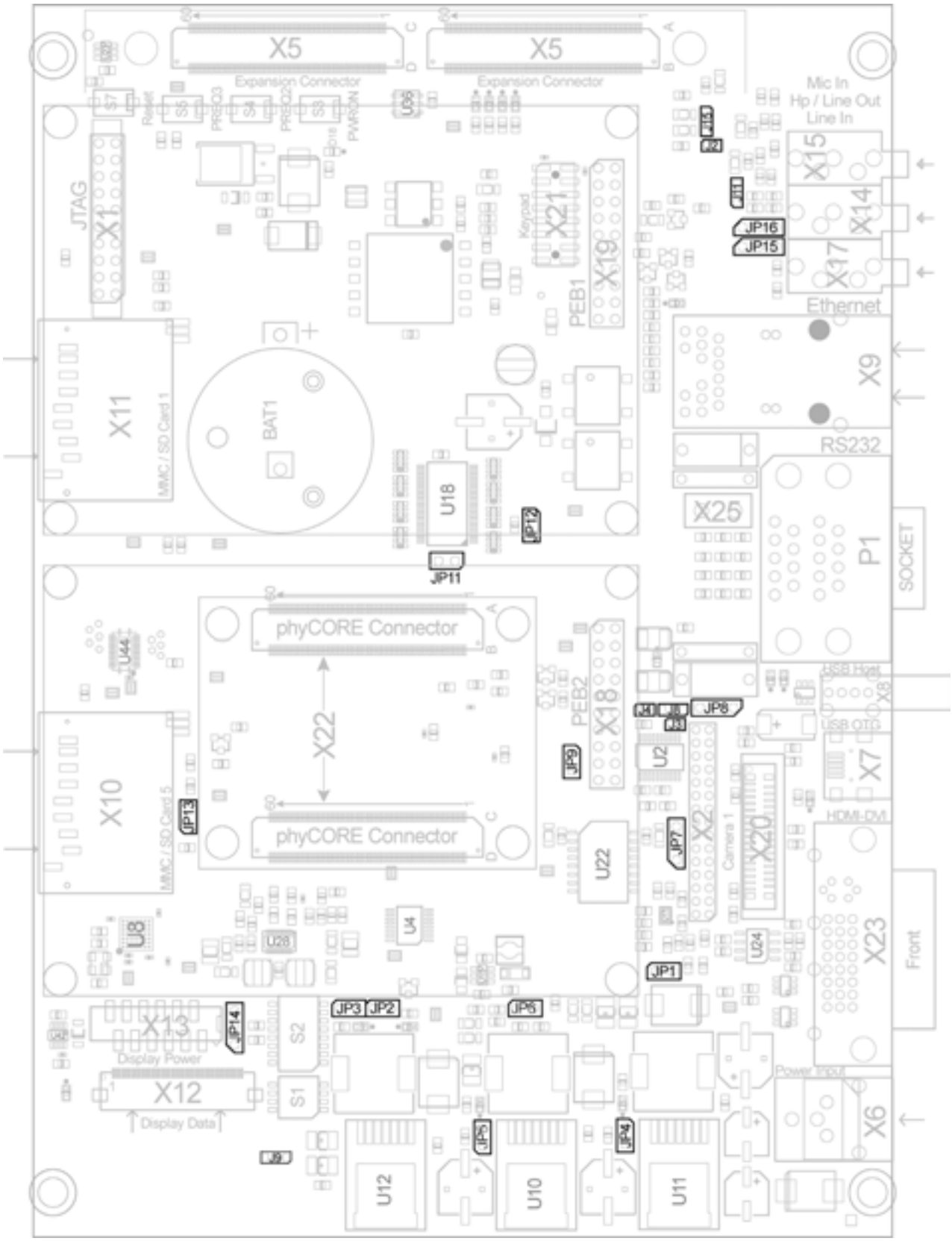


Figure 18: phyCORE-OMAP44xx Carrier Board Jumper Locations (top view)

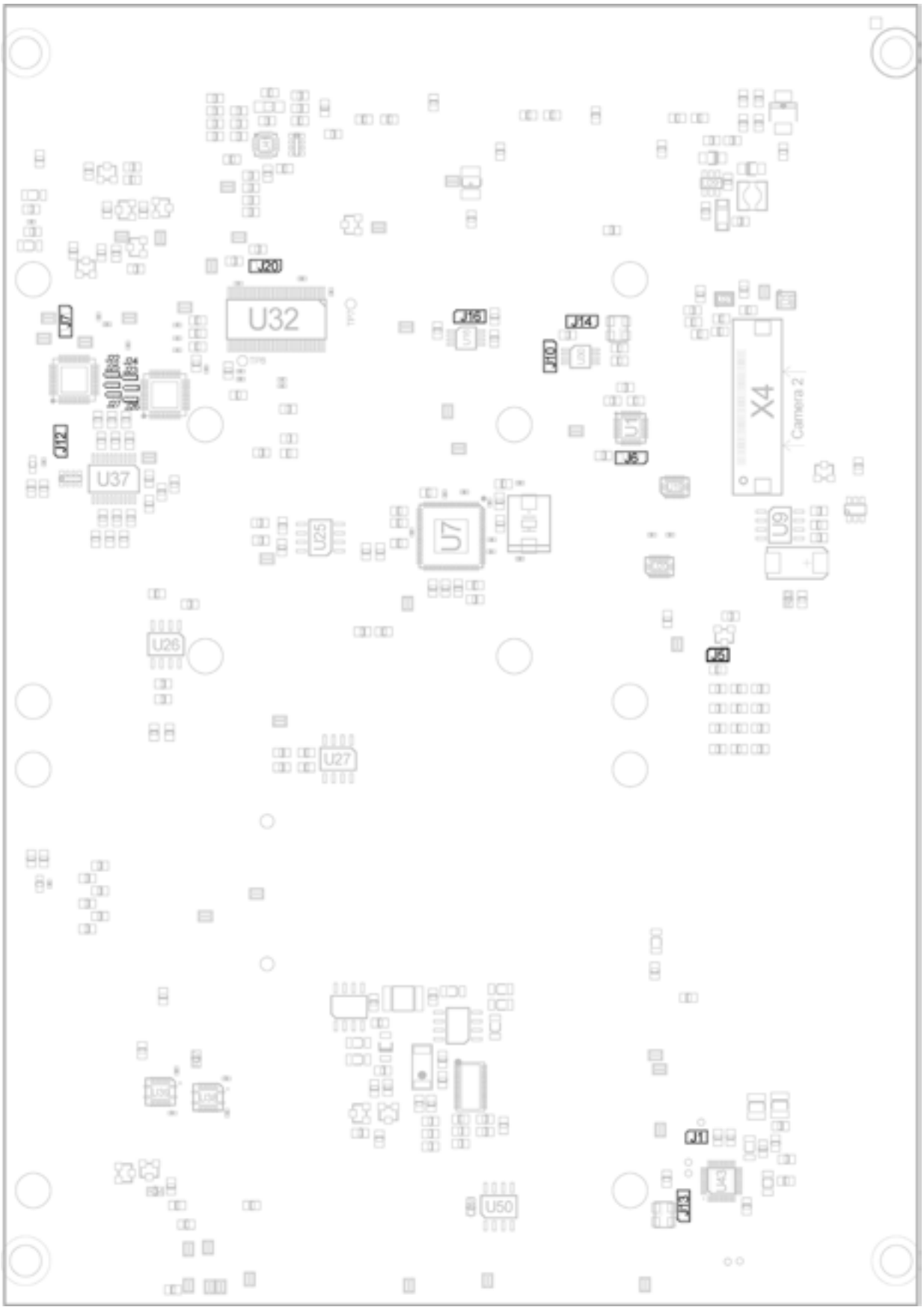


Figure 19: phyCORE-OMAP44xx Carrier Board Jumper Locations (bottom view)

The following conventions were used in the Jumper column of the jumper table (Table 41)

- J = solder jumper
- JP = removable jumper

Jumper	Setting	Description	Chapter
JP1		Jumper JP1 connects the supply voltage VCC_CAM-2 to the circuitry of the second phyCAM-P camera interface Camera_2 at connector X4.	Section 2.1.3.9.2
	open	VCC_CAM-2 not connected; second phyCAM-P interface Camera_2 not available	
	closed	**Supply voltage VCC_CAM-2 connected; second phyCAM-P interface Camera_2 can be used**	
JP2		Jumper JP2 enables the DC/DC converter for the VCC_1V8 supply voltage	Section 2.1.3.2
	open	**VCC_1V8 enabled**	
	closed	VCC_1V8 disabled	
JP3		Jumper JP3 enables the DC/DC converter for the VCC_1V2 supply voltage	Section 2.1.3.2
	open	**VCC_1V2 enabled**	
	closed	VCC_1V2 disabled	
JP4		Jumper JP4 enables the DC/DC converter for the VCC_5V supply voltage	Section 2.1.3.2
	open	**VCC_5V enabled**	
	closed	VCC_5V disabled	
JP5		Jumper JP5 enables DC/DC converter for the the VCC_3V3 supply voltage	Section 2.1.3.2
	open	**VCC_3V3 enabled**	
	closed	VCC_3V3 disabled	
JP6		Jumper JP6 connects the supply voltage VCC_CAM-1 to the circuitry of the first phyCAM-P camera interface Camera_1 at connector X20.	**For future derivatives of the phyCORE-OMAP44xx !**
	open	VCC_CAM-1 not connected; first phyCAM-P interface Camera_1 not available	
	closed	Supply voltage VCC_CAM-1 connected; first phyCAM-P interface Camera_1 can be used	

Table 41: phyCORE-OMAP44xx Carrier Board Jumper Settings[1]

Jumper	Setting	Description	Chapter
JP7		Jumper JP7 selects the voltage level of the CAM-2_CTRL1 pin (X4-27) at phyCAM-Connector X4	Section 2.1.3.9.2
	open	CAM-2_CTRL1 not connected	
	1+2	CAM-2_CTRL1 connected to VCC_CAM-2	
	2+3	**CAM2_CTRL1 connected to GND**	
JP8		Jumper JP8 selects the voltage level of the CAM-2_CTRL2 pin (X4-4) at phyCAM-Connector X4	Section 2.1.3.9.2
	open	CAM-2_CTRL2 not connected	
	1+2	CAM-2_CTRL2 connected to VCC_CAM-2	
	2+3	**CAM2_CTRL2 connected to GND**	
JP9		Jumper JP9 forces the USB OTG interface of the phyCORE-OMAP44xx to function either as host (master), or device (slave).	Section 2.1.3.6
	open	**USB_OTG_ID floating, phyCORE-OMAP44xx in slave mode, or according to the mode configured by software**	
	closed	USB_OTG_ID connected to GND, phyCORE-OMAP44xx in host mode	
JP11		Jumper JP11 enables the bus transceiver of the first phyCAM-P camera interface Camera_1 at connector X20	**For future derivatives of the phyCORE-OMAP44xx !**
	open	Bus transceiver disabled; first phyCAM-P interface Camera_1 not available	
	closed	Bus transceiver enabled; first phyCAM-P interface Camera_1 can be used	
JP12		Jumper JP12 selects either 8-bit, or 10-bit resolution of the first phyCAM-P camera interface at connector X20	**For future derivatives of the phyCORE-OMAP44xx !**
	open	First phyCAM-P interface with 8-bit resolution	
	closed	First phyCAM-P interface with full 10-bit resolution	
JP13		Jumper JP13 selects either the parallel, or the DSI display interface of the phyCORE-OMAP44xx as source for the PHYTEC Display -Interface (PDI) at connector X12	Section 2.1.3.7.1
	open	**Data of the parallel display interface of the phyCORE-OMAP44xx brought out at PDI-Connector X12**	
	closed	Data of the DSI interface of the phyCORE-OMAP44xx brought out at PDI-Connector X12	

Table 41: phyCORE-OMAP44xx Carrier Board Jumper Settings[1]

Jumper	Setting	Description	Chapter
JP14		JP14 connects the Shutdown input of the FLATLINK™ transmitter at U32 to reset, or GND	Section 2.1.3.7.1
	1 + 2	**The X_nReset_PWRON signal of the phyCORE-OMAP44xx shuts down the FLATLINK™ transmitter to avoid bad display signals during reset**	
	2 + 3	The Shutdown input of the FLATLINK™ transmitter is connected to GND in order to disable the device (e.g. if a custom display interface is connected to extension connector X5)	
JP15, JP16		JP15 and JP16 select the source for audio connector X14. X14 can serve as either headphone output connector, or as stereo line out connector. JP15 selects the source of the right channel, while JP16 connects the left channel of the desired source to connector X14.	Section 2.1.3.10
	1+2	**Audio jack X14 serves as headphone output connector**	
	2+3	The stereo line out signals are available at audio jack X14	
J3		In combination with jumpers J4 and J8, and resistors R25 and R26 jumper J3 allows to configure the various operating modes of the RS-232 transceiver at U2. J3 connects the Force-On input of the RS-232 transceiver to pad 2 of jumper J8 for further configuration.	Section 2.1.3.3.2
	open	FORCEON disconnected from jumper J8 and pulled HIGH by R25	
	closed	**FORCEON connected to jumper J8**	
J4		In combination with jumpers J3 and J8, and resistors R25 and R26 jumper J4 allows to configure the various operating modes of the RS-232 transceiver at U2. J4 connects the Force-Off input of the RS-232 transceiver to pad 2 of jumper J8 for further configuration.	Section 2.1.3.3.2
	open	/FORECOFF disconnected from jumper J8 and pulled HIGH by R26	
	closed	**/FORECOFF connected to jumper J8**	
J5		Jumper J5 allows to extend the USB OTG overcurrent signal USB_OTG_OC to pin X1D42 (X_SYS_NIRQ2) of the phyCORE-OMAP44xx which connects to GPIO 183 of the OMAP44xx	Section 2.1.3.6
	open	disconnected	
	closed	**USB_OTG_OC can be evaluated at GPIO 183 of the OMAP44xx**	

Table 41: phyCORE-OMAP44xx Carrier Board Jumper Settings[1]

Jumper	Setting	Description	Chapter
J7		Jumper J7 configures the operation mode (normal operation / test mode) of the TC358764 DSI2LVDS Bridge Chip mounted at U8	Section 2.1.3.7.1
	1+2	Test mode enabled	
	2+3	**Normal operation; test mode disabled**	
J8		In combination with jumpers J3 and J8, and resistors R25 and R26 jumper J8 allows to configure the various operating modes of the RS-232 transceiver at U2. J8 connects jumpers J3 and J4 (and in further consequence the Force-On and Force-Off inputs of the RS-232 transceiver) to GND, or the /Invalid output.	Section 2.1.3.3.2
	open	Jumpers J3 and J4 are neither connected to GND nor to the /Invalid output. FORCEON and /FORECOFF are pulled HIGH by pull-up resistors R25 and R26	
	1+2	**Depending on the configuration of jumpers J3 and J4 FORCEON, or /FORECOFF, or both inputs are connected to the /Invalid output of the RS-232 driver.**	
	2+3	Depending on the configuration of jumpers J3 and J4 FORCEON, or /FORECOFF, or both inputs are connected to GND_RS232.	
J9		Jumper J9 configures the I^2C address of the touch screen controller at U41	Section 2.1.3.7.3
	1+2	**I2C device address set to 0x41**	
	2+3	I^2C device address set to 0x44	
J10		Jumper J10 selects the source of the reset signal at phyCAM-P interface connector X4. The camera reset can be triggered either by the system reset of the PMIC on the phyCORE-OMAP44xx, or the OMAP44xx's camera sensor reset signal X_CAM_GLOBAL_RESET	Section 2.1.3.9.2
	1+2	**Camera reset is triggered by the PMIC's system reset signal X_nRESET_PWRON**	
	2+3	The camera sensor reset signal X_CAM_GLOBAL_RESET resets a camera connected to X4	

Table 41: phyCORE-OMAP44xx Carrier Board Jumper Settings[1]

Jumper	Setting	Description	Chapter
J11		Jumper J11 connects the shield contact of audio jack X14 (headphone out) to either GND, or the HPCOM output driver of the stereo audio codec at U43. Connecting the shield contact to HPCOM allows to use the jack detection function of the stereo audio codec.	Section 2.1.3.10
	1+2	Shield contact connected to the HPCOM output driver of the stereo audio codec, jack detection enabled	
	2+3	**Shield contact connected to GND, jack detection disabled**	
J12		Jumper J12 configures the level of the supply voltage for the SD / MM card interface at connector X10	Section 2.1.3.16
	1+2	**VCC_3V3 connected to VCC_SDMMC5**	
	2+3	VCC_1V8 connected to VCC_SDMMC5	
J13		Jumper J13 configures the source for the audio codec's master clock. The clock can be generated either on the phyCORE-OMAP44xx (pin X_FREF_CLK4_REQ), or an oscillator at OZ1 on the carrier board.	Section 2.1.3.10
	1+2	Pin MCLK of the audio codec connected to oscillator OZ1 (19.2 MHz)	
	2+3	**Pin MCLK of the audio codec connected to X_FREF_CLK4_REQ (X1D29) of the phyCORE-OMAP44xx**	
J14		Jumper J14 configures the source for the master clock at the phyCAM-P interface connector X4. The clock can be generated either on the phyCORE-OMAP44xx (pin X_FREF_CLK4_OUT), or an oscillator at QO1 on the carrier board.	Section 2.1.3.9.2
	1+2	**CAM-2_MCLK connected to oscillator QO1 (26 MHz)**	
	2+3	CAM-2_MCLK connected to X_FREF_CLK4_OUT (X1B13) of the phyCORE-OMAP44XX	
J20		J20 selects rising, or falling edge strobe for the FlatLink™ transmitter at U32 used for the display connectivity of the phyCORE-OMAP44xx	Section 2.1.3.7.1
	1+2 (10 k resistor)	**Rising edge strobe used for the LVDS display signals**	
	2+3	Falling edge strobe used for the LVDS display signals	

Table 41: phyCORE-OMAP44xx Carrier Board Jumper Settings[1]

1. Default settings are in **bold blue** text

2.1.3 Functional Components on the phyCORE-OMAP44xx Carrier Board

This section describes the functional components of the phyCORE-OMAP44xx Carrier Board supporting the phyCORE-OMAP44xx. Each subsection details a particular connector/interface and associated jumpers for configuring that interface.

2.1.3.1 phyCORE-OMAP44xx SOM Connectivity (X22)

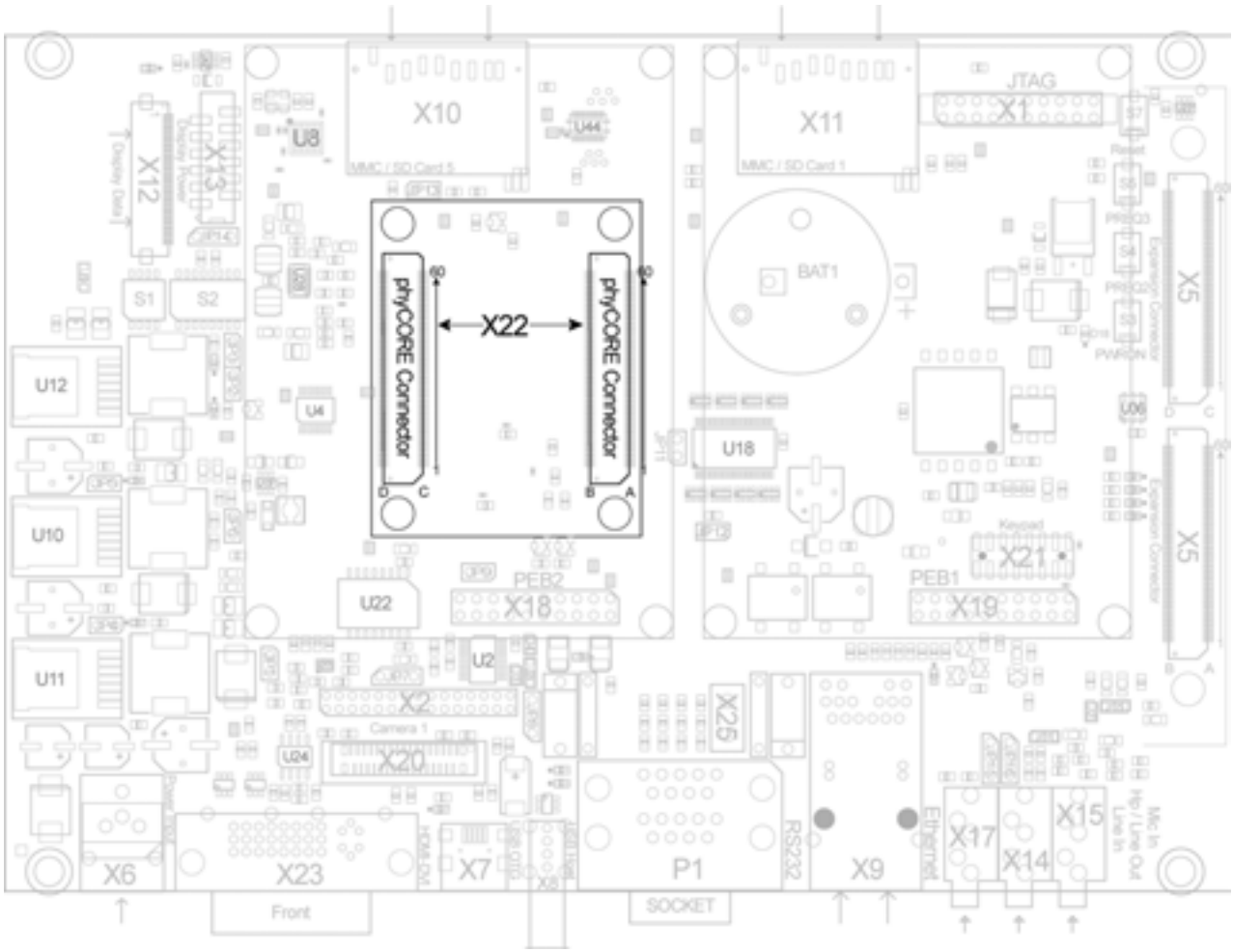


Figure 20: phyCORE-OMAP44xx SOM Connectivity to the Carrier Board

Connector X22 on the carrier board provides the phyCORE System on Module connectivity. The connector is keyed for proper insertion of the SOM. Figure 20 above shows the location of connector X22, along with the pin numbering scheme as described in Section 1.2. Please refer to Section 1.15 for information on manufacturer, part number and ordering.

Caution:

Samtec connectors guarantee optimal connection and proper insertion of the phyCORE-OMAP44xx. Please make sure that the phyCORE-OMAP44xx is fully plugged into the matting connectors of the carrier board. Otherwise individual signals may have a bad, or no contact.

To support all features of the phyCORE-OMAP44xx Carrier Board the BSP provided assigns functions different to what is described in Table 2 to some pins of the phyCORE-OMAP44xx. Table 42 lists all pins with functions different to what is described in Table 2. Use of these pins in their original function described in Section 1 of this manual requires changing the BSP.

Pin # at phyCORE-Connector	Signal	I/O (from the phyCORE's perspective)	SL at phyCORE-Connector	Description
X1A38	X_GPIO_115	O	VCC_1V8_IO	USB_OTG_EN enables the USB OTG V_{BUS} detection
X1A39	X_McASP_AMUTEIN	I	1.8 V	Interrupt signal of the touch controller, available at GPIO 117 of the OMAP44xx
X1B13	X_FREF_CLK1_OUT_GPIO_181	I	1.8 V	GPIO 181 used as power on/off signal input to allow for an ON/OFF switch on a front panel
X1B36	X_ABE_CLKS	O	VCC_1V8_IO	GPIO 118 used as display enable signal at display data connector X12
X1B39	X_GPIO_114	I	VCC_1V8_IO	SPI Interface Ready signal
X1D16	X_UART4_TX	I	1.8 V	GPIO 156 used as interrupt input of PEB connector X18
X1D17	X_UART4_RX	I	1.8 V	GPIO 155 used as interrupt input of PEB connector X19
X1D28	X_GPIO_WK30	I	1.8 V	GPIO WK30 functions as input for the card detect signal of SDMMC5 Card Slot X10
X1D29	X_FREF_CLK4_REQ	O	VCC_1V8_IO	Clock for the audio driver at U43[1]
X1D34	X_HDMI_CEC	I/O	1.8 V / VCC_1V8_IO	Connects to GPIO 64 as SPI interrupt input
X1D42	X_SYS_NIRQ2	I	1.8 V	In the standard configuration the USB OTG overcurrent signal (USB_OTG_OC) is attached to this pin and interpreted by the BSP utilizing GPIO 183 of the OMAP44xx.[2]

Table 42: Specifically used Pins on the phyCORE-Connector

1. Can be disconnected by changing jumper J13
2. Opening jumper J5 disconnects USB_OTG_OC from the phyCORE-Connector

2.1.3.2 Power

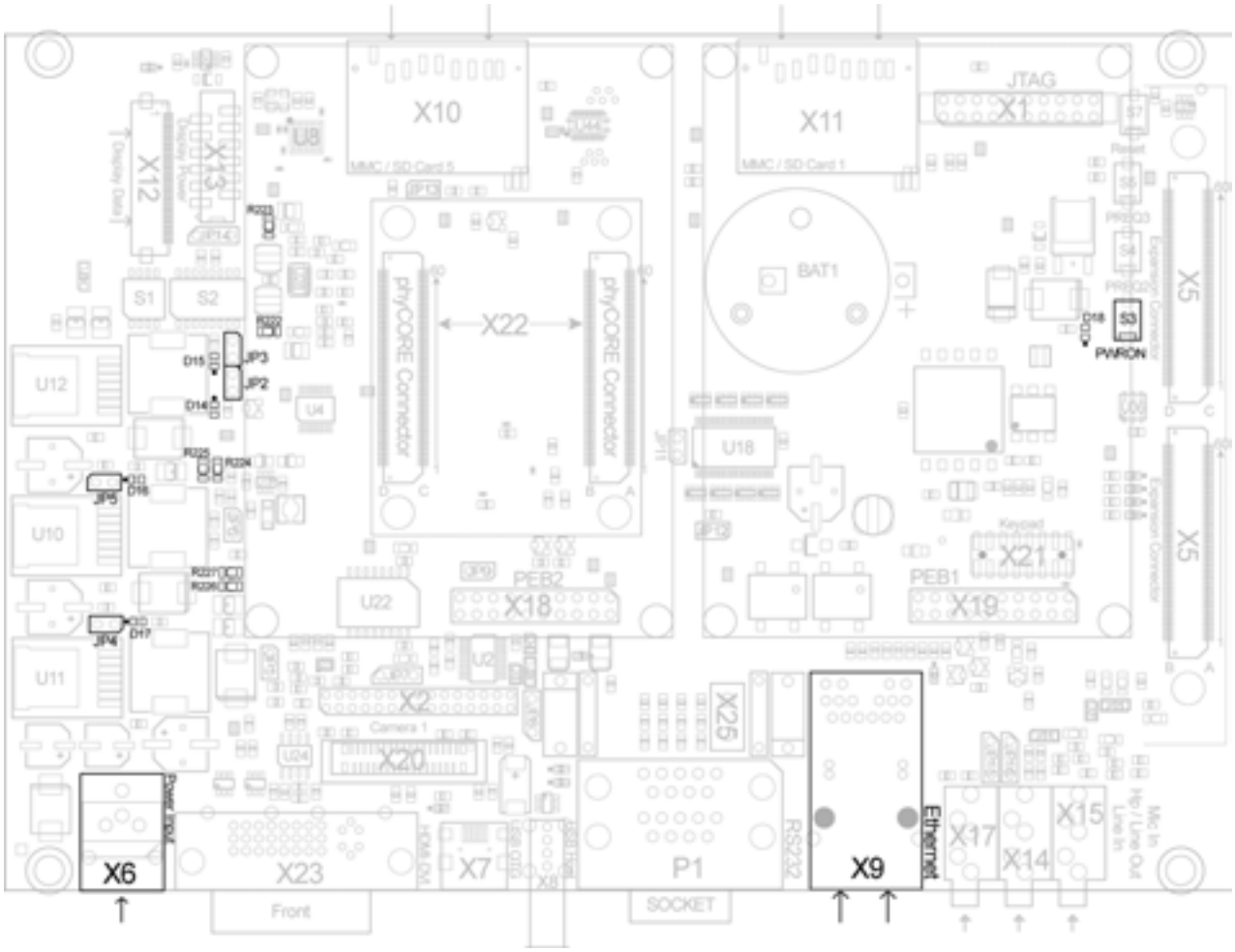


Figure 21: Powering Scheme

The primary input power of the phyCORE-OMAP44xx Carrier Board comes from either the wall adapter jack X6 (+12 V or +24 V), or the Power-over-Ethernet circuit (via the Ethernet jack X9).

Switching regulators on the carrier board generate five different voltages to supply the phyCORE-OMAP44xx and the different components of the system. The following table lists the 5 voltage domains and their main use.

Voltage domain	Description
VCC_12_24	Main supply voltage from wall adapter input at X6 or Power of Ethernet (+12 V to +24 V DC) at X9
VCC_5V	5 V voltage domain required for different interfaces, such as USB, HDMI, etc.
VCC_3V3	3.3 V voltage domain supplying the phyCORE-OMAP44xx and various peripherals
VCC_5V_FIX	5 V voltage domain to supply the 1.8 V and 1.2 V regulators
VCC_1V8	1.8 V voltage domain supplying some peripherals (e.g. audio codec, etc.)
VCC_1V2	1.2 V voltage domain to supply DSI2LVDS Bridge Chip only

Table 43: Voltage Domains on the Carrier Board

Five LEDs on the phyCORE-OMAP44xx Carrier Board show the status of the different voltage domains. The assignment of the LEDs to the voltage domains is shown in the following table:

LEDs	Color	Description
D17	green	VCC_5V - 5 V supply voltage
D16	green	VCC_3V3 - 3.3 V supply voltage for the phyCORE-OMAP44xx and various peripherals on the phyCORE-OMAP44xx Carrier Board
D15	green	VCC_1V2 - 1.2 V supply voltage for the DSI2LVDS Bridge Chip
D14	green	VCC_1V8 - 1.8 V supply voltage
D18	green	POE supply voltage available

Table 44: Power LEDs

Four jumpers on the phyCORE-OMAP44xx Carrier Board allow to enable, or disable single voltage domains. Closing a jumper **disables** the corresponding voltage domain. The following table lists the jumpers and the associated voltage domain.

Voltage domain	Jumper
VCC_5V	JP4
VCC_3V3	JP5
VCC_1V8	JP2
VCC_1V2	JP3

Table 45: Power Jumpers

2.1.3.2.1 Wall Adapter Input (X6)

Caution:

Do not use a laboratory adapter to supply power to the carrier board! Power spikes during power-on could destroy the phyCORE module mounted on the carrier board! Do not change modules or jumper settings while the carrier board is supplied with power!

Permissible input voltage at X6: +12 V to +24 V DC unregulated.

The required current load capacity of the power supply depends on the specific configuration of the phyCORE mounted on the carrier board, the particular interfaces enabled while executing software as well as whether an optional expansion board is connected to the carrier board. An adapter with a minimum supply of 2.0 A is recommended.

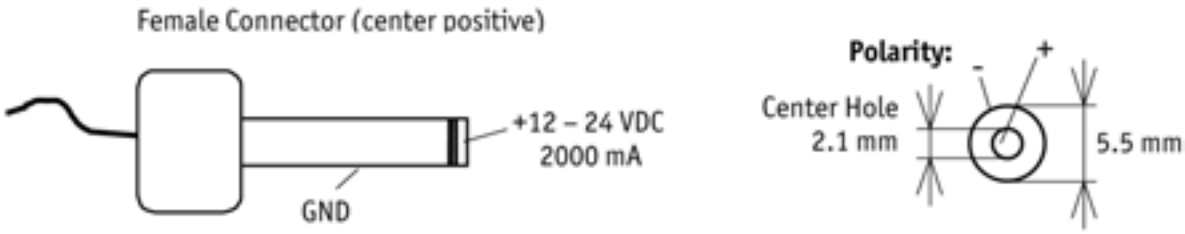


Figure 22: Power Connector Corresponding to Wall Adapter Input X6

It is necessary to ensure that jumper JP5 is open in order to supply power to the phyCORE module!

Note:

For powering up the phyCORE the following actions have to be done:
1. Plug in the power supply connector
   » The power LEDs D14 - D17 should light up and the phyCORE sends serial data from UART3 to the top DB-9 sub-connector of connector P1.
2. For powering down the phyCORE-OMAP44xx button S3 should be pressed for a minimum time of 10 s.
3. To restart the system press button S3 for approx. 2 s.
   » All power LEDs should light up again and the phyCORE sends serial data from UART3 to the top DB-9 sub-connector of connector P1.

2.1.3.2.2 Power over Ethernet (PoE)

The Power-over-Ethernet (PoE) circuit provides a method of powering the board via the Ethernet interface. In this configuration the phyCORE-OMAP44xx Carrier Board acts as the Powered Device (PD) while the connecting Ethernet interface acts as the Power Source Equipment (PSE). For applications that require Ethernet connectivity this is an extremely convenient method to also simultaneously provide power. To make use of the PoE circuit you must have a PSE for connectivity. Typically a PoE enabled router or switch can be used. LED D18 indicates the availability of the PoE supply voltage.

The PoE circuit generates a supply voltage of 12 V, which is feed into the VCC_12_24 branch through a diode. The IEEE PoE standard restricts the maximum amount of power a PSE must provide and therefore a PD can consume. The phyCORE-OMAP44xx PoE circuit was designed to provide up to 25 W of power to the board.

The phyCORE-OMAP44xx Carrier Board Ethernet connector X9 supports both PSE power sourcing methods of power over the data wires, or power over the spare wires.

Caution:

The PoE circuit was designed to provide up to 25 W of power to the board. This is less than the board can potentially consume. Be aware that this limitation could cause board operation to fail if peak power is exceeded due to enabled peripherals. Do not supply the system over Ethernet, if the power consumption expected is more than 25 W ! Do not change modules or jumper settings while the carrier board is supplied with power over the Ethernet!

Note:

For powering up the phyCORE the following actions have to be done:
1. Plug in the POE supply connector
   » The power LEDs D14 - D18 should light up and the phyCORE sends serial data from UART3 to the top DB-9 sub-connector of connector P1.
2. For powering down the phyCORE-OMAP44xx button S3 should be pressed for a minimum time of 2000 ms.
3. To restart the system press button S3 for a maximum time of 1000 ms.
   » All power LEDs should light up again and the phyCORE sends serial data from UART3 to the top DB-9 sub-connector of connector P1.

2.1.3.2.3 Power Management

Switches S4 and S5 on the phyCORE-OMAP44xx Carrier Board support the features of the Power Management IC on the phyCORE-OMAP44xx. They connect to pins X1C44 (X_PMIC_PREQ2A)and X1C43 (X_PMIC_PREQ3) at the phyCORE-Connector. Please refer to Section 1.4.3.3 to learn more about the power management available on the phyCORE-OMAP44xx.

S4 Issues a **trigger** signal at pin X1C44 (X_PMIC_PREQ2A) of the phyCORE-OMAP44xx in order to switch power group 2[1]. Pressing this button will toggle the PREQ2A pin of the PMIC on the phyCORE-OMAP44xx LOW.

S5 Issues a **trigger** signal at pin X1C43 (X_PMIC_PREQ3) of the phyCORE-OMAP44xx in order to switch power group 31. Pressing this button will toggle the PREQ3 pin of the PMIC on the phyCORE-OMAP44xx LOW.

Note:

Signal X_PMIC_PREQ2A is also connected to the power management event signal (PME) of the Ethernet controller on the phyCORE-OMAP44xx. Please read Section 1.8.5.1 to get to know how to avoid conflicts when using switch S4.

2.1.3.2.4 Current Measurement

To facilitate current measurement at each voltage domain resistors R222 to R227 are provided as current access measurement points. To calculate the current draw the resulting voltage drop across the shunt resistors must be measured. Table 46 lists the voltage domains and the associated shunt resistors as well as the resistor values. The shunt resistors chosen are small enough to not affect the output voltage (it will be reduced by the voltage drop across the shunt), but large enough to have a discernible measurement from general noise.

Voltage domain	Shunt resistor	Value
VCC_5V	R226, R227	0,07 Ohm||0,07 Ohm => 0,035 Ohm
VCC_3V3	R224, R225	0,07 Ohm||0,07 Ohm => 0,035 Ohm
VCC_1V8	R222	0,07 Ohm
VCC_1V2	R223	0,07 Ohm

Table 46: Resistor Values for Current Measurement

1. All special functions of the PMIC such as use of power groups, etc. require the PMIC to be programmed via I^2C interface. At the time of delivery only the generation of the required voltages is implemented . Please refer to the TWL6030 Technical Ref. Man. for more information on how to program the PMIC.

2.1.3.3 Connectivity to Universal Asynchronous Interfaces (P1 + X5)

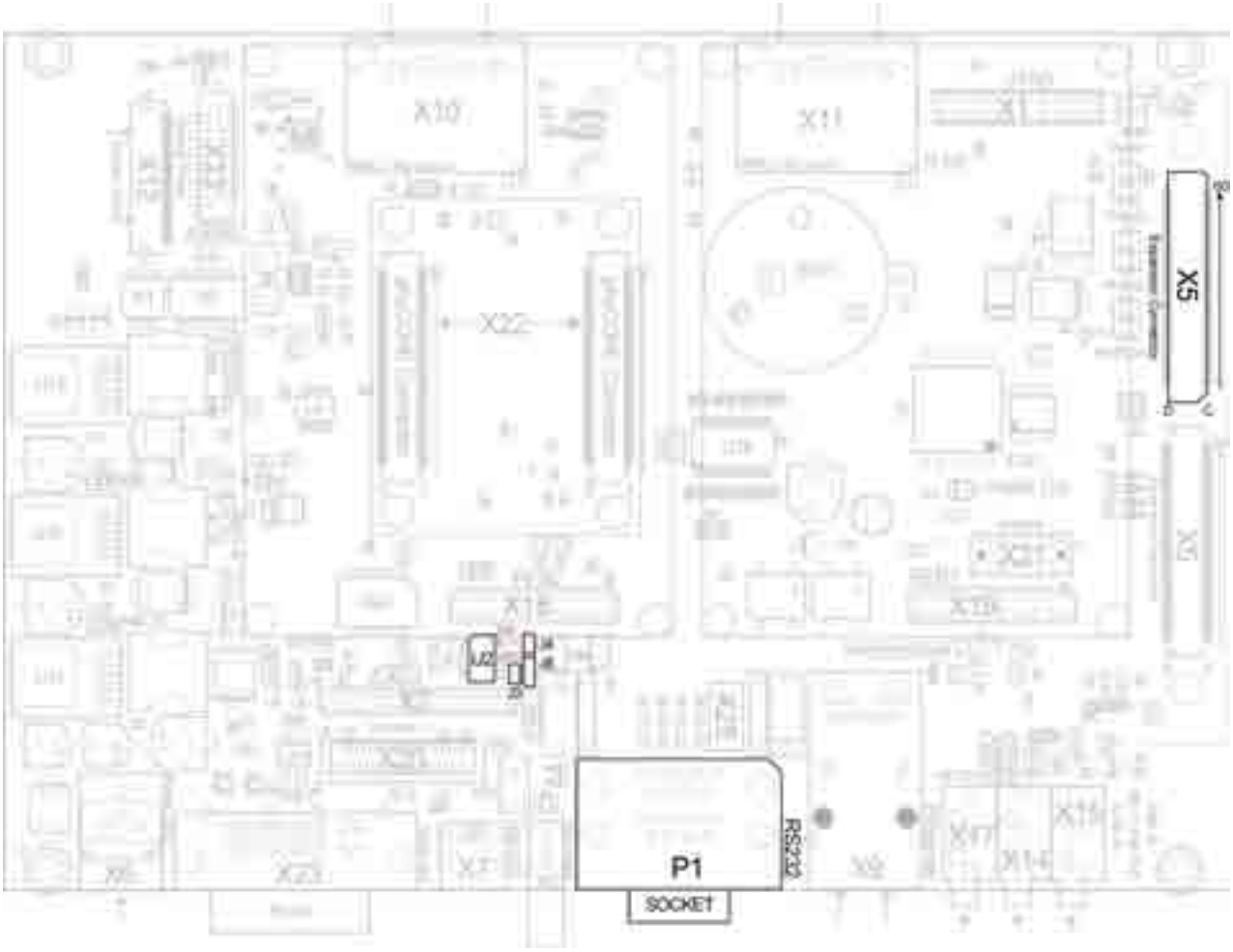


Figure 23: RS-232 Interface Connectors (P1, X5) and Jumpers

The phyCORE-OMAP44xx Carrier Board provides connectivity to three of the four universal asynchronous interfaces of the phyCORE-OMAP44xx. The signals of UART2 and UART3 are available on the Dual-Port Connector P1 at RS-232 level, whereas the signals of UART1 are brought out on the expansion connector X5 at TTL level.

Figure 24 shows the signal mapping of the two female DB-9 connectors at connector P1.

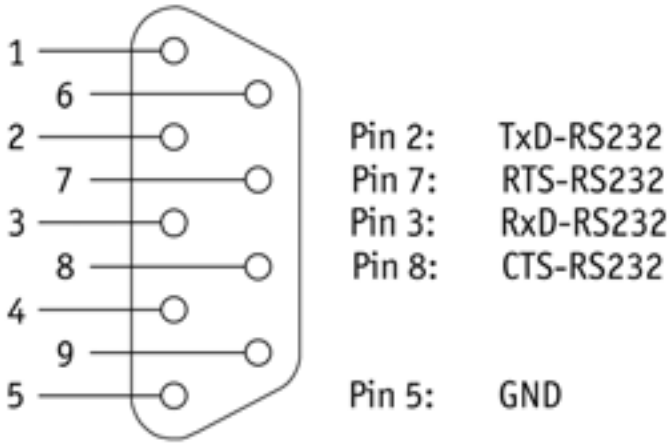


Figure 24: RS-232 connector P1 Signal Mapping

2.1.3.3.1 Connectivity to UART 1 (TTL)

The TTL level signals of UART1 extend directly from the phyCORE-Connector X22 (pins X22C10 and X22D10) to the expansion connector X5. UART1 of the OMAP44xx is not further used on the carrier board.

The following table shows the location of the signals on the expansion connector.

Pin #	Signal	I/O	SL	Description
X5C35	X_UART1_TX	O	VCC_1V8_IO	Serial transmit signal of UART 1
X5C36	X_UART1_RX	I	1.8 V	Serial receive signal of UART 1

Table 47: Mapping of the UART1 Signals on the Expansion Connector (X5)

2.1.3.3.2 Connectivity to UART 2 (RS-232)

The bottom DB-9 connector of the Dual-Port Connector P1 provides the UART2 signals of the OMAP44xx at RS-232 level. A MAX3380E RS-232 transceiver at U2 converts the TTL level signals from the phyCORE-OMAP44xx to RS-232 level signals. To protect the phyCORE-OMAP44xx a level shifter and a quad-channel isolator at U22 isolate the transceiver from the phyCORE. The interface is 5-wire including the signals RTS and CTS for hardware flow control.

The MAX3380E transceiver offers different operation modes including Maxim's AutoShutdown Plus™ feature to automatically enter a 1 µA shutdown mode. In AutoShutdown Plus™ mode the device shuts down the on-chip power supply and drivers when it does not sense a valid signal transition for 30 seconds on either the receiver or transmitter inputs. The signal inputs FORCEON and /FORCEOFF together with the /INVALID output signal control the different operation states of the MAX3380, as can be seen in Table 48. Jumpers J3, J4 and J8, as well as resistors R25 and R26 allow to configure the MAX3380 transceiver for the various operation modes. Table 49 shows the required settings.

2.1.3.3.3 Connectivity to UART 3 (RS-232)

The top DB-9 connector of the Dual-Port Connector P1 provides the UART3 signals of the OMAP44xx at RS-232 level. The interface is 5-wire including the signals RTS and CTS for hardware flow control. This RS-232 interface is hard-wired and no jumpers must be configured for proper operation, as the TTL level signals from the OMAP44xx are converted to RS-232 level on the phyCORE-OMAP44xx (see also Section 1.8.1).

UART3 of the phyCORE-OMAP44xx is used as monitoring/debug interface.

Note:

The RS-232 transceiver on the phyCORE-OMAP44xx is configured to operate in AutoShutdown mode, which means that it shuts down if invalid signals are detected (Please refer to Section 1.8.1 and the datasheet of the MAX3380E/MAX3381E for more information).

Operation Status	FORCEON	/FORCEOFF	Valid Receiver Level	Receiver or Transmitter Edge within 30 s	T_OUT	R_OUT
Shutdown (Forced Off)	X	0	X	X	High-Z	Active
Normal Operation (Forced On)	1	1	X	X	Active	Active
Normal Operation (AutoShutdown Plus)	0	1	X	Yes	Active	Active
Shutdown (AutoShutdown Plus)	0	1	X	No	High-Z	Active
Normal Operation	/INVALID	1	Yes	X	Active	Active
Normal Operation	/INVALID	1	X	Yes	Active	Active
Shutdown	/INVALID	1	No	No	High-Z	Active
Normal Operation (AutoShutdown)	/INVALID	/INVALID	Yes	X	Active	Active
Shutdown (AutoShutdown)	/INVALID	/INVALID	No	X	High-Z	Active

Table 48: Operation States of the RS-232 Transceiver MAX3380

Operation Mode	R25	R26	J3	J4	J8
Shutdown (Forced Off)	no matter	not mounted	not mounted	mounted	2+3
Normal Operation (Forced On)	mounted	mounted	not mounted	not mounted	not mounted
Normal Operation (AutoShutdown Plus™, shutdown after 30 s without receive, or transmit signal)	not mounted	mounted	mounted	not mounted	2+3
Normal Operation (shutdown after 30 s without receive, or transmit signal, or if signal is invalid)	not mounted	mounted	mounted	not mounted	1+2
Normal Operation (AutoShutdown, shutdown if signal is invalid)	**not mounted**	**not mounted**	**mounted**	**mounted**	**1+2**

Table 49: Possible Configurations of the MAX3380 RS-232 Transceiver

2.1.3.4 Ethernet Connectivity (X9)

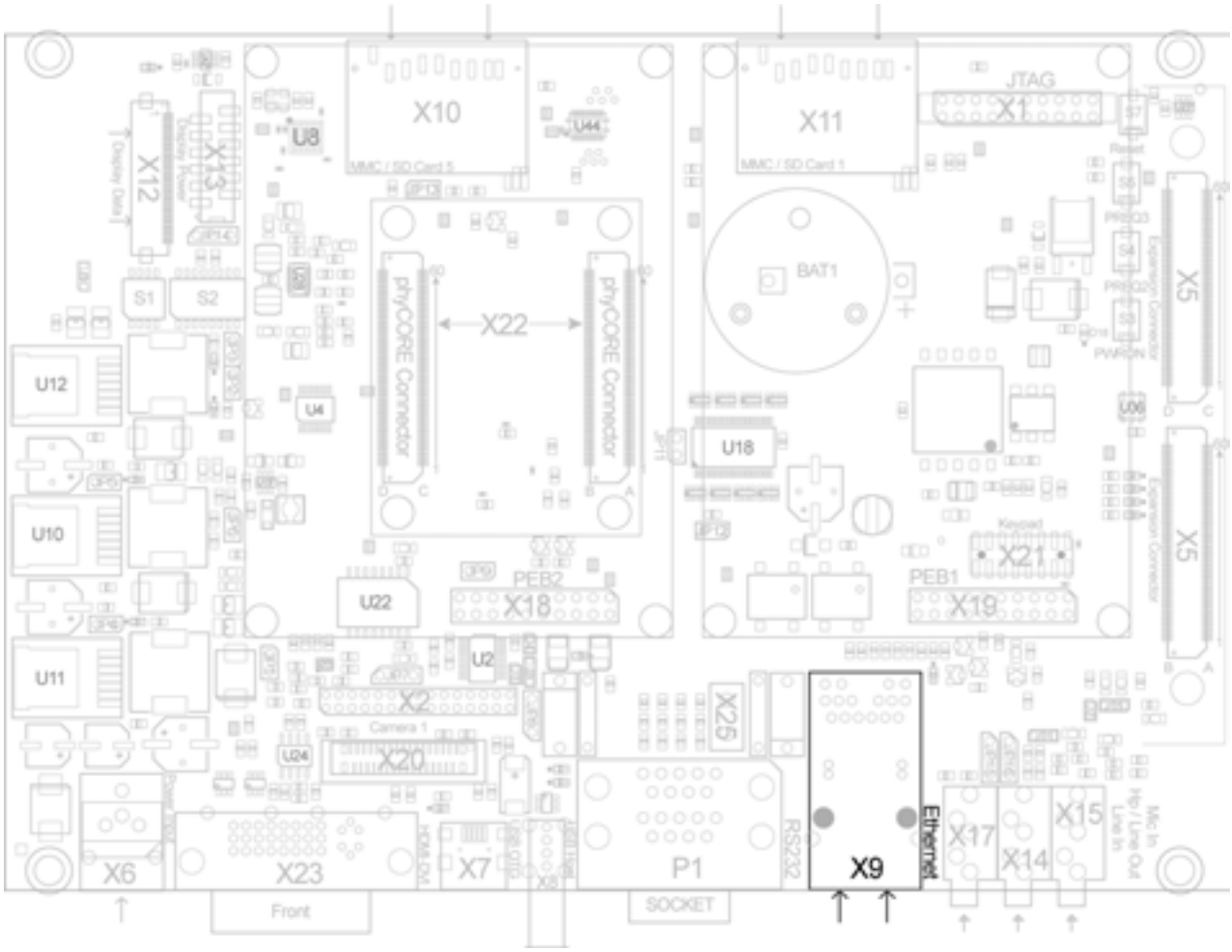


Figure 25: Ethernet Interface at Connector X9

The Ethernet interface of the phyCORE is accessible at an RJ-45 connector (X9) on the carrier board. Due to its characteristics this interface is hard-wired and can not be configured via jumpers. The LEDs for LINK (green) and SPEED (yellow) indication are integrated in the connector.

The required termination resistors for the Ethernet interface are assembled on the phyCORE-OMAP44xx. The Ethernet circuit includes a protective circuit to avoid a reverse current over the terminating resistors if the Ethernet controller's supply voltage VCC_3V3_S is turned off by the power management on the phyCORE-OMAP44xx. Please refer to Section 1.8.5.1 for more information.

The Ethernet interface also supports Power over Ethernet (PoE). Please refer to Section 2.1.3.2.2 for more information.

2.1.3.5 USB Host Connectivity (X8, X12,X18,X19)

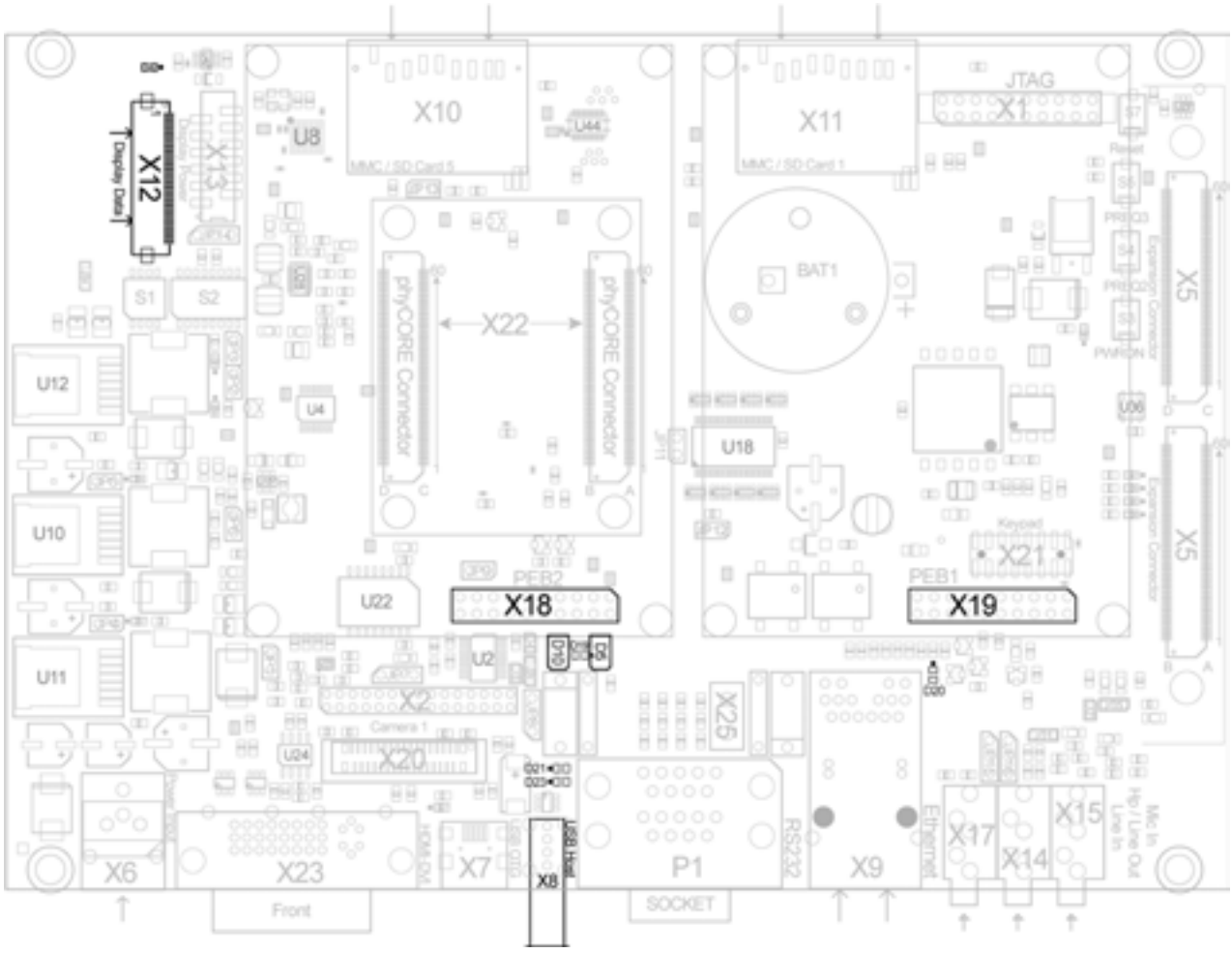


Figure 26: Components supporting the USB Host Interface

The USB Host interface of the phyCORE is accessible via the USB hub controller U7 on the carrier board. The controller supports control of input USB devices such as keyboard, mouse or USB key. The USB hub has 4 downstream facing ports. One port extends to the standard USB connector X8 (USB A). The remaining ports are accessible at the display data connector X12[1], as well as on the PEB connectors X18 and X19[2]. The latter three interfaces provide only data lines D+ and D-. They do not feature a supply line Vbus.

LEDs D19 to D23 as well as D5 and D10 signal use of the USB host interfaces. Table 40 shows the assignment of the LEDs to the different USB ports.

Table 50 shows the distribution of the seven downstream facing ports to the different connectors.

1. please refer to Table 51 to locate the signals on the display data connectors X12
2. please see Section 2.1.3.15

USB Hub Port #	Connector	Connector Type	LED
USB4	X12	40 pin FCC (pins 16 (D+) and 17 (D-))	D22
USB3	X18	20 pin header Row (pins 19 (D-) and 20 (D+))	D19
USB2	X19	20 pin header Row (pins 19 (D-) and 20 (D+))	D20
USB1	X8	USB A	D21

Table 50: Distribution of the USB Hub's (U7) Ports

2.1.3.6 USB OTG Connectivity (X7)

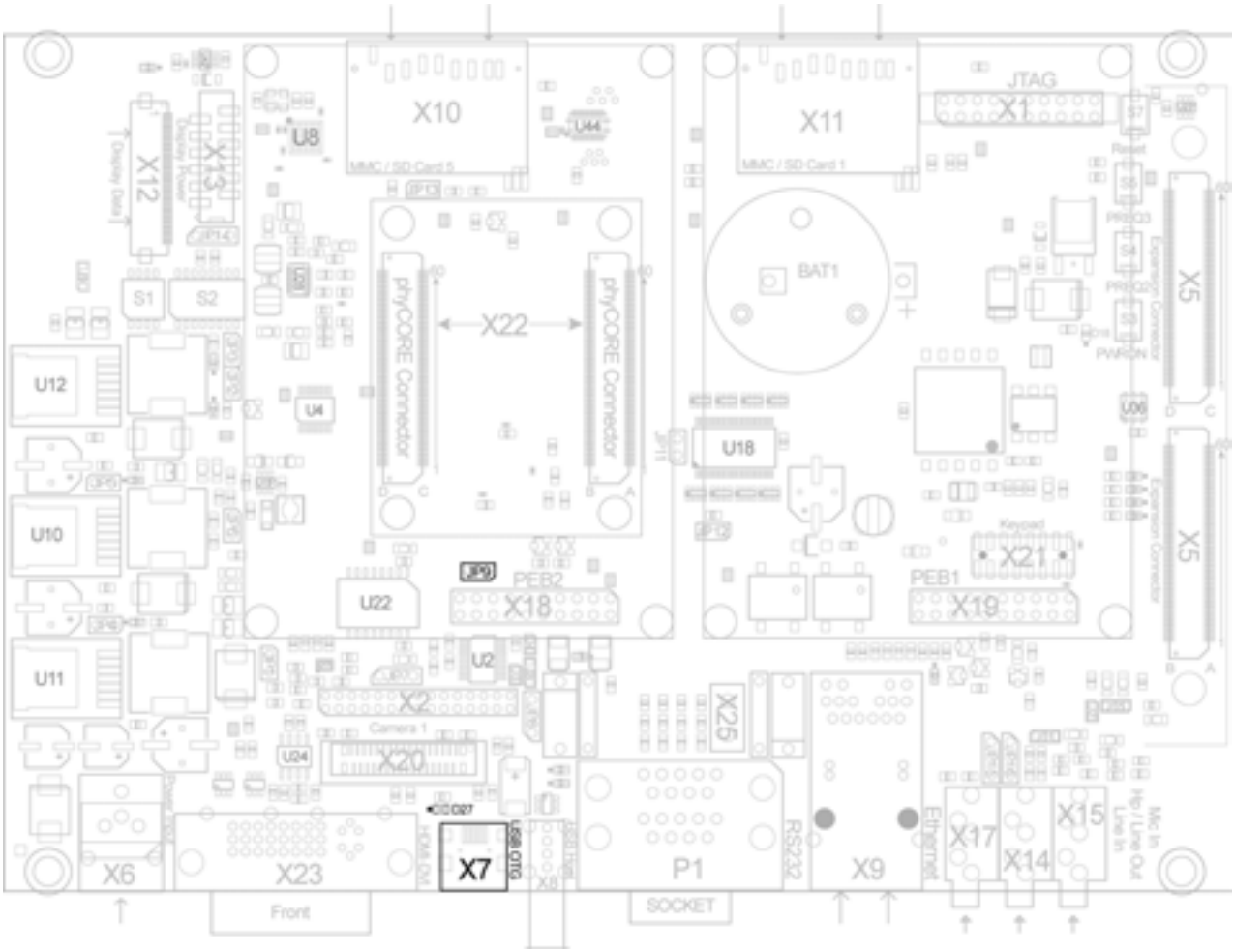


Figure 27: USB OTG Interface at Connector X7

The USB OTG interface of the phyCORE is accessible at connector X7 (USB Mini AB) on the carrier board. The phyCORE supports the On-The-Go feature. The Universal Serial Bus On-The-Go is a device capable to initiate the session, control the connection and exchange Host/Peripheral roles between each other. This interface is compliant with USB revision 2.0.

Two jumpers allow to configure the USB OTG interface. Jumper J5 on the backside of the carrier board (see Figure 19) connects the overcurrent signal USB_OTG_OC to pin X1D42 (X_SYS_NIRQ2 (GPIO183)) of the phyCORE-OMAP44xx making it possible to evaluate this signal. An overcurrent is detected if this signal is LOW. Removing jumper J5 allows to utilize GPIO 183 of the OMAP44xx for other purpose. Jumper JP9 configures the OTG operating mode. By default this jumper is open, which leaves the USB_OTG_ID pin floating, and thus configuring the OTG interface as slave. Alternatively this jumper can be closed, connecting USB_OTG_ID to GND, and configuring the OTG interface as host. Typically the configuration of a connecting device as host or slave is done automatically via a USB OTG cable. However, given the limited number of OTG enabled devices in the embedded market this jumper is provided to either simulate an OTG cable, or force the OTG interface into Host mode when OTG operation is not required.

LED D27 signals VBUS power output.

2.1.3.7 Display / Touch Connectivity (X12, X13)

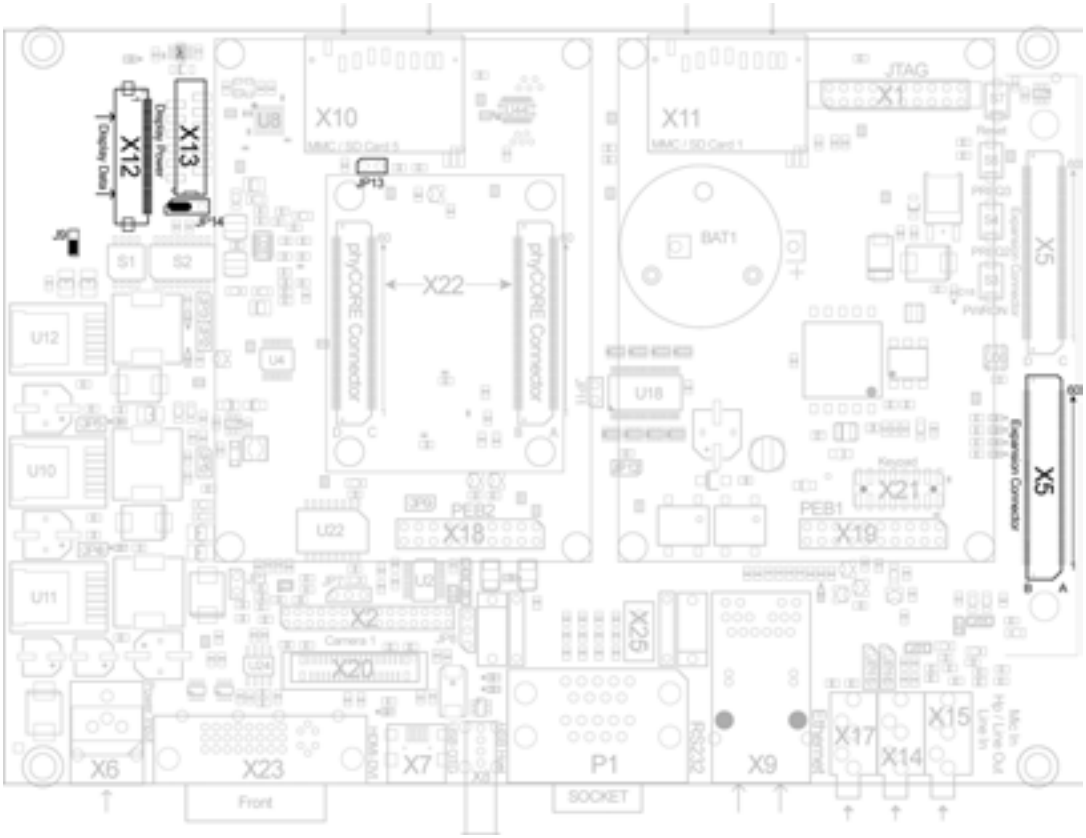


Figure 28: Display / Touch Connectivity (X12, X13)(top view)

Figure 29: Display / Touch Connectivity (X12, X13)(bottom view)

The phyCORE-OMAP44xx Carrier Board supports both display interfaces provided by the phyCORE-OMAP44xx. The parallel display interface and the DSI interface signals are converted into LVDS and are available at the PHYTEC Display -Interface (PDI) which is described in the following paragraph. In addition, the parallel display interface is available at expansion connector X5.

The various performance classes of the phyCORE family allow to attach a large number of different displays varying in resolution, signal level, type of the backlight, pin-out, etc. In order not to limit the range of displays connectable to the phyCORE, the phyCORE-OMAP44xx Carrier Board has no special display connector suitable only for a small number of displays. The new concept intends the use of an adapter board (e.g. PHYTECs LCD display adapters LCD-014 and LCD-017) to attach a special display, or display family to the phyCORE. A new Phytec Display-Interface (PDI) was defined to connect the adapter board to the phyCORE-OMAP44xx Carrier Board. It consists of two universal connectors which provide the connectivity for the display adapter. They allow easy adaption also to any customer display adapter. One connector (40 pin FCC connector 0.5mm pitch) at X12 is intend for connecting all data signals to the display adapter. It combines various interface signals like LVDS, USB, I^2C, etc. required to hook up a display. The second connector of the PDI (AMP microMatch 8-338069-2) at X13 provides all supply voltages needed to supply the display and a backlight, and the brightness control.

The following sections contain specific information on each connector.

2.1.3.7.1 PDI Data Connector (X12)

PDI data connector X12 provides display data from the parallel display interface, or the DSI1 interface of the OMAP44xx. After the signals from either display interface are converted to LVDS two multiplexer at U51 and U52 forward the LVDS signals to the PDI data connector. Jumper JP13 allows to select which data is forwarded.

If jumper JP13 is open PDI data connector X12 provides the display signals from the parallel display interface of the phyCORE-OMAP44xx (see Section 1.11.1). These signals are converted into LVDS by the Texas Instruments SN75LVDS83B FlatLink™ transmitter at U32. The SN75LVDS83B is a 4-channel 24-bit LVDS transmitter and supports displays up to 1366x768 24-bit pixel resolution. Jumper J20 allows to select either rising, or falling edge strobe for the input clock signal of the FlatLink™ transmitter. The default configuration selects rising edge strobe (see Table 41 for details).

The signals of the parallel display interface are also available at expansion connector X5 to allow for designing a custom specific display interface. Please refer to Section 2.1.3.21.

Note:

If the parallel display interface of the phyCORE-OMAP44xx is intend to be used with a custom hardware connected to expansion connector X5 closing jumper JP14 at position 2+3 shuts down the FlatLink™ transmitter. This allows to avoid signal conflicts and to reduce disturbances.

If jumper JP13 is closed data from the OMAP44xx's DSI1 interface is forwarded to the PDI data connector X12. The DSI interface of the phyCORE-OMAP44xx (refer to Section 1.11.2) extends to the Toshiba TC358764 DSI2LVDS Bridge Chip mounted at U8 on the phyCORE-OMAP44xx Carrier Board. This chip functions primarily as a DSI-to-LVDS communication protocol bridge, allowing to connect an LVDS display to the DSI1 Display Interface of the OMAP44xx. The DSI-RX receiver supports from 1- to 4-Lane configurations and the LVDS transmitter displays up to 1366 x 768 24-bit pixel resolution. The TC358764 can be configured via I^2C interface (I2C4) at address 0x0F. It also features a test mode, which can be entered by closing jumper J7 at 1+2 (Please refer to the TC358764 "Functional Specification" for more information). The default configuration

selects normal operation (see Table 41 for details).

At the time of delivery jumper JP13 is open, consequently data from the parallel display interface is available at PDI data connector X12.

In addition other useful interfaces such as USB, I^2C, etc. are available at PDI data connector X12. Table 52 lists all miscellaneous signals and gives detailed explanations.

The following table shows the pin-out of the PDI's display data connectors at X12.

Pin #	Signal	I/O	SL	Description
1	SPI1_CLK_3V3	O	3.3 V	SPI 1 clock
2	SPI1_MISO_3V3	I/O	3.3 V	SPI 1 master data in; slave data out
3	SPI1_MOSI_3V3	O/I	3.3 V	SPI 1 master data out; slave data in
4	SPI1_CS2_3V3	O	3.3 V	SPI 1 chip select display adapter
5	DISP_IRQ	I	3.3 V	SPI interrupt input (connected to GPIO 64 of the OMAP44xx (X1D34 on the phyCORE-Connector))
6	VCC_3V3	O	3.3 V	Logic supply voltage[1]
7	I2C4_SCL_3V3	I/O	3.3 V	I^2C clock signal
8	I2C4_SDA_3V3	I/O	3.3 V	I^2C data signal
9	GND	-	-	Ground
10	LS_BRIGHT	O	3.3 V	PWM brightness control
11	VCC_3V3	O	3.3 V	Logic supply voltage1
12	/PWR_KEY	I	3.3 V	Power on/off signal
13	/DISP_ENA	O	3.3 V	Display enable signal
14	X_1-WIRE_3V3	I/O	3.3 V	Hardware Introspection Interface **for internal use only**
15	GND	-	-	Ground
16	USB1DN_DP4	I/O	3.3 V	USB data + (port 4 of the USB hub at U7)[2]
17	USB1DN_DM4	I/O	3.3 V	USB data - (port 4 of the USB hub at U7)2
18	GND	-	-	Ground
19	DISP_LVDS_0-	O	3.3 V	LVDS data channel 0 negative output

Table 51: PDI Display Data Connector X12 Signal Description

Pin #	Signal	I/O	SL	Description
20	DISP_LVDS_0+	O	3.3 V	LVDS data channel 0 positive output
21	GND	-	-	Ground
22	DISP_LVDS_1-	O	3.3 V	LVDS data channel 1 negative output
23	DISP_LVDS_1+	O	3.3 V	LVDS data channel 1 positive output
24	GND	-	-	Ground
25	DISP_LVDS_2-	O	3.3 V	LVDS data channel 2 negative output
26	DISP_LVDS_2+	O	3.3 V	LVDS data channel 2 positive output
27	GND	-	-	Ground
28	DISP_LVDS_3-	O	3.3 V	LVDS data channel 3 negative output
29	DISP_LVDS_3+	O	3.3 V	LVDS data channel 3 positive output
30	GND	-	-	Ground
31	DISP_LVDS_CLK-	O	3.3 V	LVDS clock channel negative output
32	DISP_LVDS_CLK+	O	3.3 V	LVDS clock channel positive output
33	GND	-	-	Ground
34	TS_X+	I/O	3.3 V	Touch
35	TS_X-	I/O	3.3 V	Touch
36	TS_Y+	I/O	3.3 V	Touch
37	TS_Y-	I/O	3.3 V	Touch
38	n.c.	-	-	not connected
39	GND	-	-	Ground
40	LS_ANA	I	3.3 V	Light sensor analog input

Table 51: PDI Display Data Connector X12 Signal Description

1. Provided to supply any logic on the display adapter. Max. draw 100 mA
2. LED D22 signals use of this USB interface

The table below shows the auxiliary interfaces at display data connector X12.

Signal	Description
USB1DN	USB host interface derived from port 4 of the USB hub at U7. Suitable for optional features e.g. front USB (refer to Section 2.1.3.5 for more information about the USB host interfaces)
I2C4	I^2C interface for a optional EEPROM, or other I^2C devices (additional information on the I^2C interfaces can be found in Section 2.1.3.11)
SPI1	SPI interface to connect optional SPI slave
1-WIRE	Hardware Introspection Interface **for internal use only**
/PWR_KEY	Power on/off signal to allow for an ON/OFF switch on a front panel. It connects to the PWRON input of the PMIC (X1C9 on the phyCORE-Connector) and to GPIO 181 (X1B13 on the phyCORE-Connector) of the OMAP44xx
/DISP_ENA	Can be used to enable, or disable the display, or to shutdown the backlight. /DISP_ENA is connected to GPIO 118 (X1B36 on the phyCORE-Connector) of the OMAP44xx
LS_BRIGHT	PWM output to control the brightness of a display's backlight (0% = dark, 100% = bright). This signal is connected to the phyCORE's X_DMTIMER9_PWM_EVT output at X22A43 meaning that the PWM signal can be generated by general-purpose timer GPT9 of the OMAP44xx[1]
LS_ANA	Analog light sensor input. The analog light sensor input at pin 40 extends to an 8-bit A/D converter (U42) which is connected to the I^2C bus I2C4 at address 0x64. To get the maximum adjustment range the output voltage of an applicable light sensor should range from 0 V to V_{Ref} (VCC_3V3AD).

Table 52: Auxiliary Interfaces at PDI Data Connector X12

1. Jumper J6 on the phyCORE-OMAP44xx must be configured at 1+2 to have this signal available (see Table 5)

2.1.3.7.2 PDI Power Connector (X13)

The display power connector X13 (AMP microMatch 8-338069-2) provides all supply voltages needed to supply the display and a backlight, and the brightness control.

Pin #	Signal	I/O	SL	Description
1	GND	-	-	Ground
2	VCC_3V3	O	3.3 V	3.3 V power supply display
3	GND	-	-	Ground
4	VCC_5V	O	5 V	5 V power supply display
5	GND	-	-	Ground
6	VCC_5V	O	5 V	5 V power supply display
7	GND	-	-	Ground
8	VCC_5V	O	5 V	5 V power supply display
9	GND	-	-	Ground
10	LS_BRIGHT	O	3.3 V	PWM brightness output[1]
11	VCC_12_24	O	+12 V - +24 V	Power Supply for backlight; corresponds to the input voltage at power jack X6
12	VCC_12_24	O	+12 V - +24 V	Power Supply for backlight; corresponds to the input voltage at power jack X6

Table 53: PDI Power Connector X32 Signal Description

1. (refer to Table 52 for detailed information)

Caution:

There is no protective circuitry for the backlight. The output for the backlight supply voltage connects directly to the main power input at X6. Thus the main supply voltage must match the input voltage of your backlight power circuitry.

2.1.3.7.3 Touch Screen Connectivity

As many smaller applications need a touch screen as user interface, provisions are made to connect 4-wire resistive touch screens to the PDI data connector X12 (pins 34 - 37, refer to Table 51). The signals from the touch screen panel are processed by a STMPE811 touch panel controller at U41. The touch panel controller is connected to I^2C bus I2C4 at address 0x41. By changing jumper J9 the address can be set to 0x44 if needed (refer to Table 41).

An additional interrupt output is connected to GPIO 117 (X1A39 on the phyCORE-Connector) of the OMAP44xx.

2.1.3.8 HDMI - DVI Connectivity (X23)

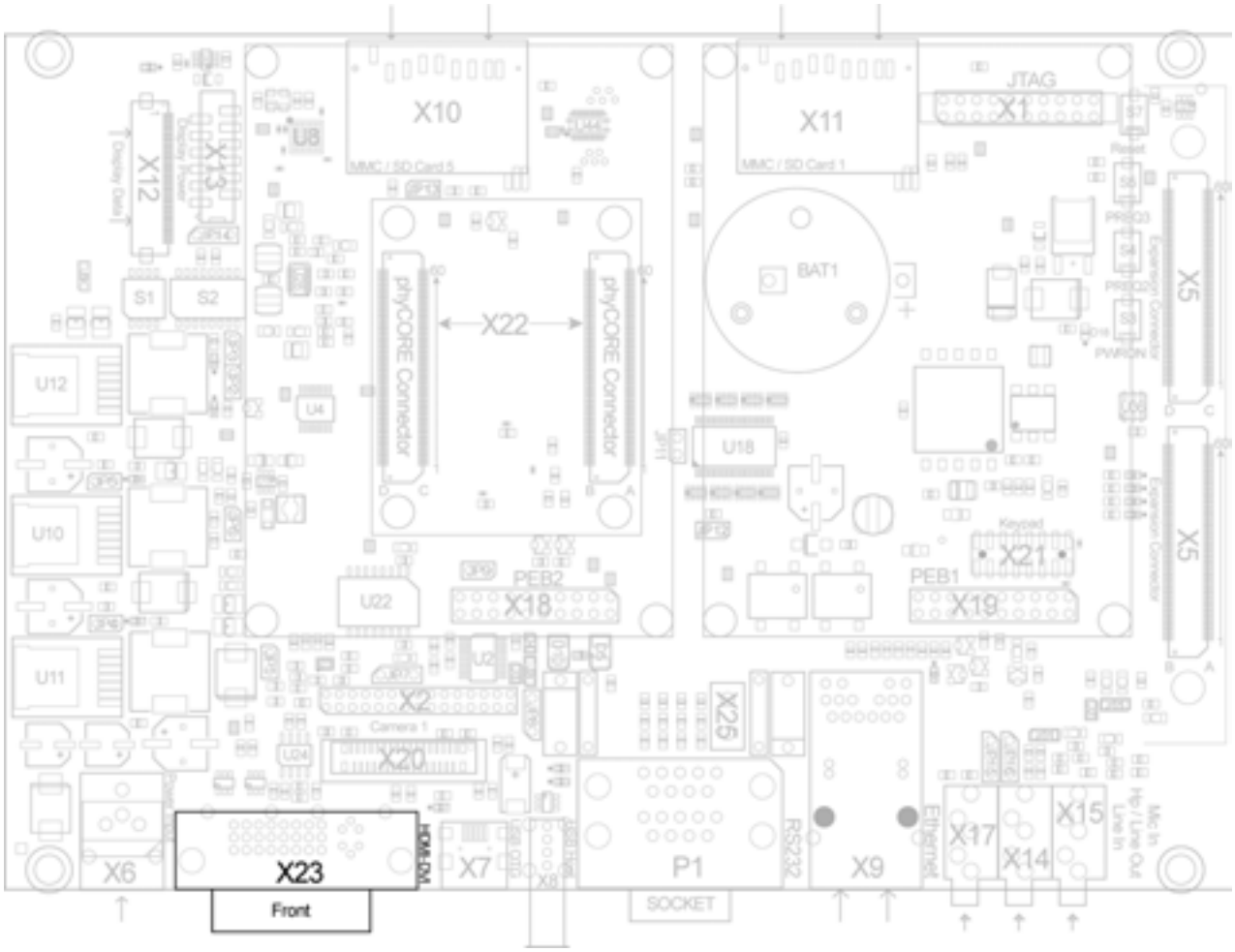


Figure 30: HDMI - DVI Connectivity (X23)

The phyCORE-OMAP44xx provides a HDMI 1.3 and DVI 1.0 compliant interface. The HDMI module of the OMAP44xx converts the RGB video into standard high-definition digital video format. The HDMI interface brought out at DVI female connector X23 on phyCORE-OMAP44xx Carrier Board comprises the following signal groups: three pairs of data signals, one pair of clock signals, an I^2C bus which is exclusively for the HDMI interface, and the hot plug detect (HPD) signal. Level shifters shift the I^2C interface signals and the hot plug detect signal from the IO voltage (VCC_1V8IO) to 5 V, while the data and clock signals extend directly from the phyCORE-Connector to the DVI receptacle.

Pin #	Signal	I/O	SL	Description
1	X_HDMI_DATA2X	O	HDMI	HDMI data channel 2 negative output
2	X_HDMI_DATA2Y	O	HDMI	HDMI data channel 2 positive output
3	GND	-	-	Ground
4	NC	-	-	not connected
5	NC	-	-	not connected
6	DDCCLK	I/O	5 V	HDMI I²C clock signal
7	DDCDATA	I/O	5 V	HDMI I²C data signal
8	NC	-	-	not connected
9	X_HDMI_DATA1X	O	HDMI	HDMI data channel 1 negative output
10	X_HDMI_DATA1Y	O	HDMI	HDMI data channel 1 positive output
11	GND	-	-	Ground
12	NC	-	-	not connected
13	NC	-	-	not connected
14	VCC_5V	O	5 V	5V power supply
15	GND	-	-	Ground
16	HDMI_HPD	I	5 V	HDMI hot plug detection
17	X_HDMI_DATA0X	O	HDMI	HDMI data channel 0 negative output
18	X_HDMI_DATA0Y	O	HDMI	HDMI data channel 0 positive output
19	GND	-	-	Ground
20	NC	-	-	not connected
21	NC	-	-	not connected
22	GND	-	-	Ground
23	X_HDMI_CLOCKY	O	HDMI	HDMI clock positive output
24	X_HDMI_CLOCKX	O	HDMI	HDMI clock negative output
C1	NC	-	-	not connected
C2	NC	-	-	not connected
C3	NC	-	-	not connected
C4	NC	-	-	not connected
C5	NC	-	-	not connected

Table 54: DVI Connector X23

Pin #	Signal	I/O	SL	Description
S1	PE	-	-	Earth
S2	PE	-	-	Earth
S3	PE	-	-	Earth
S4	PE	-	-	Earth
S5	PE	-	-	Earth
S6	PE	-	-	Earth

Table 54: DVI Connector X23

2.1.3.9 Camera Interfaces (X4, X5)

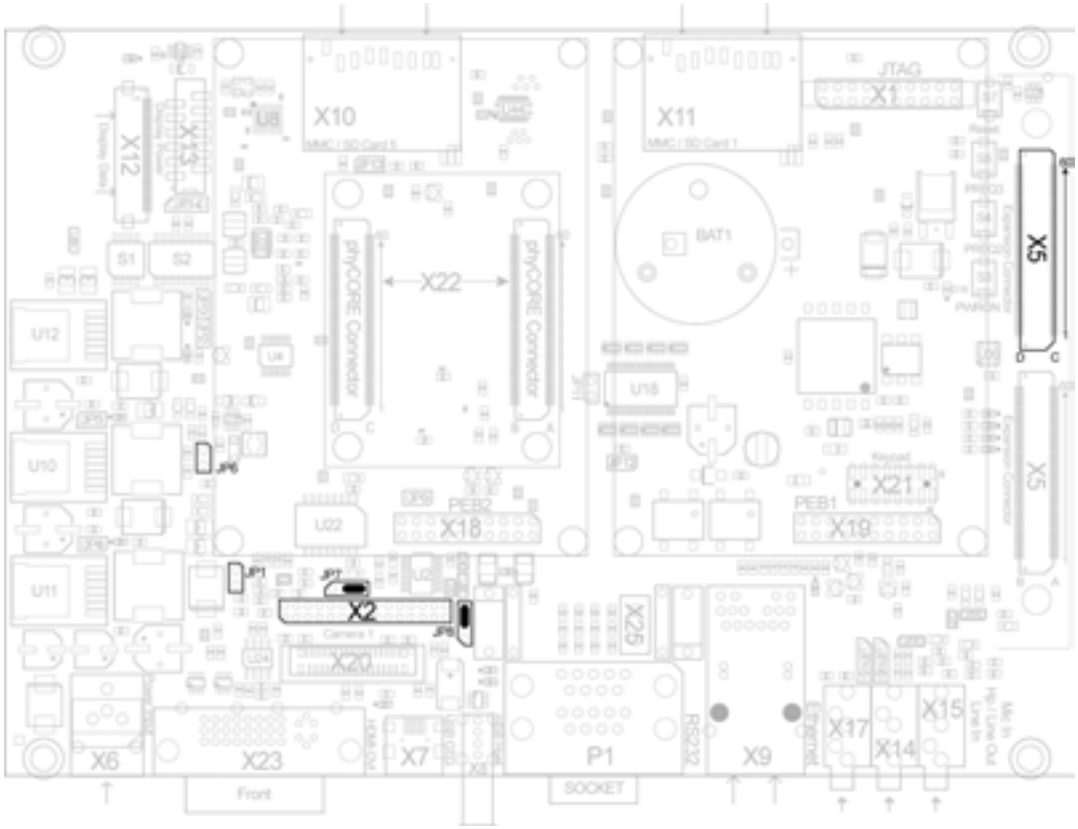


Figure 31: Camera Interfaces (top view)

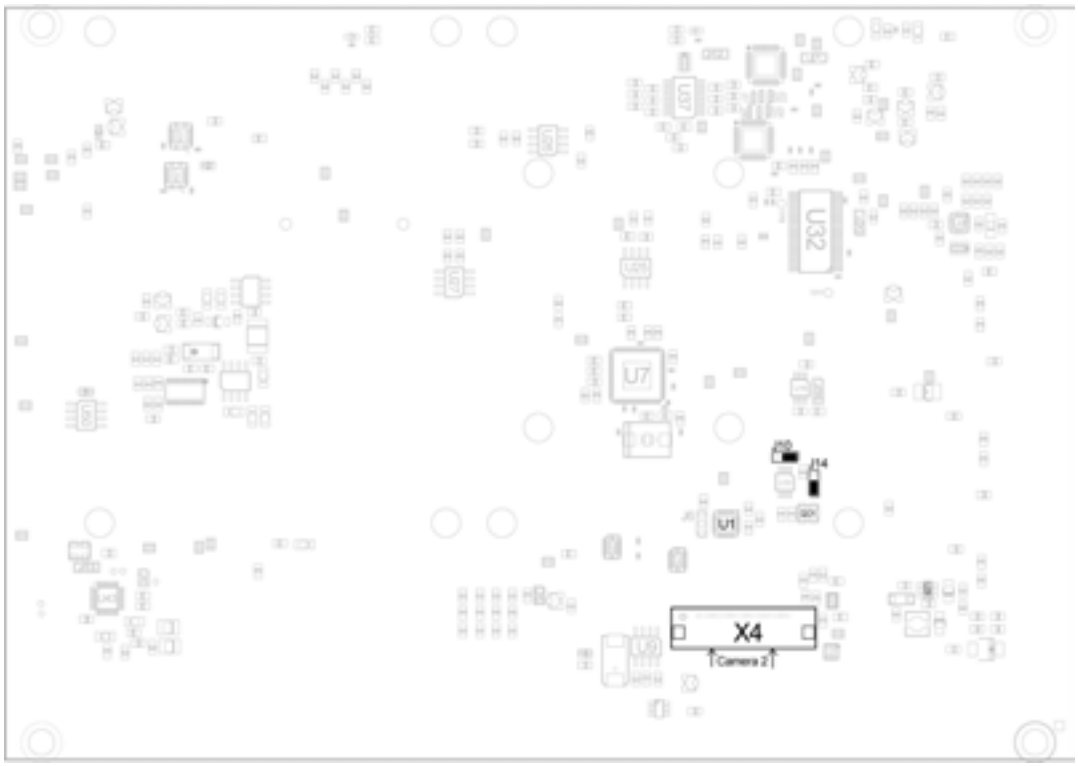


Figure 32: Camera Interfaces (bottom view)

The phyCORE-OMAP44xx Carrier Board provides connectivity for both camera interfaces of the phyCORE-OMAP44xx. The primary camera interface (CSI2-A/ CSI21) is available at expansion connector X5, whereas the secondary camera interface (CSI2-B/CCP2) is connected to FFC connector X4 on the backside of the board.

2.1.3.9.1 Primary Camera Interface CSI2-A/CSI21 (X5)

The primary camera interface (CSI2-A/CSI21) of the OMAP44xx is brought out directly at the expansion connector X5. The following table shows the location of the signals on the connector. A complete list of the signals available at the expansion connector X5 can be found in chapter Section 2.1.3.21.

Pin #	Signal	I/O	SL	Description
X5C18	X_CSI21_DX0	I	CSI	CSI2-A (CSI21) differential clock positive input
X5C19	X_CSI21_DY0	I	CSI	CSI2-A (CSI21) differential clock negative input
X5C20	X_CSI21_DX1	I	CSI	CSI2-A (CSI21) differential data lane positive input 1
X5C21	X_CSI21_DY1	I	CSI	CSI2-A (CSI21) differential data lane negative input 1
X5C22	X_CSI21_DX2	I	CSI	CSI2-A (CSI21) differential data lane positive input 2
X5C23	X_CSI21_DY2	I	CSI	CSI2-A (CSI21) differential data lane negative input 2
X5C24	X_KPD_COL4_CSI21_DX3	O/I	VCC_1V8_IO / CSI	Keyboard column 4 (open drain) / CSI2-A (CSI21 differential data lane positive input 3 (see note below)
X5C25	X_KPD_ROW4_CSI21_DY3	I	1.8 V / CSI	Keyboard row 4 / CSI2-A (CSI21) differential data lane negative input 3 (see note below)
X5C26	X_KPD_COL5_CSI21_DX4	O/I	VCC_1V8_IO / CSI	Keyboard column 5 (open drain) / CSI2-A (CSI21) differential data lane positive input 4 (see note below)
X5C27	X_KPD_ROW5_CSI21_DY4	I	1.8 V / CSI	Keyboard row 5 / CSI2-A (CSI21) differential data lane negative input 4 (see note below)

Table 55: Primary Camera Interface CSI2-A/CSI21 at Expansion Connector X5

Note:

Pins X1B5 to X1B8 on the phyCORE-Connector provide either signals of the keyboard interface, or camera lanes 3 and 4 of the primary camera interface. The resistor array JN1 on the phyCORE-OMAP44xx allows to choose which signals are brought out at these pins. In order to use lanes 3 and 4 of the primary camera interface JN1 must be set to position 2. Please refer to Figure 6 to see where JN1 is located.

The next table shows the supplementary signals related to the camera interface (I^2C, STROBE, SHUTTER, etc.) which are also available at the expansion connector X5.

Pin #	Signal Name	I/O	SL	Description
X5C10	CAM-1_SCL	I/O	VCC_CAM-1	Camera_1 I^2C clock signal[1]
X5C11	CAM-1_SDA	I/O	VCC_CAM-1	Camera_1 I^2C data signal1
X5C13	CAM-1_CTRL1	-	-	Camera_1 control signal 1
X5C14	CAM-1_CTRL2	-	-	Camera_1 control signal 2
X5C15	X_CAM_STROBE	O	VCC_1V8_IO	Camera flash activation trigger
X5C16	X_CAM_SHUTTER	O	VCC_1V8_IO	Mechanical shutter control signal
X5C17	X_CAM_GLOBAL_RESET	I/O	1.8 V / VCC_1V8_IO	Camera sensor reset

Table 56: CSI2-A/CSI21 Supplementary Signals at Expansion Connector X5

1. To use the Camera_1 I^2C interface JP6 must be closed to have VCC_CAM_1 available.

Note:

The function of camera control signals CAM-1_CTRL1 and CAM-1_CTRL2 depends on the camera board used. Connector X2 allows to connect them either to GND, or VCC_CAM-1 (only available at X2 if jumper JP6 is closed) or any other signal needed. Please refer to the hardware manual delivered with your camera board for precise information on theses signals and their function.

2.1.3.9.2 Secondary Camera Interface CSI2-B/CSI22 (X4)

The secondary camera interface (CSI2-B/CSI22) of the phyCORE-OMAP44xx is available at FFC connector X4 (Camera_2 interface of the phyCORE-OMAP44xx carrier board), which is compatible to PHYTEC's phyCAM-P camera interface standard. It provides connectivity to an 8-bit parallel camera interface. The camera serializer at U1 (SN65LVDS315RGER) converts the 8-bit parallel camera data to MIPI-CSI1 compliant serial data. The serialized data is available on the differential serial data output DOUT which connects to the CSI2-B/CSI22 camera interface of the phyCORE-OMAP44xx.

The phyCAM-P camera interface provides also an I^2C interface to control the image sensor of the camera module. It connects to the I2C3 I^2C bus of the phyCORE-OMAP44xx.

The supply voltage for the camera module ranges from 1.8 V to 3.3 V depending on the camera module attached to the secondary camera interface. A step-down switching regulator at U29 adjusts the camera supply voltage automatically according to the resistor connected to the camera module's "Power Voltage Set" output (input CAM-2_VSET on camera connector X4). To attach the supply voltage to the Camera_2 interface circuitry jumper JP1 must be closed.

Pin #	Signal	I/O	SL	Description
1	VCC_CAM-2	O	1.8 V - 3.3 V	Camera_2 supply voltage
2	VCC_CAM-2	O	1.8 V - 3.3 V	Camera_2 supply voltage
3	CAM-2_VSET	I	VCC_CAM-2	Configuration input for the camera supply voltage
4	CAM-2_CTRL-2	I/O	-	Camera_2 control signal 2
5	CAM-2_MCLK	O	VCC_CAM-2	Camera_2 main clock
6	GND	-	-	Ground
7	CAM-2_PCLK	I	VCC_CAM-2	Camera_2 pixel clock
8	GND	-	-	Ground
9	NC	-	-	not connected
10	NC	-	-	not connected
11	GND	-	-	Ground
12	CAM-2_DD2	I	VCC_CAM-2	Camera_2 data input 2
13	CAM-2_DD3	I	VCC_CAM-2	Camera_2 data input 3
14	GND	-	-	Ground
15	CAM-2_DD4	I	VCC_CAM-2	Camera 2 data input 4
16	CAM-2_DD5	I	VCC_CAM-2	Camera_2 data input 5
17	GND	-	-	Ground
18	CAM-2_DD6	I	VCC_CAM-2	Camera_2 data input 6
19	CAM-2_DD7	I	VCC_CAM-2	Camera_2 data input 7
20	GND	-	-	Ground
21	CAM-2_DD8	I	VCC_CAM-2	Camera_2 data input 8
22	CAM-2_DD9	I	VCC_CAM-2	Camera 2 data input 9
23	GND	-	-	Ground
24	CAM-2_HS	I	VCC_CAM-2	Camera_2 horizontal sync
25	CAM-2_VS	I	VCC_CAM-2	Camera_2 vertical sync
26	GND	-	-	Ground
27	CAM-2_CTRL1	O	-	Camera_2 control signal 1
28	CAM-2_SCL	O	VCC_CAM-2	Camera_2 I^2C clock line
29	CAM-2_SDA	I/O	VCC_CAM-2	Camera_2 I^2C data line
30	GND	-	-	Ground
31	CAM-2_RST	O	VCC_CAM-2	Camera_2 reset
32	VCC_CAM-2	O	1.8 V - 3.3 V	Camera_2 supply voltage
33	VCC_CAM-2	O	1.8 V - 3.3 V	Camera_2 supply voltage

Table 57: Secondary Camera Interface CSI-B/CSI22 at Camera Connector X4

The clock signal of the camera interface can be derived from either a 26 MHz oscillator at QO1, or from the X_FREF_CLK4_OUT signal (pin X1D43) of the phyCORE-OMAP44XX. The clock source can be configured with jumper J14. In the default configuration (position 1+2) the oscillator at QO1 (26 MHz) is selected as clock source.

Configuring the trigger of the camera reset is also possible. Jumper J10 connects the reset output of the phyCAM-P interface to the main system reset (X_nRESET_PWRON), or to the OMAP44xx's specially dedicated reset output (cam_globalreset) at pin X1B11 (X_CAM_GLOBAL_RESET) of the phyCORE-OMAP44xx. At the time of delivery jumper J10 is closed at 1 + 2 which selects the main system reset (X_nRESET_PWRON).

Camera control signals CAM-2_CTRL1 and CAM-2_CTRL2 support different features which vary according to the camera module connected. Jumpers JP7 (for CAM-2_CTRL1) and JP8 (for CAM-2_CTRL2) allow to connect them either to GND, VCC_CAM-2, or to leave them unconnected. Please refer to the hardware manual delivered with your camera board for precise information which configuration is needed for your camera module. The default setting of jumpers JP7 and JP8 is 2+ 3 which connects the camera control signals to GND.

2.1.3.9.3 Camera Auxiliary Connector (X2)

The camera auxiliary connector X2 can be used to configure camera control signals CAM-1_CTRL1 and CAM-1_CTRL2. They are available at expansion connector X5 to support implementation of a custom camera interface using the primary camera interface (CSI2-A/CSI21) of the OMAP44xx. Removable jumpers can be used to connect CAM-1_CTRL1 and CAM-1_CTRL2 to GND, or VCC_CAM-1[1] . Pin 30 (CAM-1_VSET) can be used to adjust VCC_CAM-1 to meet the voltage required for your camera module (refer to the hardware manual delivered with your camera board for precise information which configuration is needed and how to adjust the voltage). Leaving pin 30 open results in a voltage level of 1.25 V at VCC_CAM-1 .

All other pins of the camera auxiliary connector X2 are reserved for future use and should be left open.

Pin #	Signal Name	I/O	SL	Description
1	VCC_3V3	O	3.3 V	Power supply
2	VCC_3V3	O	3.3 V	Power supply
3	VCC_CAM-1	O	VCC_CAM-1	Camera power supply
4	VCC_CAM-1	O	VCC_CAM-1	Camera power supply
5	CAM-1_CTRL1	-	-	Camera control line 1
6	CAM-1_CTRL2	-	-	Camera control line 2
7	GND	-	-	Ground
8	GND	-	-	Ground
9	CAM-1_SDA	I/O	VCC_CAM-1	Reserved for future use
10 x	CAM-1_SCL	I/O	VCC_CAM-1	Reserved for future use
11	/CAM-1_RST	O	VCC_CAM-1	Reserved for future use
12	CAM-1_VS	I	VCC_CAM-1	Reserved for future use
13	CAM-1_HS	I	VCC_CAM-1	Reserved for future use
14	GND	-	-	Ground

Table 58: Camera Auxiliary Connector X2

1. JP6 must be closed to have VCC_CAM_1 available at the camera auxiliary connector X2

Pin #	Signal Name	I/O	SL	Description
15	CAM-1_DD9	I	VCC_CAM-1	Reserved for future use
16	CAM-1_DD8	I	VCC_CAM-1	Reserved for future use
17	CAM-1_DD7	I	VCC_CAM-1	Reserved for future use
18	CAM-1_DD6	I	VCC_CAM-1	Reserved for future use
19	CAM-1_DD5	I	VCC_CAM-1	Reserved for future use
20	CAM-1_DD4	I	VCC_CAM-1	Reserved for future use
21	CAM-1_DD3	I	VCC_CAM-1	Reserved for future use
22	CAM-1_DD2	I	VCC_CAM-1	Reserved for future use
23	CAM-1_DD1	I	VCC_CAM-1	Reserved for future use
24	CAM-1_DD0	I	VCC_CAM-1	Reserved for future use
25	GND	-	-	Ground
26	CAM-1_PCLK	I	VCC_CAM-1	Reserved for future use
27	GND	-	-	Ground
28	CAM-1_MCLK	O	VCC_CAM-1	Reserved for future use
29	GND	-	-	Ground
30	CAM-1_VSET	I	-	Camera supply voltage configuration

Table 58: Camera Auxiliary Connector X2

2.1.3.10 Audio Connectivity (X5, X14, X15, X17)

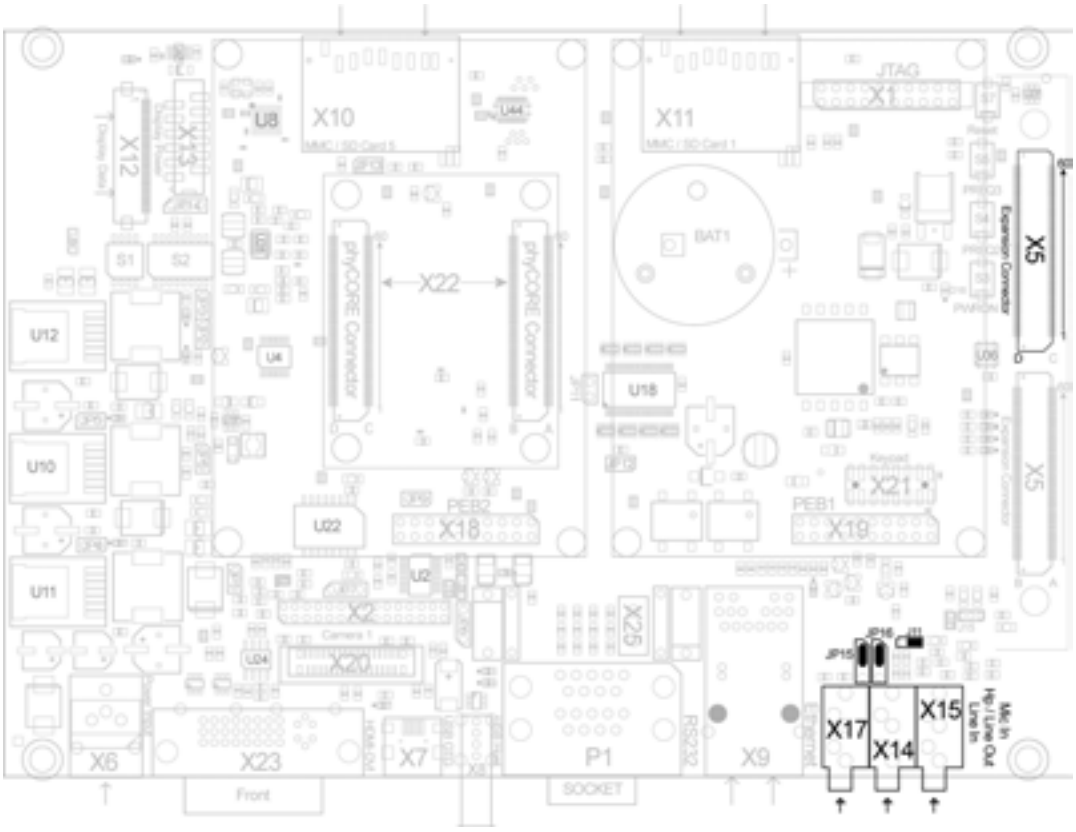


Figure 33: Components supporting the Audio Interface at connectors X5, X14, X15 and X17 (top view)

Figure 34: Components supporting the Audio Interface at connectors X5, X14, X15 and X17 (bottom view)

The audio interface provides a method of exploring the OMAP44xx's I^2S capabilities. The phyCORE-OMAP44xx Carrier Board is populated with a Texas Instruments low-power stereo audio codec with integrated mono class-d amplifier (TLV320AIC3007) at U43. The TLV320AIC3007 provides a High Performance Audio DAC and ADC with sample rates from 8 kHz to 96 kHz. It supports a stereo line input, stereo microphone input, stereo line output, stereo headphone output, and direct speaker output.

The TLV320AIC3007 is interfaced to the phyCORE-OMAP44xx SOM via the I^2S interface of the multichannel buffered serial port's third module (McBSP3) for audio data and the fourth I^2C interface (I2C4) for codec configuration (I^2C address 0x18). Audio devices can be connected to 3.5 mm audio jacks at X14, X15 and X17, and to expansion connector X5. A detailed list of applicable connectors is presented below.

Audio Outputs:

X14 - Headset Out or Line Output - Line_OUTL/Line_OUTR

X5 - Speaker Out (X5D22 - Speaker negative differential output; X5D23 - Speaker positive differential output)

Audio Inputs:

X15- Microphone Inputs - MIC1/MIC2

X17 - Line Input - Line_INL/Line_INR

Please refer to the audio codec's reference manual for additional information regarding the special interface specification.

Jumper J13 allows flexible control over the audio codec's master clock source (MCLK). In the default position (2 + 3) the codec is clocked from the module's X_FREF_CLK4_REQ clock signal. The audio codec's master clock can range from 512 kHz to 50 MHz. If J13 is set to 1 + 2 the clock is generated by a crystal oscillator (19,2 MHz) at OZ1 on the carrier board. See Table 41 for jumper configuration settings.

Connector X14 carries either signals from the headset out or the line output of the codec. Jumpers JP15 (right channel) and JP16 (left channel) allow to select the audio source for connector X14. The default configuration (1 + 2) connects the headset output to X14 (see Table 41 for details).

As well the microphone input (X15), as the headset output (X14) allow for jack detection. The jack detection of the microphone input is hardwired, while jack detection of the headset output can be disabled by jumper J11. In the default position (2 +3) jumper J11 connects the shield contact of audio jack X14 (headphone out) to either GND. In this configuration jack detection is disabled. Connecting the shield contact to the HPCOM output driver of the stereo audio codec at U43 (J11 at 1 + 2) allows to use the jack detection function.

2.1.3.11 I²C Connectivity

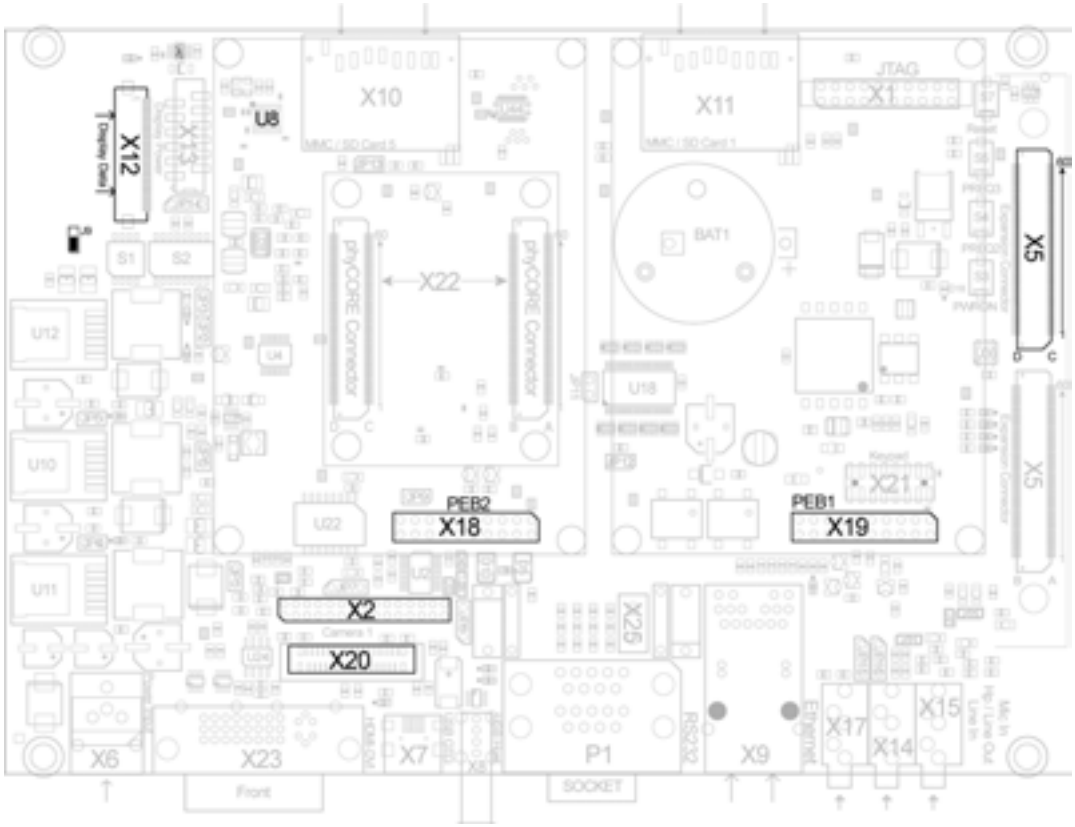


Figure 35: I²C Connectivity (top view)

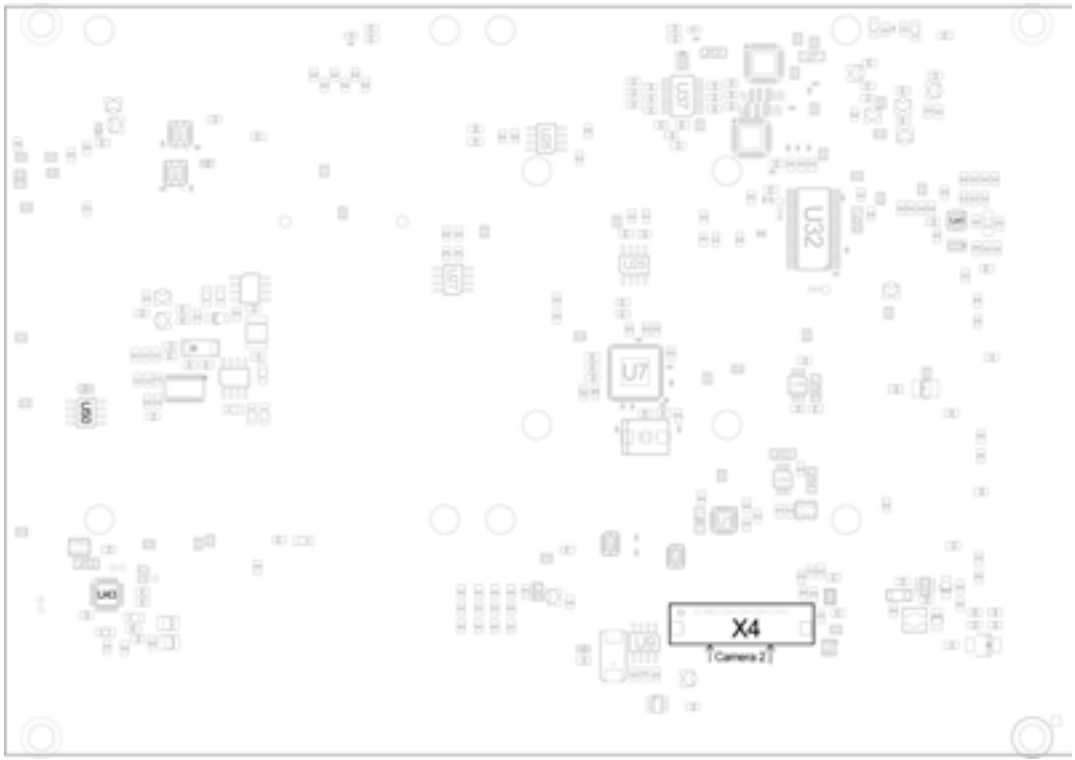


Figure 36: I²C Connectivity (bottom view)

The I²C interfaces of the phyCORE-OMAP44xx are available at different connectors on the phyCORE-OMAP44xx Carrier Board. The following table provides a list of the connectors and pins with I²C connectivity. The voltage level of some of the I²C interfaces are translated to a higher level by level shifters on the carrier board. The following table itemizes the I²C interfaces, the connector where they can be found, and the voltage level.

Connector	Location	SL
Connectors providing I²C interface I2C1		
Expansion connector X5	pin 2C (I2C1_SDA_3V3); pin 1C (I2C1_SCL_3V3)	3.3 V
Connectors providing I²C interface I2C3		
Camera_1 interface X20[1]	pin 29 (CAM-1_SDA); pin 28 (CAM-1_SCL)	VCC_CAM-1
Camera_1 interface X21	pin 9 (CAM-1_SDA); pin 10 (CAM-1_SCL)	VCC_CAM-1
Camera_2 interface X4	pin 29 (CAM-2_SDA); pin 28 (CAM-2_SCL)	VCC_CAM-2
PEB interface X18	pin 7 (I2C3_SDA_3V3); pin 8 (I2C3_SCL_3V3)	3.3 V
Expansion connector X5	pin 5C (I2C3_SDA_3V3); pin 4C (I2C3_SCL_3V3)	3.3 V
Expansion connector X5	pin 11C (CAM-1_SDA); pin 10C (CAM-1_SCL)	VCC_CAM-1
Expansion connector X5	pin 7D (CAM-2_SDA); pin 6D (CAM-2_SCL)	VCC_CAM-2
Connectors providing I²C interface I2C4		
Display data connector X12	pin 8 (I2C4_SDA_3V3); pin 7 (I2C4_SCL_3V3)	3.3 V
PEB interface X19	pin 7 (I2C4_SDA_3V3); pin 8 (I2C4_SCL_3V3)	3.3 V
Expansion connector X5	pin 8C (I2C4_SDA_3V3); pin 7C (I2C4_SCL_3V3)	3.3 V

Table 59: I²C Connectivity

1. To use the Camera_1 I²C interface JP6 must be closed to have VCC_CAM_1 available.

To avoid any conflicts when connecting external I²C devices to the phyCORE-OMAP44xx Carrier Board the addresses of the on-board I²C devices must be considered. Some of the addresses can be configured by jumper. Table 60 lists the addresses already in use. It shows only the default address.

I²C Interface	Device on the phyCORE-OMAP44xx		I²C Address (standard) (7 MSB)	Maximum Speed
I2C1	EEPROM (module)		0x50[1]	400 kHz
I2C1	PMIC (module)		0x48, 0x49, 0x4A	400 kHz
I²C Interface	**Device on the Carrier Board**		**I²C Address (standard) (7 MSB)**	**Maximum Speed**
I2C3	X18 - PEB2 Interface		Depends on the PHYTEC Extension Board (PEB) connected to this interface. Please refer to the corresponding hardware manual of the PEB	
I2C4	U8 - TC358764 (DSI2LVDS)		0x0F	400 kHz
I2C4	U42 - MAX1037 (ADC Display)		0x64	400 kHz
I2C4	U41 - STMPE811 (Touch)		0x41[2]	400 kHz
I2C4	U43 - TLV320AIC3007 (Audio)		0x18	400 kHz
I2C4	X19 - PEB1 Interface		Depends on the PHYTEC Extension Board (PEB) connected to this interface. Please refer to the corresponding hardware manual of the PEB	
I2C4	U50 - PCA9533 (LED Dimmer)		0x62	400 kHz
I²C Interface	**External Device connectable to the Carrier Board**		**I²C Address (standard) (7 MSB)**	**Maximum Speed**
I2C3	Camera Boards with phyCAM-P interface connected to X4	I²C interface of the image sensor (all camera boards)	Depends on the camera board (VM-00x) connected to this interface. Please refer to the corresponding phyCAM-P / phyCAM-S manual (L-748)	
		I²C interface of the bus expander (only cameras which allow for dynamic switching between 8/10 bit interface)	0x41	Equal to the speed of the sensor's I²C interface
I2C4	LCD-014 connected to the PHYTEC Display - Interface (X12, X13)		0x50, 0x51	400 kHz
I2C4	LCD-017 connected to the PHYTEC Display - Interface (X12, X13)		0x50, 0x51	400 kHz

Table 60: I²C Addresses in Use

1. Can be configured by changing the appropriate jumper(s). Please refer to Section 1.3 for alternative address settings.
2. Can be configured by changing the appropriate jumper(s). Please refer to Section 2.1.2.4 for alternative address settings.

Note:

Please note that the I²C interface of some of the applicable camera modules have a maximum speed of 100 kHz. Accordingly the I2C3 interface is slowed down and doesn't operate at it's maximum speed of 400 kHz. This must be considered when attaching additional devices to I2C3 (e.g. if an I²C device is attached to the PHYTEC Extension Board connector X18 (PEB2)).

The HDMI interface has a dedicated I²C interface. For more informations about this see Section 2.1.3.8.

2.1.3.12 SPI Connectivity

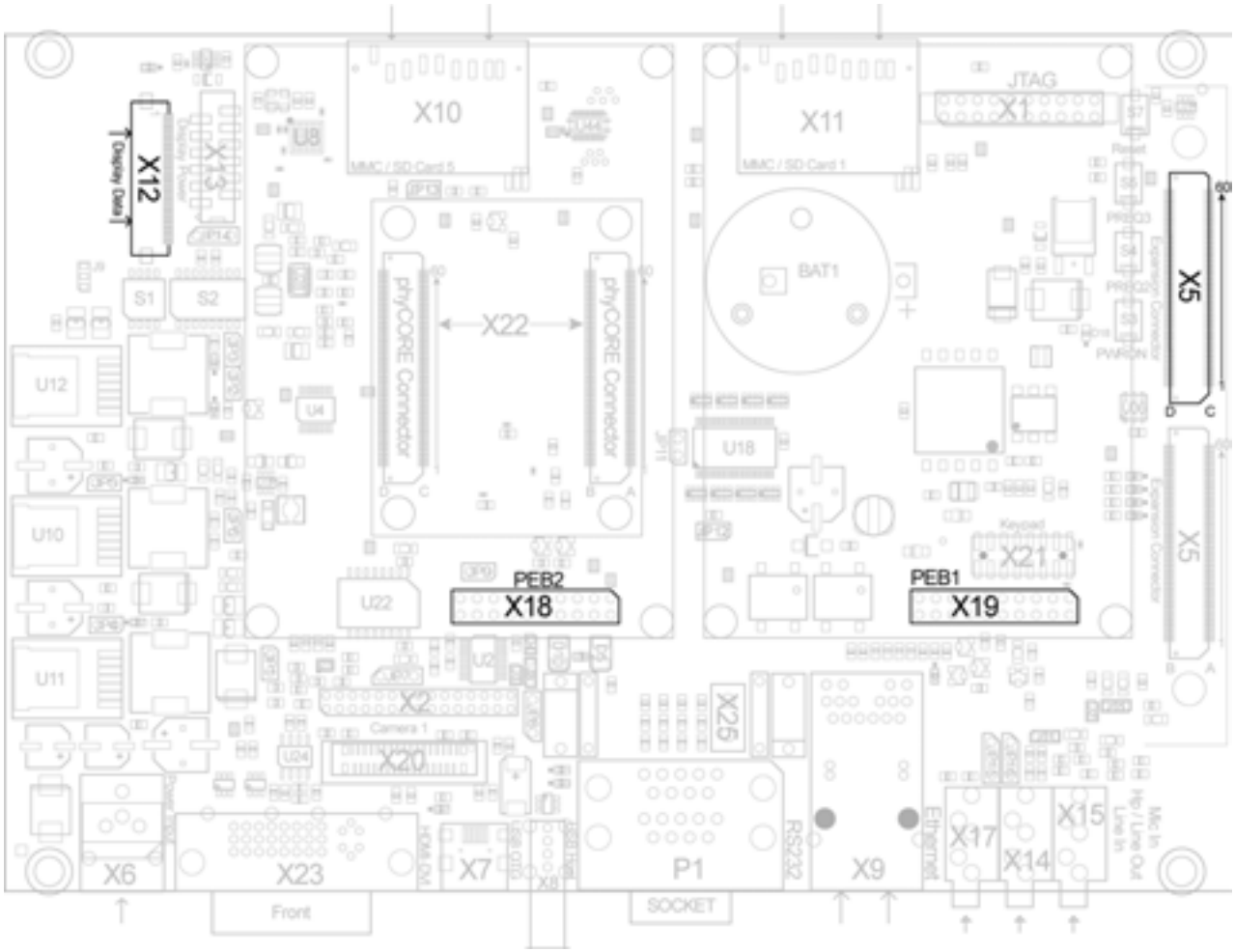


Figure 37: SPI Connectivity

The phyCORE-OMAP44xx Carrier Board supports two SPI interfaces. The first one originates from the phyCORE-OMAP44xx's SPI1 interface which is Master/Slave configurable and supports up to four peripherals (refer to Section 1.8.7 for details). This interface is available at the PHYTEC Extension Board (PEB) connectors X18 and X19, as well as at the display data connector X12 and the expansion connector X5. Table 61 shows the assignment of the SPI chip select signals to the different connectors.

The second SPI interface is derived from the Multichannel Audio Serial (McASP) interface pins of the phyCORE-OMAP44xx as these pins embody the signals of the second SPI module SPI2 as alternative function. This interface provides only one chip select signal (CS0). The second SPI interfaces is available at Expansion Connector X5 (please refer to Section 2.1.3.21.6 for details on the correlation between McASP and SPI2 signals).

The signals of both SPI interfaces are translated from 1.8 V to 3.3 V.

SPI1 Chip Select Signal	Connector / Interface	SL
SPI1_CS0_3V3	PEB1 Interface (X19)	3.3 V
SPI1_CS1_3V3	PEB2 Interface (X18)	3.3 V
SPI1_CS2_3V3	Display Interface (X12)	3.3 V
SPI1_CS3_3V3	Expansion Connector (X5)	3.3 V

Table 61: Assignment of the SPI1 Chip Select Signals

2.1.3.13 User programmable GPIOs

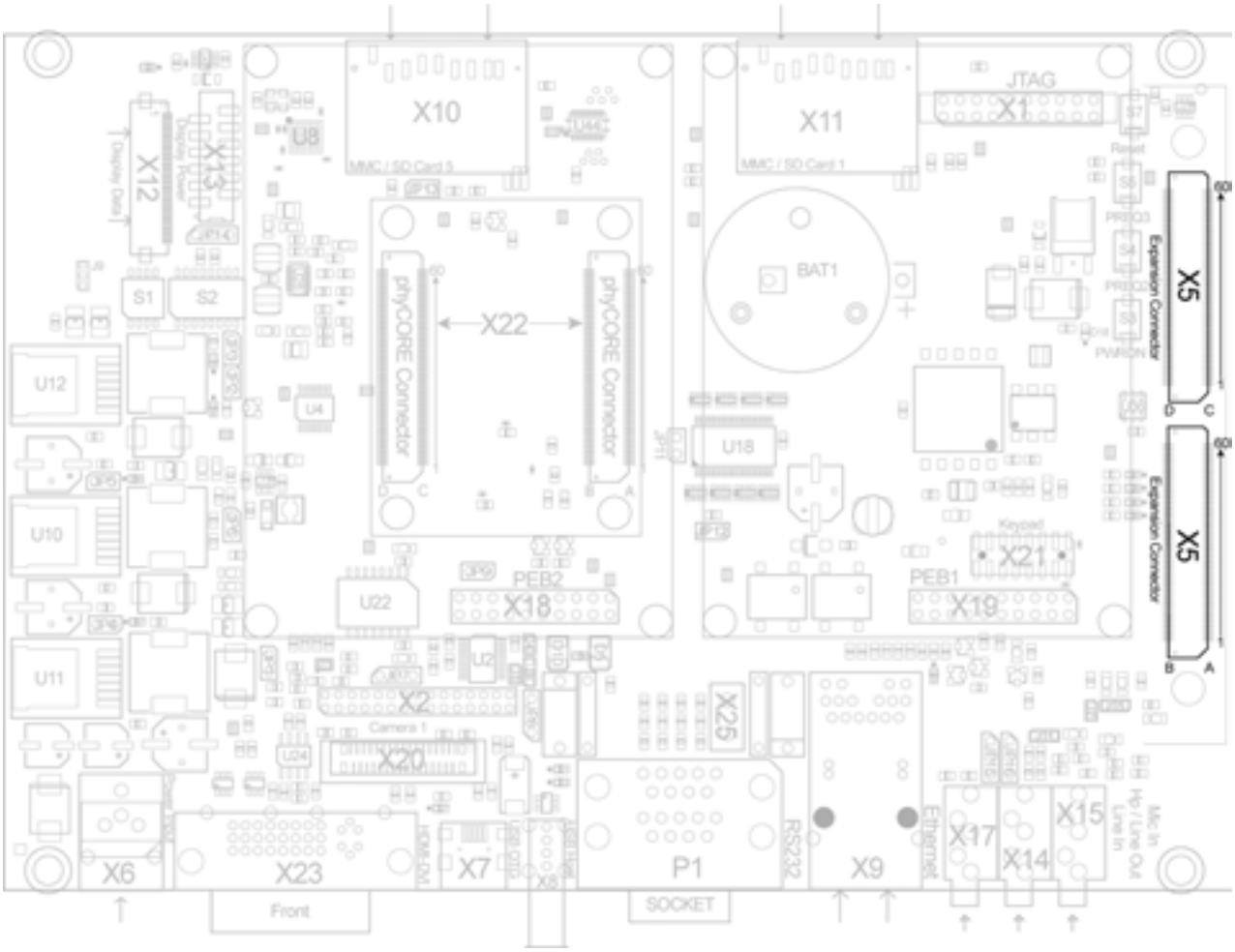


Figure 38: GPIOs at Expansion Connector X5

In general most of the pins of the phyCORE-OMAP44xx which are connected directly to the OMAP44xx can be configured to act as GPIOs, due to the function multiplexin at most controller pins. Thereby, it must be considered that most of the signals are used on the phyCORE-OMAP44xx Carrier Board already. This also applies to the three dedicated GPIOs of the phyCORE-OMAP44xx. Special functions have been assigned to these GPIOs in order to demonstrate their use (see also Table 42). Signals not used extend from the phyCORE-Connector (X22) directly to the expansion connector X5. The following table lists all signals available as GPIOs.

In order to use the GPIOs the software must be changed.

Signal	Pin #	I/O	SL	Description
X_CSI21_DX0	X5C18	I	CSI	GPI 67, or CSI2-A (CSI21) differential clock positive input
X_CSI21_DY0	X5C19	I	CSI	GPI 68, or CSI2-A (CSI21) differential clock negative input
X_CSI21_DX1	X5C20	I	CSI	GPI 69, or CSI2-A (CSI21) differential data lane positive input 1
X_CSI21_DY1	X5C21	I	CSI	GPI 70, or CSI2-A (CSI21)differential data lane negative input 1
X_CSI21_DX2	X5C22	I	CSI	GPI 71, or CSI2-A (CSI21) differential data lane positive input 2
X_CSI21_DY2	X5C23	I	1.8 V/CSI	GPI 72, or CSI2-A (CSI21) differential data lane negative input 2
X_UART1_TX	X5C35	I/O	1.8 V	GPIO 129, or UART1 transmit
X_UART1_RX	X5C36	I/O	1.8 V	GPIO 128, or UART1 receive
X_SDMMC1_DAT4	X5D1	I/O	VCC_MMC1	GPIO 106, or SD/MMC1 Data 4
X_SDMMC1_DAT5	X5D2	I/O	VCC_MMC1	GPIO 107, or SD/MMC1 Data 5
X_SDMMC1_DAT6	X5D3	I/O	VCC_MMC1	GPIO 108, or SD/MMC1 Data 6
X_SDMMC1_DAT7	X5D4	I/O	VCC_MMC1	GPIO 109, or SD/MMC1 Data 7
X_USBC1_ICUSB_DP	X5D12	I/O	USB	GPIO 98, or USBC1 data plus
X_USBC1_ICUSB_DM	X5D13	I/O	USB	GPIO 99, or USBC1 data minus
X_USBB1_OC_GPIO_120	X5D35	I	1.8 V	GPIO 120, or USB Host overcurrent signal input

Table 62: Signals freely available as GPIO

To avoid mismatch of different voltage levels the signal level (SL) shown in the table must be taken into account when connecting external devices to these pins.

2.1.3.14 User programmable LEDs

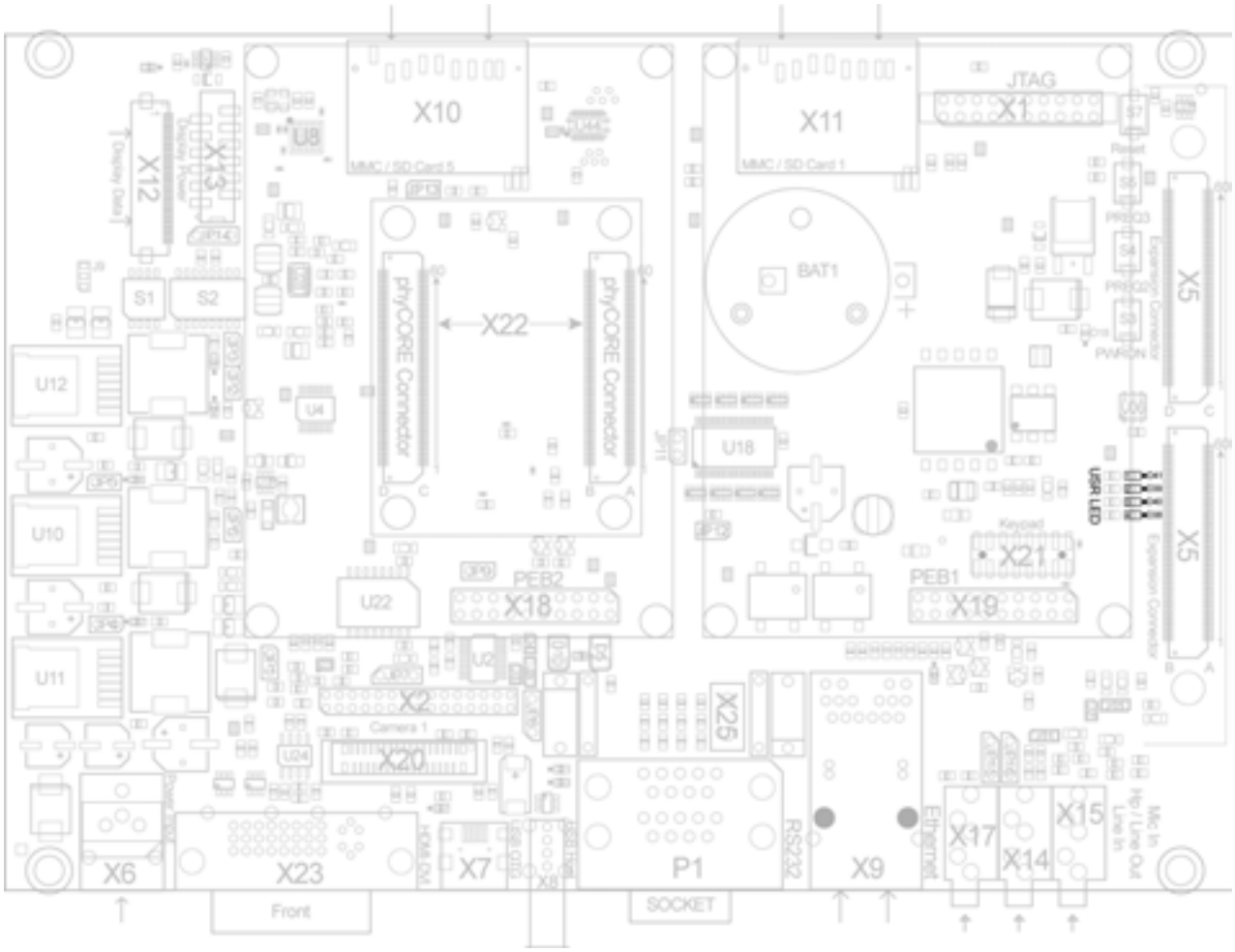


Figure 39: User programmable LEDs

Four user programmable LEDs are available on the phyCORE-OMAP44xx Carrier Board. These LEDs are controlled by the I^2C LED dimmer at U50 (PCA9533), which is connected to the phyCORE's I^2C4 bus. The I^2C address is 0x62. The user LEDs are free programmable for example a Heartbeat Connect detection of SD/MMC card or other things. The LEDs are in different colors on the carrier board. In cases of need it can assembled with other color LEDs.

LED title	LED color	description
D41	red	User LED 1 (LED driver 0 of the PCA9533)
D39	yellow	User LED 2 (LED driver 1 of the PCA9533)
D40	yellow	User LED 3 (LED driver 2 of the PCA9533)
D38	green	User LED 4 (LED driver 3 of the PCA9533)

Table 63: User Programmable LEDs

2.1.3.15 Extension Connectors (X18, X19)

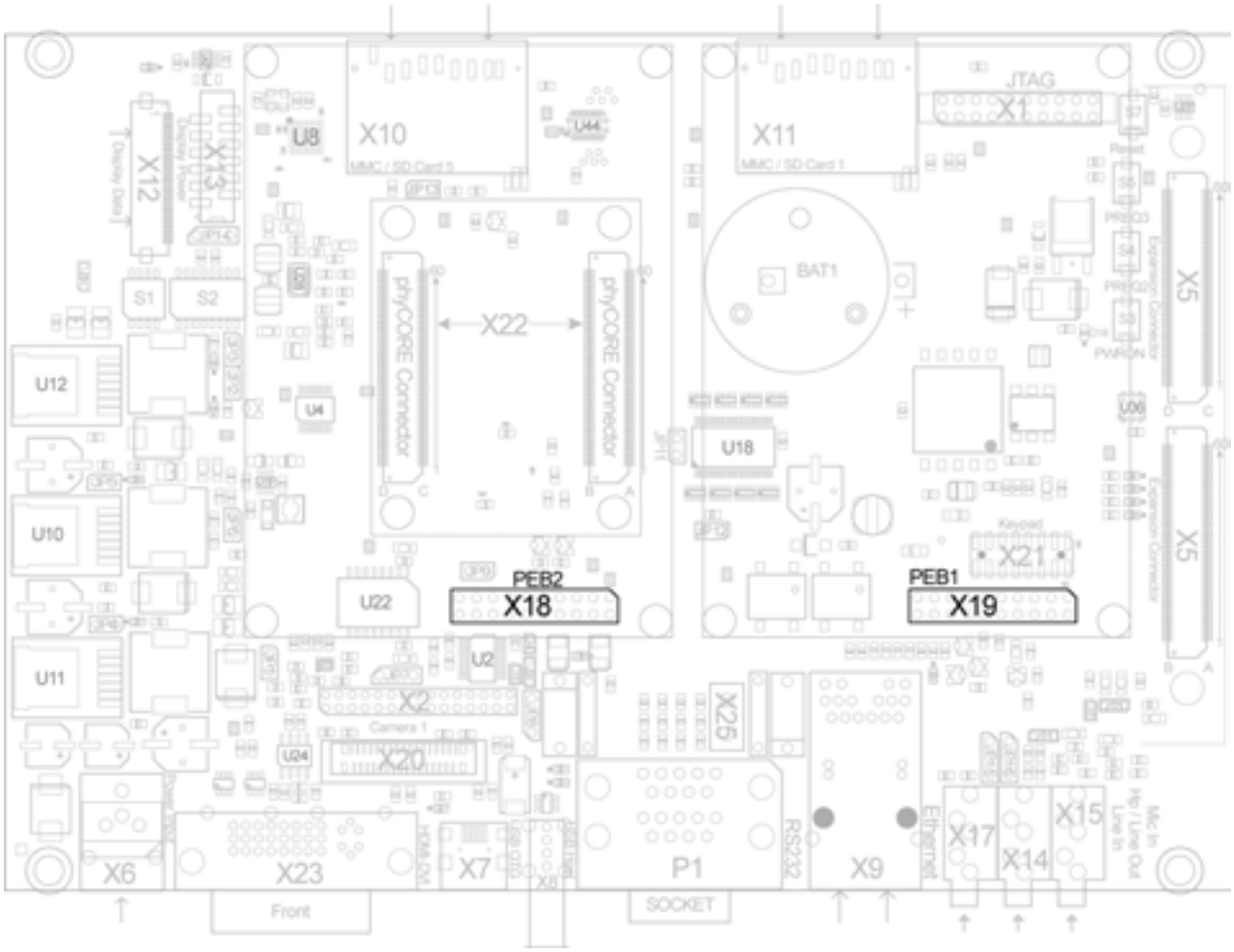


Figure 40: Extension Connectors X18, X19

Extension connectors X18 and X19 provide an easy way to add other functions and features to the phyCORE-OMAP44xx Carrier Board. Standard interfaces such as USB, SPI and I^2C as well as different supply voltages and one GPIO are available at the pin header Rows.

As can be seen in Figure 40 the location of the connectors allows to extend the functionality without expanding the physical dimensions. Mounting wholes can be used to screw the additional PCBs to the phyCORE-OMAP44xx Carrier Board. When referencing pin numbers note that pin 1 is located at the angled corner. Pins towards the labeling "X18", or "X19"are odd numbered.

The extension connectors share the SPI interface of the phyCORE-OMAP44xx with the display data connector X12, but they used different CS- signals.

Signal	Extension Connector	Description
SPI1_CS0_3V3	X19	Chip Select 0 of the SPI 1 interface
SPI1_CS1_3V3	X18	Chip Select 1 of the SPI 1 interface
X_UART4_RX_GPIO_155	X19	The SLOT0_IRQ of PEB
X_UART4_TX_GPIO_155	X18	The SLOT1_IRQ of PEB

Table 64: Signal Assignment to Extension Connector

Pin #	Signal	I/O	SL	Description
1	VCC5V	O	5 V	5V power supply
2	VCC5V	O	5 V	5V power supply
3	VCC3V3	O	3.3 V	3.3V power supply
4	VCC3V3	O	3.3 V	3.3V power supply
5	GND	-	-	Ground
6	GND	-	-	Ground
7	I2C4_SDA_3V3 I2C3_SDA_3V3	I/O	3.3 V	X19 I2C4 Data extension port 0 X18 I2C3 Data extension port 1
8	I2C4_SCL_3V3 I2C3_SCL_3V3	I/O	3.3 V	X19 I2C4 Clock extension port 0 X18 I2C3 Clock extension port 1
9	PHYWIRE	I/O	3.3 V	Hardware Introspection Interf. **For internal use only**
10	GND	-	-	Ground
11	SPI1_CS0_3V3 SPI1_CS1_3V3	O	3.3 V	X19 SPI chip select extension port 0 X18 SPI chip select extension port 1
12	SPI1_MOSI_V3	O	3.3 V	SPI master output/slave input
13	SPI1_CLK_3V3	O	3.3 V	SPI clock output
14	SPI1_MISO_3V3	I	3.3 V	SPI master input/slave output
15	/SPI1_RDY_3V3	I/O	3.3 V	SPI data ready input master mode only
16	SLOT0_IRQ SLOT1_IRQ	I	3.3 V	X19 Interrupt input extension port 0 X18 Interrupt input extension port 1
17	GND	-	-	Ground
18	GND	-	-	Ground
19	USB1DN_DM2 USB1DN_DM3	I/O	USB	X19 USB1 Data DM2 X18 USB1 Data DM3
20	USB1DN_DP2 USB1DN_DP3	I/O	USB	X19 USB1 Data DP2 X18 USB1 Data DP3

Table 65: PHYTEC Extension Connectors X18, X19

2.1.3.16 Secure Digital Memory / MultiMedia Card Slots (X10, X11)

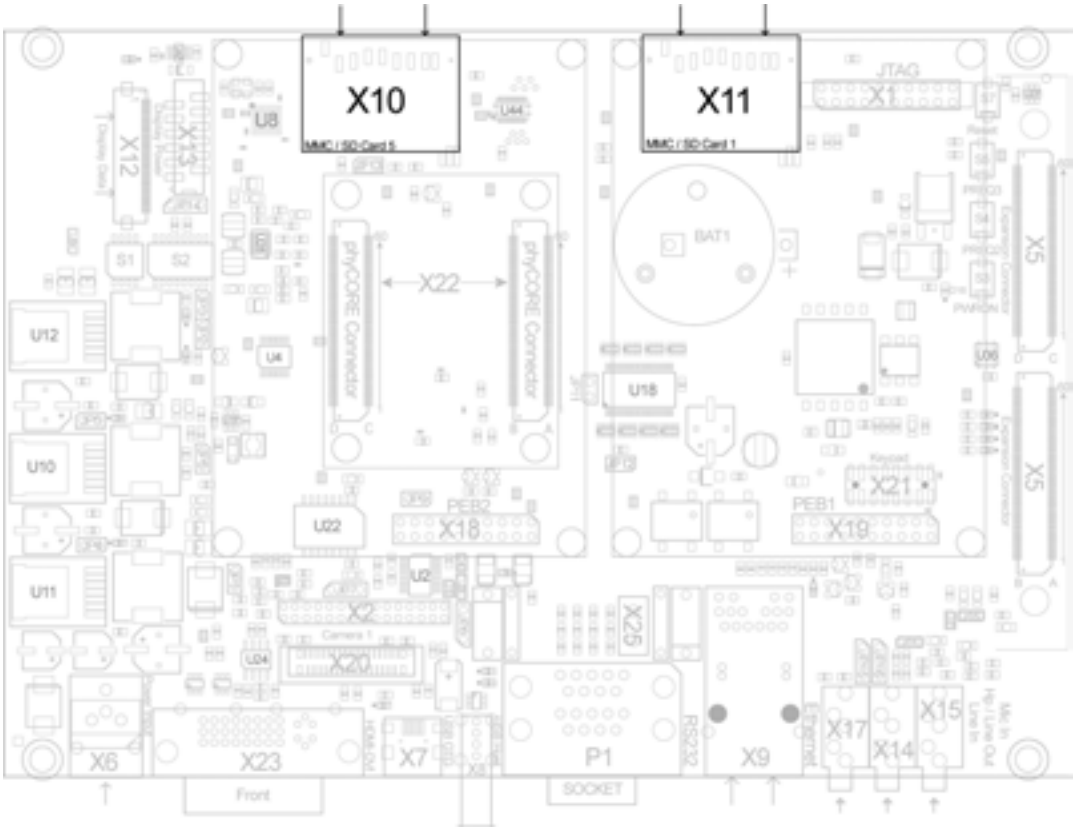


Figure 41: Components supporting the SD / MM Card interfaces at connector X10 and X11 (top view)

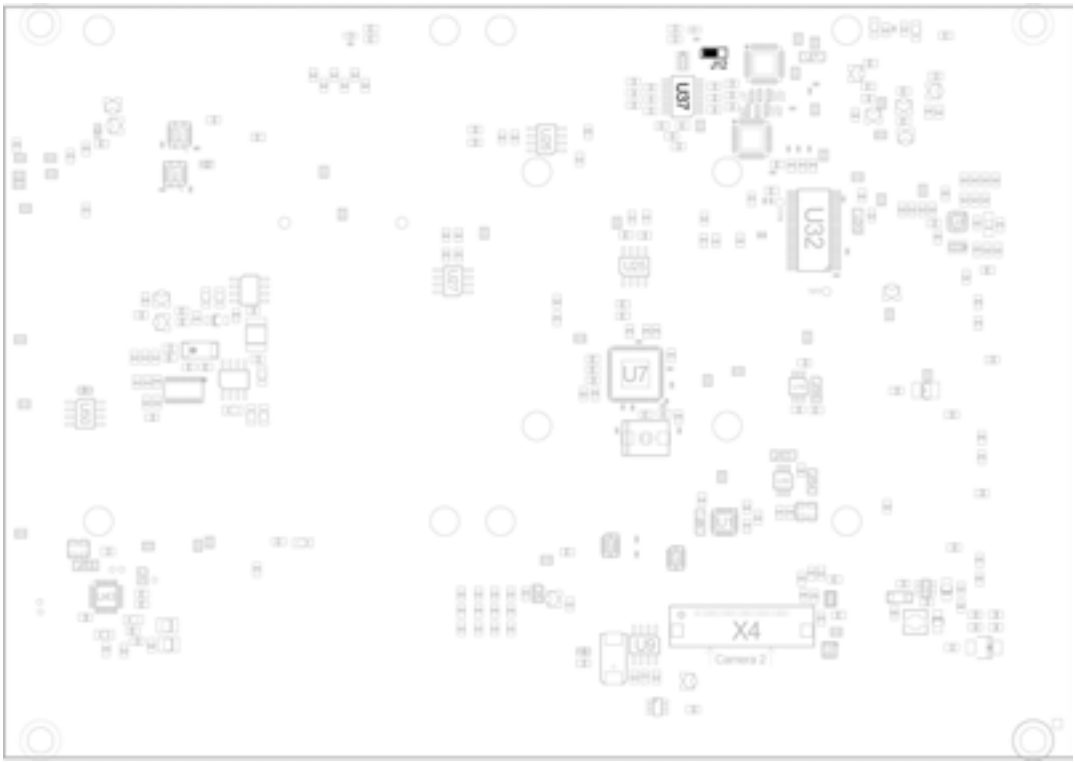


Figure 42: Components supporting the SD / MM Card interfaces at connector X10 and X11 (bottom view)

The phyCORE Carrier Board provides two standard SDHC card slots at X10 and X11 for connection to SD/MMC interface cards. It allows easy and convenient connection to peripheral devices like SD- and MMC cards. Power to the SD interface is supplied by sticking the appropriate card into the SD/MMC slot.

SD/MMC card slot 2 (X10) connects to the OMAP44xx's SD / MMC Card interface SDMMC5. The signals are shifted from VCC_1V8_IO (1.8 V) at the phyCORE Connector to VCC_SDMMC5 by level shifter U37. Jumper J12 allows to change the voltage level of the supply voltage (VCC_SDMMC5). The default level is 3.3 V (VCC_3V3) (J12 at position 1+2). Closing jumper J12 at 2+3 results in a supply voltage of 1.8 V (VCC_1V8). Removing the level shifter and mounting RN1, R157 and R155 connects the SD / MMC Card interface SDMMC5 of the phyCORE-OMAP44xx directly to SD/MMC card slot 2 (X10).

SD/MMC card slot 1 (X11) connects to the OMAP44xx's SD / MMC Card interface SDMMC1. The card slot is connected directly to the phyCORE-OMAP44xx. Howvere, the power supply for SD/MMC card slot 1(X11) is variable adjustable by the PMIC of the phyCORE-OMAP44xx. For more information please see Section 1.7 .

Note:

The SDMMC5 Bus on connector X10 doesn't have the full supported MMC bus speed of the phyCORE-OMAP44xx. The reason is the level-shifter U37, which limits the speed on 60 Mbps by 3V3 MMC- \ SD cards and 40 Mbps by 1V8 MMC- \ SD cards.

2.1.3.17 Boot Mode Selection (S1, S2)

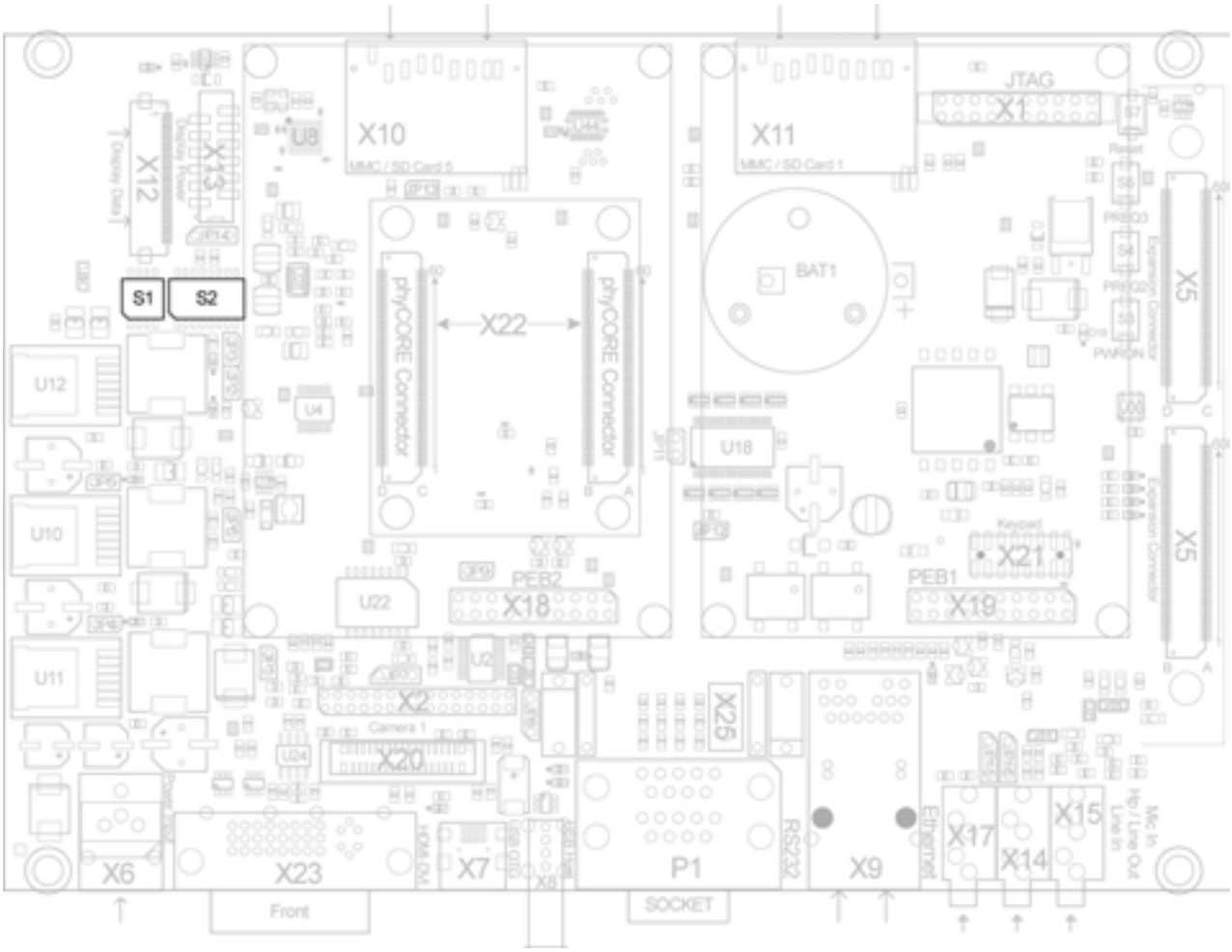


Figure 43: Boot Mode Selection Switches S1 and S2

The boot mode switches S1 and S2 are provided to allow changing the booting device order of the OMAP44xx after a reset. They are connected to the X_BOOT[x] pins of the phyCORE-OMAP44xx. There are always two switches connected to one X-BOOT input. One switch pulls X_BOOT[x] to LOW, and the second one to HIGH. With both switches turned OFF the default value predefined by the resistor network on the phyCORE-OMAP44xx is valid at the corresponding sys_boot configuration pin of the OMAP44xx. The following table shows the possible settings of the first two switches S1_1 and S1_2 as an example, while table Table 67 outlines the relation between the switches and the X_BOOT pin of the phyCORE-OMAP44xx and the corresponding sys_boot configuration pin of the OMAP44xx.

	X_BOOT[0] = LOW (sys_boot [0] = LOW)	X_BOOT[0] = HIGH (sys_boot [0] = HIGH)	value according to the configuration circuitry (pull-up or pull-down resistors) on the phyCORE-OMAP44xx
S1_1 (connecting to GND)	On	Off	**Off**
S1_2 (connecting to VCC_1V8)	Off	On	**Off**

Table 66: Possible Configurations of the DIP-Switches[1]

1. Default settings are in **bold blue** text

	phyCORE Configuration Pin	OMAP44xx Configuration Pin
S1_1 / S1_2	X_BOOT0 (X1C57)	sys_boot[0]
S1_3 / S1_4	X_BOOT1 (X1D57)	sys_boot[1]
S2_1 / S2_2	X_BOOT2 (X1C58)	sys_boot[2]
S2_3 / S2_4	X_BOOT3 (X1D58)	sys_boot[3]
S2_5 / S2_6	X_BOOT4 (X1C59)	sys_boot[4]
S2_7 / S2_8	X_BOOT5 (X1D60)	sys_boot[5]

Table 67: Connections between DIP-Switches S1 / S2 and the Configuration Pins on the phyCORE-OMAP44xx

By default the boot mode DIP-switches S1 and S2 are off, configuring the phyCORE-OMAP44xx for booting from 1st: NAND, 2nd: USB, 3rd: UART, 4th: MMC1.

Please refer to chapter Section 1.5 for more information about the possible configurations.

2.1.3.18 System Reset Button (S7)

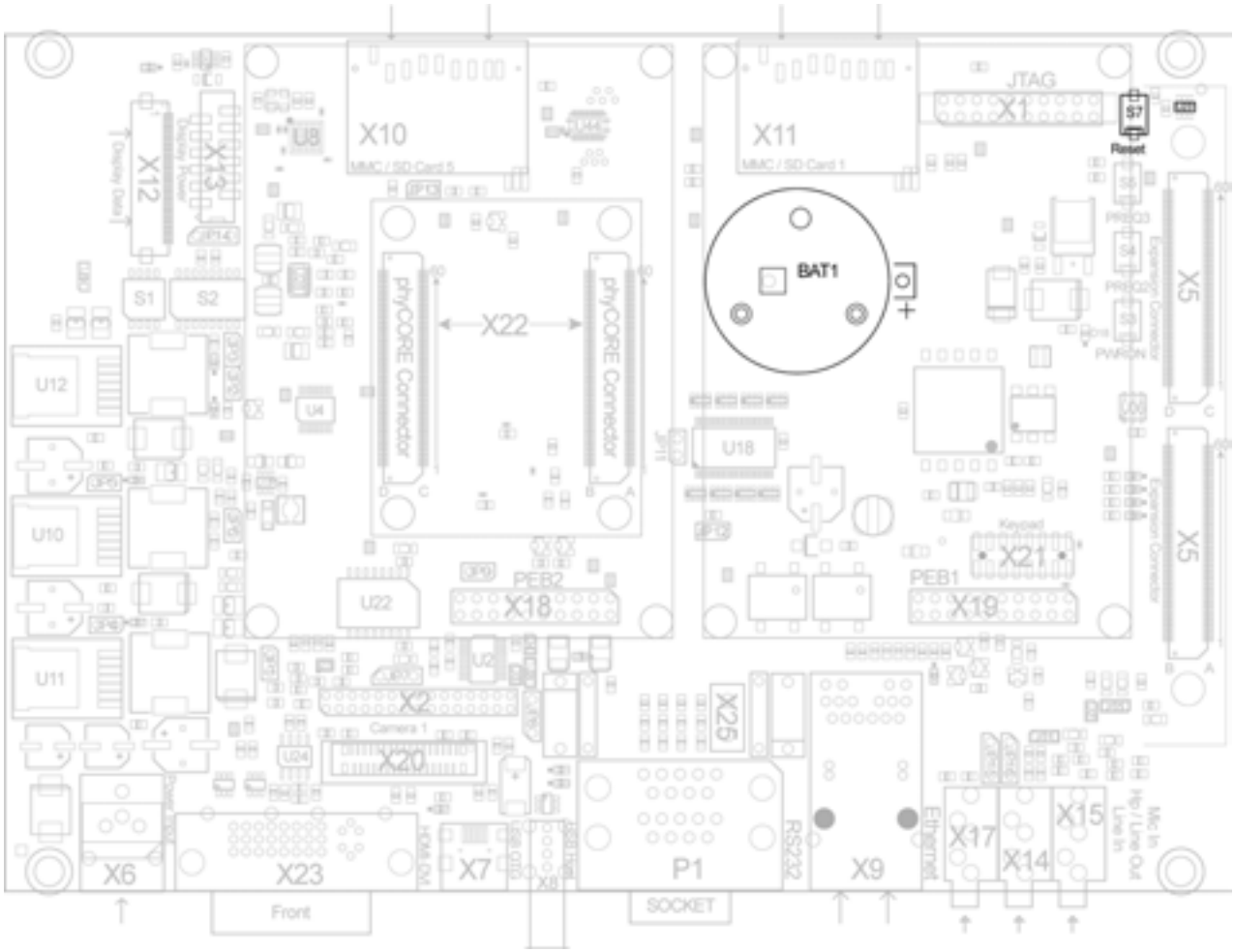


Figure 44: System Reset Button S7

The phyCORE Carrier Board is equipped with a system reset button at S7, a reset device (U23) and a LI-cell (BAT1). Pressing the button will not only reset the phyCORE mounted on the phyCORE-OMAP44xx Carrier Board, but also the peripheral devices, such as the USB Hub, etc.

S7 Issues a **system reset** signal. Pressing this button will toggle the X_nRESET_PWRON signal LOW, causing a reset of the phyCORE-OMAP44xx and the peripheral devices on the carrier board.

"If the Lithium-Ion Battery (BAT1) is assembled and VCC_3V3 falls below 2.9 V, then the reset device (U23) connects the Lithium-Ion Battery to the backup battery input (VBAT) of the phyCORE-OMAP44xx. This way the RTC and some critical registers of the PMIC on the SOM are supplied by the Lithium-Ion Battery in case of a power loss."

"If the Lithium-Ion Battery (BAT1) is not assembled and VCC_3V3 falls below 2.9 V, then the reset device (U23) triggers a system reset by pulling X_nRESET_PWRON low."

2.1.3.19 phyCORE JTAG Connectivity (X1)

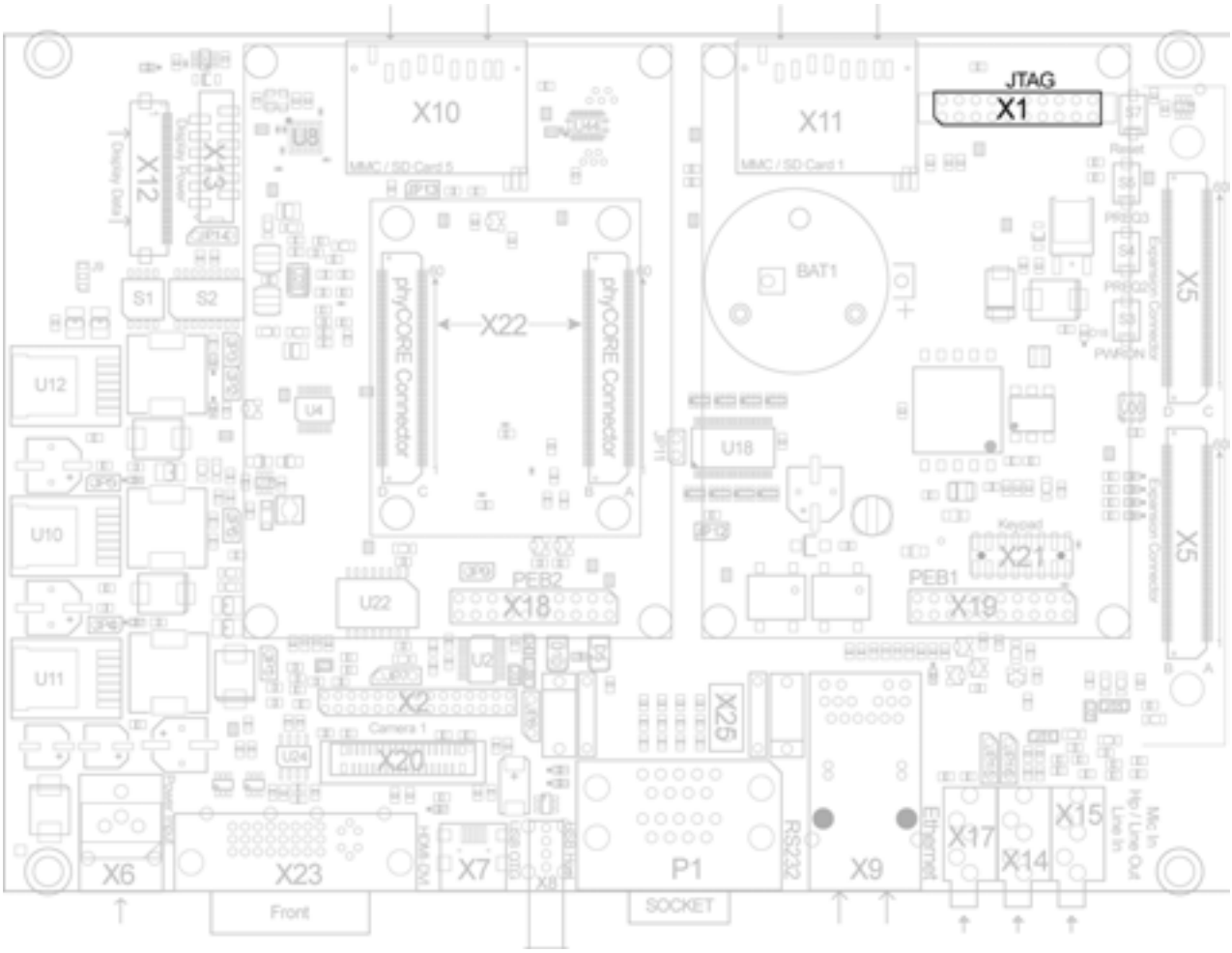


Figure 45: phyCORE JTAG Connectivity X1

The JTAG interface of the phyCORE-OMAP44xx is accessible at connector X1 on the carrier board. This interface is compliant with JTAG specification IEEE 1149.1 or IEEE 1149.7. No jumper settings are necessary for using the JTAG port. The following table describes the signal configuration at X1. When referencing contact numbers note that pin 1 is located at the angled corner. Pins towards the labeling "JTAG" are even numbered.

Pin #	Signal	I/O	SL	Description
1	VCC_1V8_IO	O	1.8 V	JTAG Chain reference voltage
2	VCC_1V8_IO	O	1.8 V	JTAG Chain supply voltage
3	X_JTAG_nTRST	I	1.8 V	JTAG Chain Test Reset
4, 6, 8, 10, 12, 14, 18, 20	GND	-	-	Ground
5	X_JTAG_TDI	I	1.8 V	JTAG Chain Test Data input
7	X_JTAG_TMS	I/O	1.8 V	JTAG Chain Test Mode Select signal
9	X_JTAG_TCK	I	1.8 V	JTAG Chain Test Clock signal
11	X_JTAG_RTCK	O	1.8 V	JTAG Chain Return Test Clock signal
13	X_JTAG_TDO	O	1.8 V	JTAG Chain Test Data Output
15	X_nRESET_WARM	I	1.8 V	System Reset
17	X_DPM_EMU0	I/O	1.8 V	Debug Request
19	X_DPM_EMU1	I/O	1.8 V	Debug Acknowledge

Table 68: JTAG Connector X1 Pin Descriptions

2.1.3.20 Keypad Connector (X21)

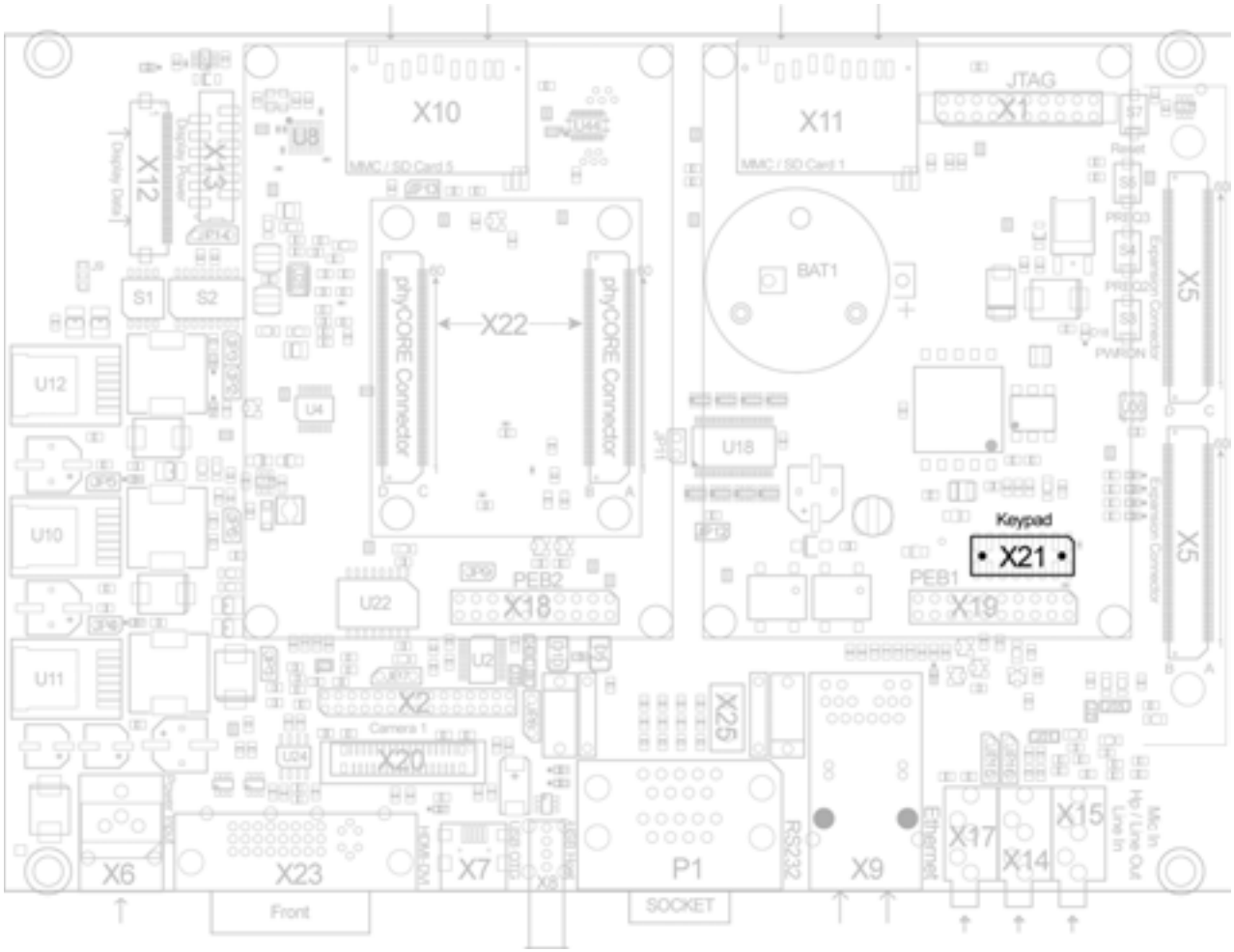


Figure 46: Keypad Connector X21

The 2.00 mm socket connector X21 provides access to the OMAP44xx keyboard controller signals (kpd). Figure 46 shows a detailed view of the location of the keypad connector. When referencing contact numbers note that contact 1 is located at the angled corner. Contacts towards the pin header connector X19 are even numbered while contacts towards the labeling "Keypad" are odd numbered.

The keypad connector supports multiconfiguration keypads with up to 6 rows x 6 columns (up to 36 keys). The reference voltage VCC_1V8_IO and the supply voltage VCC_3V3 are also available at the keypad connector. The following table describes the signal mapping at X21

Location	Signal	I/O	SL	Description
1	VCC_1V8_IO	O	VCC_1V8_IO	1.8 V IO reference voltage
2	VCC_3V3	O	VCC_3V3	3.3 V supply voltage
3	X_KPD_COL0	O	VCC_1V8_IO	Keyboard column 0 (open drain)
4	X_KPD_ROW0	I	1.8 V	Keyboard row 0
5	X_KPD_COL1	O	VCC_1V8_IO	Keyboard column 1 (open drain)

Table 69: Keypad Connector (X21) Signal Mapping

Location	Signal	I/O	SL	Description
6	X_KPD_ROW1	I	1.8 V	Keyboard row 1
7	X_KPD_COL2	O	VCC_1V8_IO	Keyboard column 2 (open drain)
8	X_KPD_ROW2	I	1.8 V	Keyboard row 2
9	X_KPD_COL3	O	VCC_1V8_IO	Keyboard column 3 (open drain)
10	X_KPD_ROW3	I	1.8 V	Keyboard row 3
11	X_KPD_COL4_CSI21_DX3	O/I	VCC_1V8_IO / CSI	Keyboard column 4 (open drain) / CSI2-A (CSI21) differential data lane positive input 3 (see note below)
12	X_KPD_ROW4_CSI21_DY3	I	1.8 V / CSI	Keyboard row 4 / CSI2-A (CSI21) differential data lane negative input 3 (see note below)
13	X_KPD_COL5_CSI21_DX4	O/I	VCC_1V8_IO / CSI	Keyboard column 5 (open drain) / CSI2-A (CSI21) differential data lane positive input 4 (see note below)
14	X_KPD_ROW5_CSI21_DY4	I	1.8 V / CSI	Keyboard row 5 / CSI2-A (CSI21) differential data lane negative input 4 (see note below)
15, 16	GND	-	-	Ground

Table 69: Keypad Connector (X21) Signal Mapping

Note:

Contacts 10 to 13 of the keypad connector provide either signals of the keyboard interface, or camera lanes 3 and 4 of the primary camera interface. The resistor array JN1 on the phyCORE-OMAP44xx allows to choose which signals are brought out at these pins. The default setting of JN1 at position 1 allows to use the keyboard interface without changes. Please refer to Table 6 for more information on JN1.

Caution:

When using the keypad connector (X21) with a smaller keypad (for example, 4 × 4), unused rows must be tied high (e.g. by connecting the corresponding pins to contact 1 (VCC_1V8_IO) of connector X21) to prevent disturbing the scanning process. Normally, all rows must be pulled up internally at the I/O cells of the device.

2.1.3.21 Expansion Connector (X5)

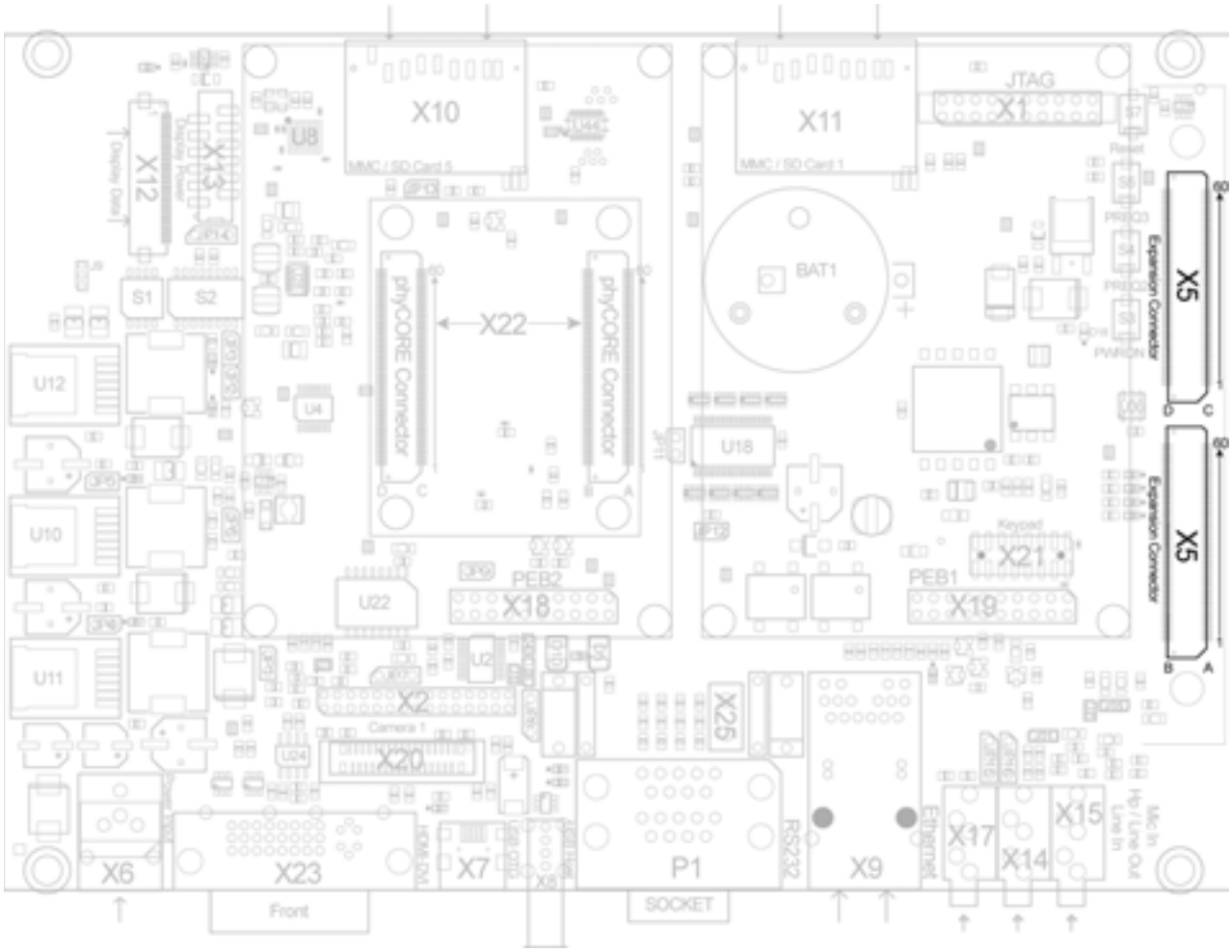


Figure 47: Expansion Connector X5

Unused signals or functions of the phyCORE-OMAP44xx or the carrier board are partial on the expansion connector X5.

2.1.3.21.1 DISPC Signal Mapping

The signals of the OMAP44xx's parallel display interface (DISPC) are available at extension connector X5 to allow connecting a customer specific display adapter to the phyCORE-OMAP44xx (refer also to Section 1.11.1).

Signal	Pin #	I/O	SL	Description
X_DISPC_DATA0	X5A1	O	1.8 V	parallel display data 0
X_DISPC_DATA1	X5A2	O	1.8 V	parallel display data 1
X_DISPC_DATA2	X5A3	O	1.8 V	parallel display data 2
X_DISPC_DATA3	X5A4	O	1.8 V	parallel display data 3
X_DISPC_DATA4	X5A5	O	1.8 V	parallel display data 4
X_DISPC_DATA5	X5A6	O	1.8 V	parallel display data 5
X_DISPC_DATA6	X5A7	O	1.8 V	parallel display data 6
X_DISPC_DATA7	X5A8	O	1.8 V	parallel display data 7
X_DISPC_DATA16	X5A10	O	1.8 V	parallel display data 16
X_DISPC_DATA17	X5A11	O	1.8 V	parallel display data 17
X_DISPC_DATA18	X5A12	O	1.8 V	parallel display data 18
X_DISPC_DATA19	X5A13	O	1.8 V	parallel display data 19
X_DISPC_DATA20	X5A14	O	1.8 V	parallel display data 20
X_DISPC_DATA21	X5A15	O	1.8 V	parallel display data 21
X_DISPC_DATA22	X5A16	O	1.8 V	parallel display data 22
X_DISPC_DATA23	X5A17	O	1.8 V	parallel display data 23
X_DISPC_DATA8	X5B1	O	1.8 V	parallel display data 8
X_DISPC_DATA9	X5B2	O	1.8 V	parallel display data 9
X_DISPC_DATA10	X5B3	O	1.8 V	parallel display data 10
X_DISPC_DATA11	X5B4	O	1.8 V	parallel display data 11
X_DISPC_DATA12	X5B5	O	1.8 V	parallel display data 12
X_DISPC_DATA13	X5B6	O	1.8 V	parallel display data 13
X_DISPC_DATA14	X5B7	O	1.8 V	parallel display data 14
X_DISPC_DATA15	X5B8	O	1.8 V	parallel display data 15
X_DISPC_DE	X5B10	O	1.8 V	parallel display enable
X_DISPC_HSYNC	X5B11	O	1.8 V	parallel display HSYNC
X_DISPC_VSYNC	X5B12	O	1.8 V	parallel display VSYNC
X_DISPC_PCLK	X5B13	O	1.8 V	parallel display pixel clock

Table 70: Parallel Display Interface (DISPC) Signal Mapping

2.1.3.21.2 USBB2 Signal Mapping

If the parallel display interface of the OMAP44xx is not needed to drive a display some of the pins can be combined to design an additional USB interface using port 2 of the OMAP44xx's high speed USB host subsystem. The HS USB host subsystem supports the 12-pin/8-bit data SDR version of the ULPI mode and allows connection to either an USB transceiver (in ULPI mode), or an USB controller (in ULPI TLL interface mode) (refer to the OMAP44xx Reference Manual). The following table shows the location of the ULPI interface signals with reference to the signal names at the phyCORE-Connector.

Signal	Pin #	I/O	SL	Description
X_DISPC_DATA18	X5A12	I/O	1.8 V	USBB2 Interface Data 2 (usbb2_ulpi_dat2)
X_DISPC_DATA19	X5A13	I/O	1.8 V	USBB2 Interface Data 1 (usbb2_ulpi_dat1)
X_DISPC_DATA20	X5A14	I/O	1.8 V	USBB2 Interface Data 0 (usbb2_ulpi_dat0)
X_DISPC_DATA21	X5A15	I	1.8 V	USBB2 Interface Next (usbb2_ulpi_nxt)
X_DISPC_DATA22	X5A16	I	1.8 V	USBB2 Interface Direction (usbb2_ulpi_dir)
X_DISPC_DATA23	X5A17	O	1.8 V	USBB2 Interface Stop (usbb2_ulpi_stp)
X_DISPC_DATA11	X5B4	I/O	1.8 V	USBB2 Interface Data 7 (usbb2_ulpi_dat7)
X_DISPC_DATA12	X5B5	I/O	1.8 V	USBB2 Interface Data 6 (usbb2_ulpi_dat6)
X_DISPC_DATA13	X5B6	I/O	1.8 V	USBB2 Interface Data 5 (usbb2_ulpi_dat5)
X_DISPC_DATA14	X5B7	I/O	1.8 V	USBB2 Interface Data 4 (usbb2_ulpi_dat5)
X_DISPC_DATA15	X5B8	I/O	1.8 V	USBB2 Interface Data 3 (usbb2_ulpi_dat3)
X_DMTIMER9_PWM_EVT	X5B15	I	1.8 V	USBB2 Interface Clock[1] (usbb2_ulpi_clk)

Table 71: USBB2 Signal Mapping

1. Jumper J6 on the phyCORE-OMAP44xx must be configured at 2+3 to have this signal available (see Table 5)

Note:

Jumper JP14 should be closed at position 2+3 in order to shut down the FlatLink™ transmitter which also connects to these signals. This allows to avoid signal conflicts and to reduce disturbances.

2.1.3.21.3 I2C Signal Mapping

"The expansion connector provides all I2C interfaces of the phyCORE-OMAP44xx as well as the I2C interfaces intended for camera connectivity. All signals have been translated from 1.8 V to 3.3 V or VCC_CAM-1/2 by voltage-level translators on the carrier board. Please pay special attention to the Signal Level (SL) column in the following table when connecting other devices to these I2C interfaces."

Signal	Pin #	I/O	SL	Description
I2C1_SCL_3V3	X5C1	I/O	3.3 V	I2C1 clock signal
I2C1_SDA_3V3	X5C2	I/O	3.3 V	I2C1 data signal
I2C3_SCL_3V3	X5C4	I/O	3.3 V	I2C3 clock signal
I2C3_SDA_3V3	X5C5	I/O	3.3 V	I2C3 data signal
I2C4_SCL_3V3	X5C7	I/O	3.3 V	I2C4 clock signal
I2C4_SDA_3V3	X5C8	I/O	3.3 V	I2C4 data signal
CAM-1_SCL	X5C10	I/O	VCC_CAM-1	Camera 1 I^2C clock signal[1]
CAM-1_SDA	X5C11	I/O	VCC_CAM-1	Camera 1 I^2C data signal1
CAM-2_SCL	X5D6	I/O	VCC_CAM-2	Camera 2 I^2C clock signal[2]
CAM-2_SDA	X5D7	I/O	VCC_CAM-2	Camera 2 I^2C data signal2

Table 72: I^2C Signal Mapping

1. To use the Camera_1 I^2C interface JP6 must be closed to have VCC_CAM-1 available.
2. To use the Camera_2 I^2C interface JP1 must be closed to have VCC_CAM-2 available.

2.1.3.21.4 Primary Camera Interface CSI2-A/CSI21 Signal Mapping

The expansion connector X5 provides the CSI2-A/CSI21 camera interface of the phyCORE-OMAP44xx.

Signal	Pin #	I/O	SL	Description
CAM-1_CTRL1	X5C13	-	-	Camera 1 control signal 1
CAM-1_CTRL2	X5C14	-	-	Camera 1 control signal 2
X_CAM_STROBE	X5C15	O	1.8 V	Camera flash activation trigger
X_CAM_SHUTTER	X5C16	O	1.8 V	Mechanical shutter control signal
X_CAM_GLOBAL_RESET	X5C17	I/O	1.8 V	Camera sensor reset
X_CSI21_DX0	X5C18	I	CSI	CSI2-A (CSI21) differential clock positive input
X_CSI21_DY0	X5C19	I	CSI	CSI2-A (CSI21) differential clock negative input
X_CSI21_DX1	X5C20	I	CSI	CSI2-A (CSI21) differential data lane positive input 1
X_CSI21_DY1	X5C21	I	CSI	CSI2-A (CSI21) differential data lane negative input 1
X_CSI21_DX2	X5C22	I	CSI	CSI2-A (CSI21) differential data lane positive input 2

Table 73: CSI21 Camera Signal Mapping

Signal	Pin #	I/O	SL	Description
X_CSI21_DY2	X5C23	I	1.8 V/CSI	CSI2-A (CSI21) differential data lane negative input 2
X_KPD_COL4_CSI21_DX3	X5C24	O/I	1.8 V/CSI	Keyboard column 4 (open drain) / CSI2-A (CSI21) differential data lane positive input 3
X_KPD_ROW4_CSI21_DY3	X5C25	I	1.8 V/CSI	Keyboard row 4 / CSI2-A (CSI21) differential data lane negative input 3
X_KPD_COL5_CSI21_DX4	X5C26	O/I	1.8 V/CSI	Keyboard column 5 (open drain) / CSI2-A (CSI21) differential data lane positive input 4
X_KPD_ROW5_CSI21_DY4	X5C27	I	1.8 V/CSI	Keyboard row 5 / CSI2-A (CSI21) differential data lane negative input 4

Table 73: CSI21 Camera Signal Mapping

Note:

The function of camera control signals CAM-1_CTRL1 and CAM-1_CTRL2 depends on the camera board used. Connector X2 allows to connect them either to GND, or VCC-CAM-1, or any other signal needed. Please refer to the hardware manual delivered with your camera board for precise information on theses signals and their function.

Note:

The resistor array JN1 on the phyCORE-OMAP44xx allows to choose which signals are brought out at these pins. In order to use camera lanes 3 and 4 of the primary camera interface at expansion connector X5 JN1 must be set to position 2. Please refer to Figure 6 to see where JN1 is located.

2.1.3.21.5 SPI1 Signal Mapping

Expansion connector X5 provides connectivity to the SPI1 interface of the phyCORE-OMAP44xx. As can be seen in the following table chip select three (CS3) addresses SPI devices attached to the expansion connector. All signals have been translated from 1.8 V to 3.3 V by voltage-level translators on the carrier board.

Signal	Pin #	I/O	SL	Description
SPI1_CLK_3V3	X5C29	O	3.3 V	SPI1 clock
SPI1_MISO_3V3	X5C30	I/O	3.3 V	SPI1 MISO
SPI1_MOSI_3V3	X5C31	I/O	3.3 V	SPI1 MOSI
SPI1_CS3_3V3	X5C32	O	3.3 V	SPI1 Chip Select 3
/SPI1_RDY_3V3	X5C33	I/O	3.3 V	SPI1 Ready

Table 74: SPI1 Signal Mapping

2.1.3.21.6 SPI2 Signal Mapping

The second SPI interface is derived from the Multichannel Audio Serial (McASP) interface pins of the phyCORE-OMAP44xx as these pins embody the signals of the second SPI module SPI2 as alternative function. However, if the pins of the expansion connector listed in the following table are intended to be used as Multichannel Audio Serial interface, it must be noted that all signals required for the second SPI interface are translated from 1.8 V to 3.3V. Only signal X_McASP_AMUTEIN_GPIO_117 (mute in from external) is at the original voltage level of 1.8 V.

Compared with the first SPI interface on the carrier board the second SPI interface provides only one chip select signal (CS0).

Signal	Extension Bus	I/O	SL	Description
X_McASP_AMUTEIN_GPIO_117	X5D15	I	1.8 V	Mute in from external at 1.8 V
McSPI2_CLK_3V3	X5D16	I/O	3.3 V	SPI2 Interface Clock / McASP transmit high frequency master clock (McASP_AHCLKX)
McSPI2_SOMI_3V3	X5D17	I/O	3.3 V	SPI2 Interface SOMI / McASP audio transmit data (McASP_AXR)
McSPI2_SIMO_3V3	X5D18	I/O	3.3 V	SPI2 Interface SIMO / McASP mute out to external (McASP_AMUTE)
McSPI2_CS0_3V3	X5D19	I/O	3.3 V	SPI2 Interface Chip Select 0 / McASP transmit frame synchronization (McASP_AFSX)
/SPI2_RDY_3V3	X5D20	I/O	3.3 V	SPI2 Interface Ready / McASP transmit bit clock (McASP_ACLKX)

Table 75: SPI2 (McASP) Signal Mapping

2.1.3.21.7 UART1 Signal Mapping

The expansion connector X5 provides the UART1 Interface of the phyCORE-OMAP44xx.

Signal	Extension Bus	I/O	SL	Description
X_UART1_TX	X5C35	O	1.8 V	UART1 transmit
X_UART1_RX	X5C36	I	1.8 V	UART1 receive

Table 76: UART1 Signal Mapping

2.1.3.21.8 PMIC Signal Mapping

The expansion connector X5 provides the PMIC control and status signals of the phyCORE-OMAP44xx

Signal	Pin #	I/O	SL	Description
X_PMIC_SYSEN	X5C38	O	1.8 V	Sysen output for switching an extern power source
X_PMIC_EXTCHRG_ENZ	X5C39	O	1.8 V	Control output to extern Loading-IC
X_PMIC_VAC	X5C40	I	-	extern VAC charger input
X_PMIC_CHRG_EXTCHRG_STATZ	X5C41	I	1.8 V	Status input from extern Loading-IC
X_PMIC_CLK32KAUDIO	X5D37	O	1.8 V	32K Clock

Table 77: PMIC Signal Mapping

2.1.3.21.9 USBC1 Signal Mapping

The expansion connector X5 provides the USBC1 signals of the phyCORE-OMAP44xx.

Signal	Pin #	I/O	SL	Description
X_USBC1_ICUSB_DP	X5D12	I/O	USB	USBC1 data plus
X_USBC1_ICUSB_DM	X5D13	I/O	USB	USBC1 data minus

Table 78: USBC1 Signal Mapping

2.1.3.21.10 Audio Speaker Mapping

The expansion connector X5 provides the Audio Speaker signals of the Audio device driver TLV320AIC3007 (U43). X24 - Speaker Out - maximal 1 Watt into a differential 8 Ohm load

Signal	Pin #	I/O	SL	Description
SPEAKER_SPOM	X5D22	O	AUDIO	Speaker negative differential output
SPEAKER_SPOP	X5D23	O	AUDIO	Speaker positive differential output

Table 79: Audio Speaker Mapping

2.1.3.21.11 Control Signal Mapping

The expansion connector X5 provides the control signals of the phyCORE-OMAP44xx.

Signal	Pin #	I/O	SL	Description
X_nRESET_WARM	X5D39	I	1.8 V	WARM Reset Signal
X_nRESET_PWRON	X5D40	I/O	1.8 V	Power On Reset Signal
X_nRESET_PER	X5D41	I/O	1.8 V	PER Reset Signal

Table 80: System Signal Mapping

2.1.3.21.12 Power Signal Mapping

The expansion connector X5 provides the power signals of the carrier board and the phyCORE-OMAP44xx.

Signal	Pin #	I/O	SL	Description
GND	X5C42, X5C43, X5C44, X5C45, X5D42, X5D43, X5D44, X5D45	-	-	Ground
V_BAT	X5C46	O	3.3 V	Backup voltage
VCC_3V3_S	X5C47, X5C48	O	3.3 V	3.3 V reference voltage
VCC_1V8	X5C49 - X5C51, X5D49 - X5D51	O	1.8 V	1.8 V voltage domain
VCC_3V3	X5C52 - X5C54, X5D52 - X5D54	O	3.3 V	3.3 V reference domain
VCC_5V	X5C55 - X5C57, X5D55 - X5D57	O	5 V	5V voltage domain
VCC_12_24	X5C58 - X5C60, X5D58 - X5D60	O	12 V - 24 V	+12 V to +24 V voltage domain
VCC_1V8_IO	X5D47, X5D48	O	1.8 V	1.8 V reference domain
VCC_1V2	X5D33	O	1.2 V	1.2 V reference domain

Table 81: Power Signal Mapping

2.1.3.21.13 Signals freely available as GPIO

Signal	Pin #	I/O	SL	Description
X_CSI21_DX0	X5C18	I	CSI	GPI 67, or CSI2-A (CSI21) differential clock positive input
X_CSI21_DY0	X5C19	I	CSI	GPI 68, or CSI2-A (CSI21) differential clock negative input
X_CSI21_DX1	X5C20	I	CSI	GPI 69, or CSI2-A (CSI21) differential data lane positive input 1
X_CSI21_DY1	X5C21	I	CSI	GPI 70, or CSI2-A (CSI21) differential data lane negative input 1
X_CSI21_DX2	X5C22	I	CSI	GPI 71, or CSI2-A (CSI21) differential data lane positive input 2
X_CSI21_DY2	X5C23	I	1.8 V/CSI	GPI 72, or CSI2-A (CSI21) differential data lane negative input 2
X_UART1_TX	X5C35	I/O	1.8 V	GPIO 129, or UART1 transmit
X_UART1_RX	X5C36	I/O	1.8 V	GPIO 128, or UART1 receive
X_SDMMC1_DAT4	X5D1	I/O	VCC_MMC1	GPIO 106, or SD/MMC1 Data 4
X_SDMMC1_DAT5	X5D2	I/O	VCC_MMC1	GPIO 107, or SD/MMC1 Data 5

Table 82: Signals freely available as GPIO

Signal	Pin #	I/O	SL	Description
X_SDMMC1_DAT6	X5D3	I/O	VCC_MMC1	GPIO 108, or SD/MMC1 Data 6
X_SDMMC1_DAT7	X5D4	I/O	VCC_MMC1	GPIO 109, or SD/MMC1 Data 7
X_USBC1_ICUSB_DP	X5D12	I/O	USB	GPIO 98, or USBC1 data plus
X_USBC1_ICUSB_DM	X5D13	I/O	USB	GPIO 99, or USBC1 data minus
X_USBB1_OC_GPIO_120	X5D35	I	1.8 V	GPIO 120, or USB Host overcurrent signal input

Table 82: Signals freely available as GPIO

Note:

The function of camera control signals CAM-1_CTRL1 and CAM-1_CTRL2 depends on the camera board used. Connector X2 allows to connect them either to GND, or VCC-CAM-1, or any other signal needed. Please refer to the hardware manual delivered with your camera board for precise information on theses signals and their function.

2.1.3.22 Carrier Board Physical Dimensions

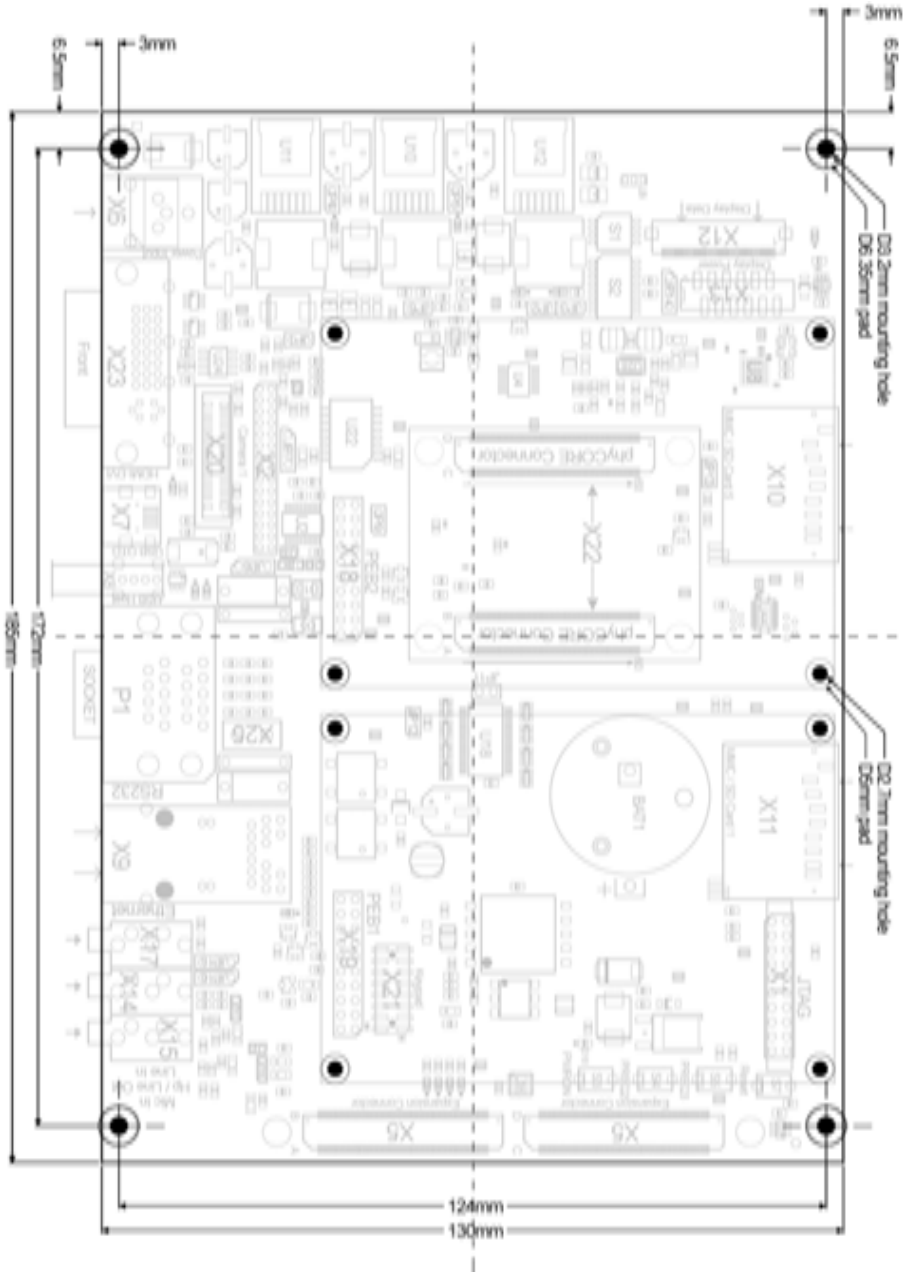


Figure 48: Carrier board physical dimensions

Please contact us if a more detailed dimensioned drawing is needed to integrate the phyCORE-OMAP44xx Carrier Board into a customer application.

3 Revision History

Date	Version numbers	Changes in this manual
01-07-2011	Manual L-760e_0	First draft, Preliminary documentation. Describes the phyCORE-OMAP44xx with phyCORE-OMAP44xx Carrier Board.
20-03-2012	Manual L-760e_1	Final documentation. Describes the phyCORE-OMAP44xx with phyCORE-OMAP44xx Carrier Board PCB-Numbers 1347.1 (SOM) and 1348.2 (CB).