HARDWARE ERRATA REPORT

P/N **PCM-052**
phyCORE-Vybrid System on Module
Revision A1, 5 February 2015

Errata ID	Errata Title	Affected PCB No.
01	Cold Boot Reliability	1374.0
02	NAND boot failure	1374.0
03	EEPROM I2C Address	1374.0, 1374.1

E01: Cold Boot Reliability

Affected PCB: 1374.0 with silicon version 1.1

Errata Impact: The system will hang occasionally after DDR initialization on a cold boot.

Errata Description: During a cold boot, the DDR controller will use an invalid starting address, which causes the system to hang.

Workaround: Press the RESET button (button S2; label RST on the carrier board PCB) to issue a warm reset, and the system will then boot successfully.

Errata Fix: Linux PD13.1.0 BSP

E02: NAND Boot Failure

Affected PCB: 1374.0

Errata Impact: The Vybrid ROM loader cannot boot a u-boot image from the NAND device.

Errata Description: The NAND controller's NFC_R/$\overline{B}$ by default should be high, putting the NAND flash into a ready state. Instead, NFC_R/$\overline{B}$ signal floats at power on. The system reads this as busy, and therefore, not ready for commands.

Workaround: Solder re-work must be done on the phyCORE-Vybrid Carrier Board (PCM-952). Add a 4.7kΩ resistor between NFC_R/$\overline{B}$ and VDD_3V3. Figure 1 below, shows a 0402 package 4.7kΩ (1/16 W, 1-5%) resistor soldered to the top pad of R114 (not populated) for a connection to VDD_3V3, which is then connected by a wire to the NFC_R/$\overline{B}$ signal available at the respective via.

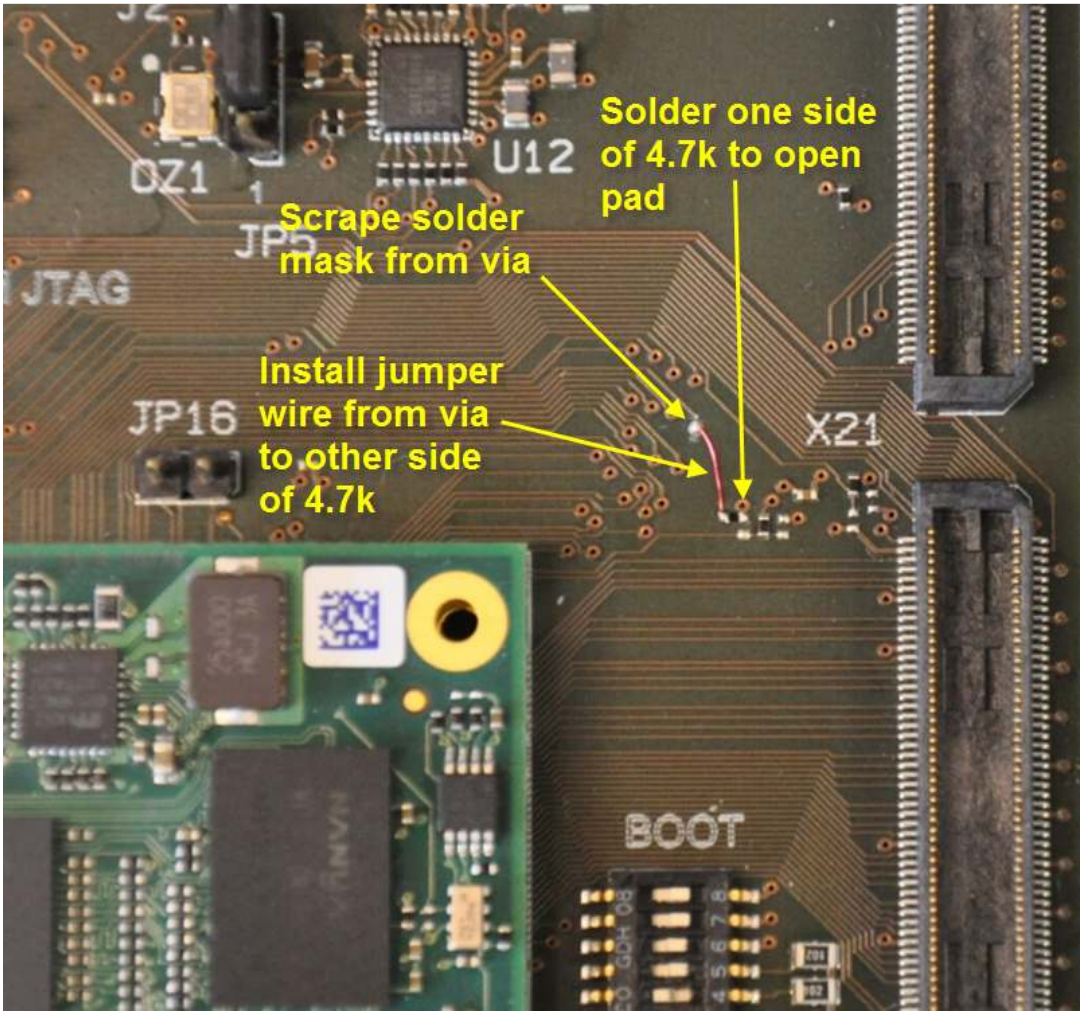

Figure 1: Errata 02 Rework

Errata Fix: 1374.1

E03: EEPROM I2C Address

Affected PCB: All 1374.0 and 1374.1 PCBs

Errata Impact: Only two 24FC256-I/MS devices can be on the same I2C bus without address overlap.

Errata Description: The schematic shows jumpers J1 and J2 configuring the EEPROM I2C address bits A1 and A2. Address bit A0 is permanently set to 0. However, the 24FC256-I/MS in an MSOP package populating the board does not have pins A1 or A0 internally connected. These address bits are permanently set to 0 inside the device. Thus only jumper J2 has an effect on setting the EEPROM I2C address. This leaves only two possible address combinations for this device, effectively limiting the I2C2 bus on Vybrid to only connecting two 24FC256-I/MS devices.

Workaround: If more than two EEPROM devices are required on the I2C2 bus then a different package other than MSOP should be chosen when using the 24xx256 devices on your Carrier Board. The 24xx256 devices also come in a SOIC or DFN package which have all three address bits accessible.

Errata Fix: None at this time.