phyCORE-i.MX35

HARDWARE MANUAL

EDITION JUNE 2010

A product of a PHYTEC Technology Holding company

In this manual are descriptions for copyrighted products that are not explicitly indicated as such. The absence of the trademark (™) and copyright (©) symbols does not imply that a product is not protected. Additionally, registered patents and trademarks are similarly not expressly indicated in this manual.

The information in this document has been carefully checked and is believed to be entirely reliable. However, PHYTEC Messtechnik GmbH assumes no responsibility for any inaccuracies. PHYTEC Messtechnik GmbH neither gives any guarantee nor accepts any liability whatsoever for consequential damages resulting from the use of this manual or its associated product. PHYTEC Messtechnik GmbH reserves the right to alter the information contained herein without prior notification and accepts no responsibility for any damages which might result.

Additionally, PHYTEC Messtechnik GmbH offers no guarantee nor accepts any liability for damages arising from the improper usage or improper installation of the hardware or software. PHYTEC Messtechnik GmbH further reserves the right to alter the layout and/or design of the hardware without prior notification and accepts no liability for doing so.

	EUROPE	NORTH AMERICA
Address:	PHYTEC Technologie Holding AG Robert-Koch-Str. 39 D-55129 Mainz GERMANY	PHYTEC America LLC 203 Parfitt Way SW, Suite G100 Bainbridge Island, WA 98110 USA
Ordering Information:	+49 (800) 0749832 order@phytec.de	1 (800) 278-9913 sales@phytec.com
Technical Support:	+49 (6131) 9221-31 support@phytec.de	1 (800) 278-9913 support@phytec.com
Fax:	+49 (6131) 9221-33	1 (206) 780-9135
Web Site:	http://www.phytec.de	http://www.phytec.com

1rst Edition June 2010

Index of Figures

Index of Tables

1 Preface

This hardware manual describes the phyCORE-i.MX35 Single Board Computer's design and function. Precise specifications for the Freescale i.MX35 microcontrollers can be found in the enclosed microcontroller Data Sheet/User's Manual.

In this hardware manual and in the attached schematics, active low signals are denoted by a "/" or "#" preceding the signal name (e.g.: /RD or #RD). A "0" indicates a logic zero or low-level signal, while a "1" represents a logic one or high-level signal.

Declaration of Electro Magnetic Conformity of the PHYTEC phyCORE-I.MX35

PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution:
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The phyCORE-i.MX35 is one of a series of PHYTEC Single Board Computers that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports a variety of 8-/16- and 32-bit controllers in two ways:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform

(2) as insert-ready, fully functional phyCORE OEM modules, which can be embedded directly into the user's peripheral hardware design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market. For more information go to:

http://www.phytec.com/services/phytec-advantage.html

1.1 Introduction

The phyCORE-i.MX35 belongs to PHYTEC's phyCORE Single Board Computer module family. The phyCORE SBCs represent the continuous development of PHYTEC Single Board Computer technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments the phyCORE board design features an increased pin package. The increased pin package allows dedication of approximately 20 % of all pin header connectors on the phyCORE boards to ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards even in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD components and laser-drilled microvias are used on the boards, providing phyCORE users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCORE-i.MX35 is a subminiature (85 x 58 mm) insert-ready Single Board Computer populated with the Freescale i.MX35x microcontroller. Its universal design enables its insertion in a wide range of embedded applications. All controller signals and ports extend from the controller to high-density pitch (0.635 mm) connectors aligning two sides of the board, allowing it to be plugged like a "big chip" into a target application.

Precise specifications for the controller populating the board can be found in the applicable controller User's Manual or datasheet. The descriptions in this manual are based on the Freescale i.MX35x. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyCORE-i.MX35.

The phyCORE-I.MX35 offers the following features:

- Subminiature Single Board Computer (85 x 58 mm) achieved through modern SMD technology
- Populated with the Freescale i.MX35x microcontroller (MAPBGA 1568-01, 17x17mm, 0.8 Pitch packaging)
- Improved interference safety achieved through multi-layer PCB technology and dedicated ground pins
- Controller signals and ports extend to two 200-pin high-density (0.635 mm) Molex connectors aligning two sides of the board, enabling it to be plugged like a "big chip" into target application
- Max. 532 MHz core clock frequency
- Boot from NOR or NAND Flash
- 32 MByte (up to 64MByte) Intel Strata NOR Flash
- 1 GByte (up to 32 GByte) on-board NAND Flash[1]
- 128 MByte (up to 256 MByte) DDR2 SDRAM on-board
- RS-232 transceiver supporting one UART at data rates of up to 460kbps
- UART Interface without transceiver
- 32 KB I²C EEPROM
- Separate I²C RTC with backup function
- Integrated High-Speed USB OTG and Full-Speed USB Host PHYs
- Integrated 10/100MBit Ethernet Controller, Ethernet-PHY onboard
- Two integrated CAN Controllers
- All controller required supplies generated on board by Power-Supply device
- Synchronous 24Bit LCD-Interface
- 12-/16-bit CMOS Camera Interface
- Support of standard 20 pin debug interface through JTAG connector
- Keyboard support for up to 16 keys in a 4 * 4 matrix
- Two I²C interfaces
- SD/MMC card interface with DMA

1: *Please contact PHYTEC for more information about additional module configurations.*

1.2 Block Diagram

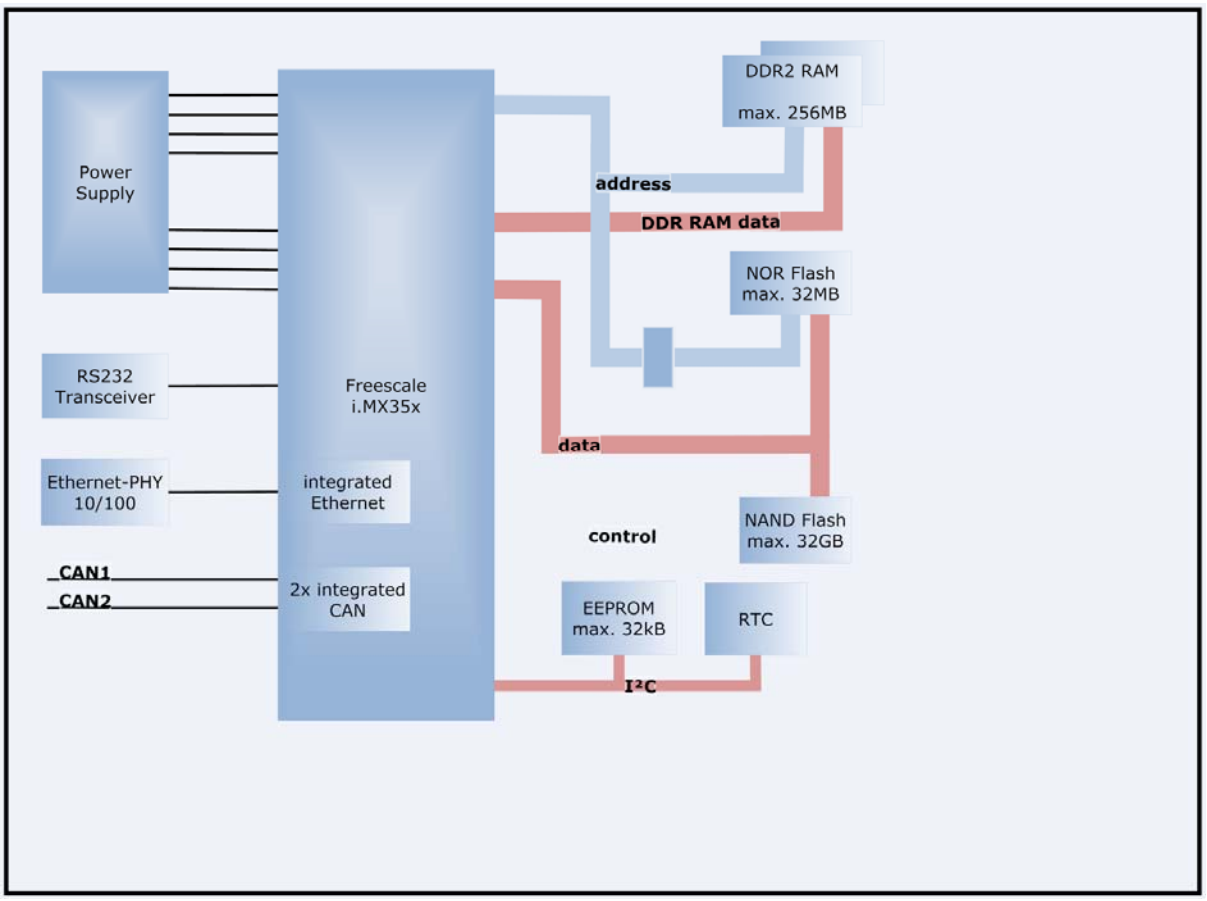

Figure 1: Block Diagram of the phyCORE-i.MX35

1.3 View of the phyCORE-i.MX35

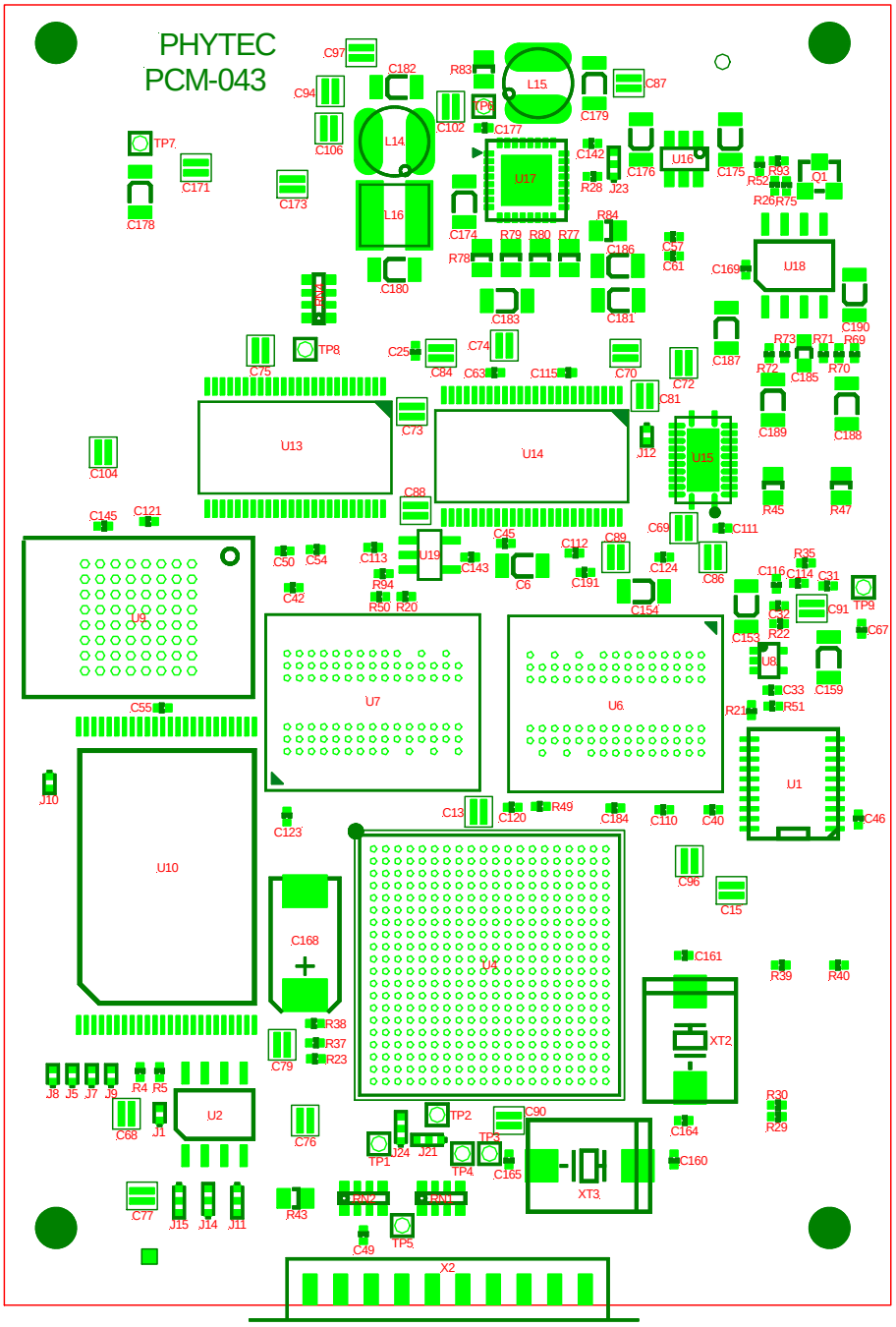

Figure 2: Top View of the phyCORE-i.MX35 (Controller Side)

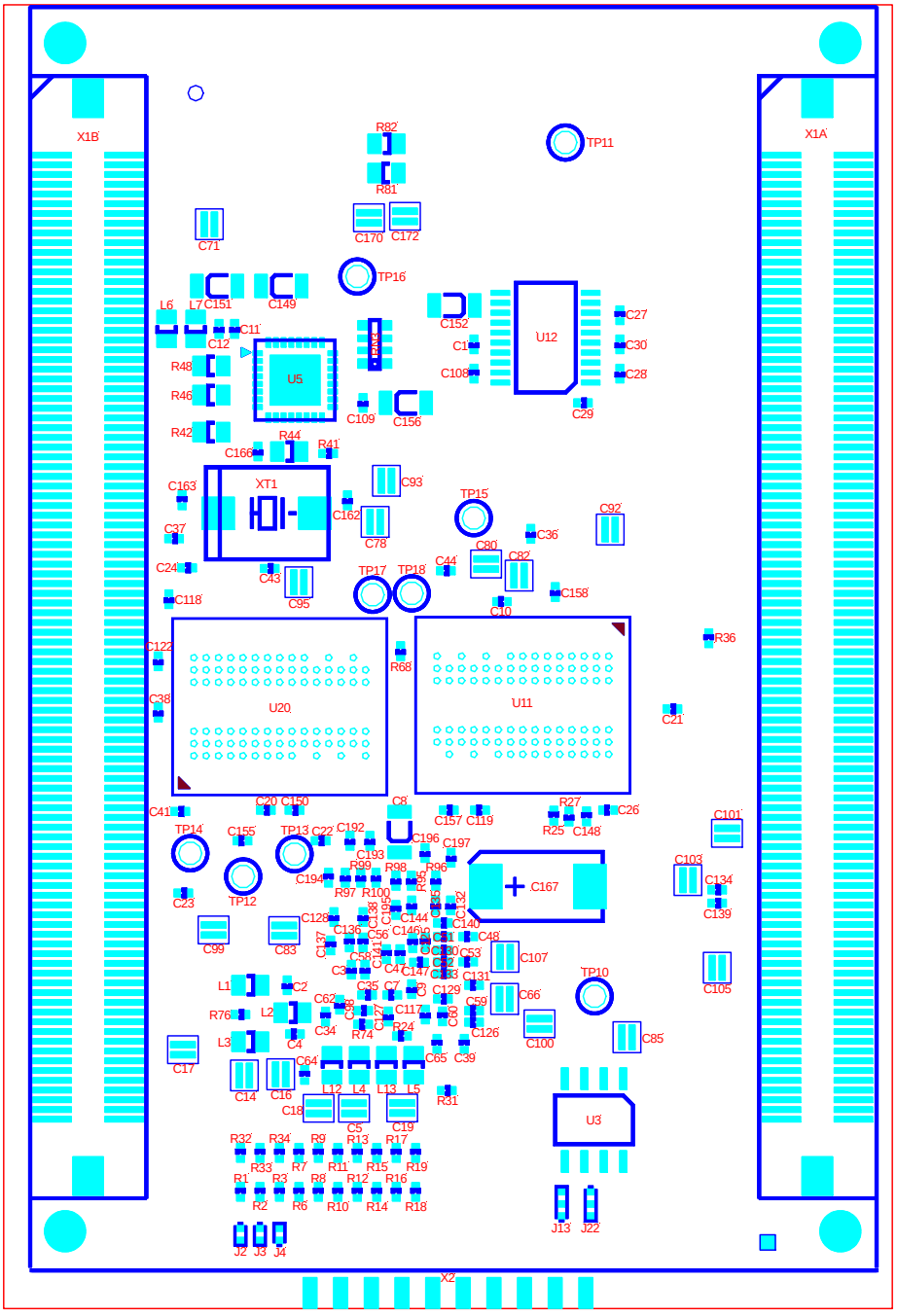

Figure 3: Bottom View of the phyCORE-i.MX35 (Connector Side)

2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Figure 4* indicates, all controller signals extend to surface mount technology (SMT) connectors (0.635 mm) lining two sides of the module (referred to as phyCORE-connector). This allows the phyCORE-i.MX35 to be plugged into any target application like a "big chip".

A new numbering scheme for the pins on the phyCORE-connector has been introduced with the phyCORE specifications. This enables quick and easy identification of desired pins and minimizes errors when matching pins on the phyCORE-module with the phyCORE-connector on the appropriate PHYTEC Development Board or in user target circuitry.

The numbering scheme for the phyCORE-connector is based on a two dimensional matrix in which column positions are identified by a letter and row position by a number. Pin 1A, for example, is always located in the upper left hand corner of the matrix. The pin numbering values increase moving down on the board. Lettering of the pin connector rows progresses alphabetically from left to right (*refer to Figure 4*).

The numbered matrix can be aligned with the phyCORE-i.MX35 (viewed from above; phyCORE-connector pointing down) or with the socket of the corresponding phyCORE Development Board/user target circuitry. The upper left-hand corner of the numbered matrix (pin 1A) is thus covered with the corner of the phyCORE-i.MX35 marked with a triangle. The numbering scheme is always in relation to the PCB as viewed from above, even if all connector contacts extend to the bottom of the module.

The numbering scheme is thus consistent for both the module’s phyCORE-connector as well as mating connectors on the phyCORE Development Board or target hardware, thereby considerably reducing the risk of pin identification errors.

Since the pins are exactly defined according to the numbered matrix previously described, the phyCORE-connector is usually assigned a single designator for its position (X1 for example). In this manner the phyCORE-connector comprises a single, logical unit regardless of the fact that it could consist of more than one physical socketed connector.
The location of row 1 on the board is marked by a triangle on the PCB to allow easy identification.

The following figure (*Figure 4*) illustrates the numbered matrix system. It shows a phyCORE-i.MX35 with SMT phyCORE-connectors on its underside (defined as dotted lines) mounted on a Development Board. In order to facilitate understanding of the pin assignment scheme, the diagram presents a cross-view of the phyCORE-module showing these phyCORE-connectors mounted on the underside of the module’s PCB.

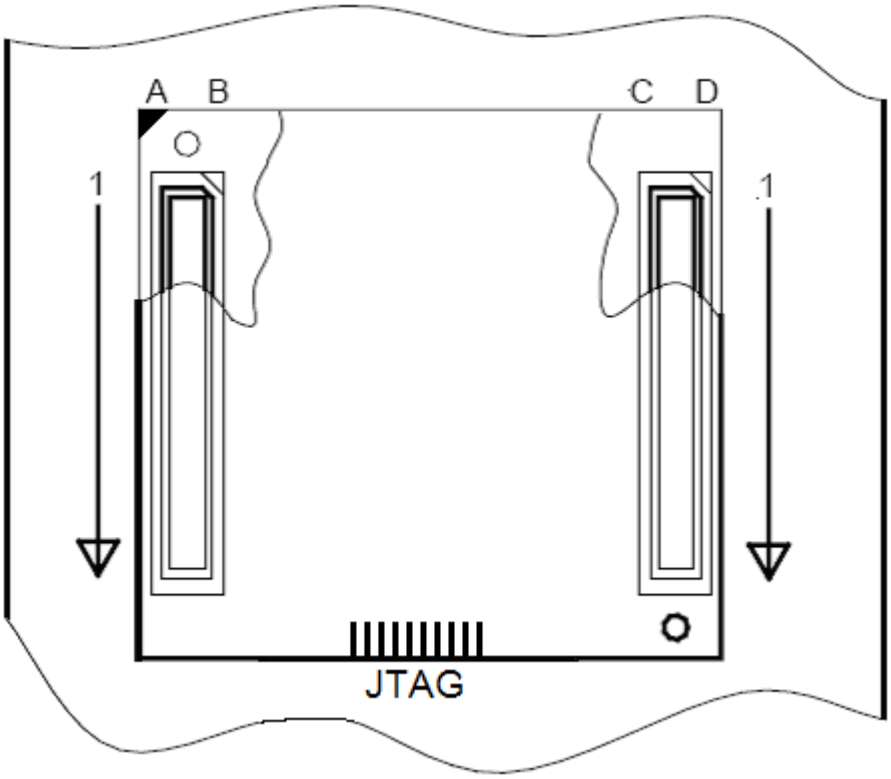

Figure 4: Pin-Out of the phyCORE-Connector (Top View, with Cross Section Insert)

Table 1 provides an overview of the pin-out of the phyCORE-connector, as well as descriptions of possible alternative functions.
Table 1 also provides the appropriate signal level interface voltages listed in the SL (**S**ignal **L**evel) column. The Freescale i.MX35 is a multi-voltage operated microcontroller and as such special attention should be paid to the interface voltage levels to avoid unintentional damage to the microcontroller and other on-board components. *Please refer to the Freescale i.MX35 User's Manual/Data Sheet for details on the functions and features of controller signals and port pins*.

Note:
SL is short for Signal Level (V) and is the applicable logic level to interface a given pin.

Table 1: Pin-out of the phyCORE-Connector X1

PIN ROW X1A				
PIN #	SIGNAL	I/O	SL	DESCRIPTION
1A	VDD_3V3	-	VDD_3V3	LCD reference voltage (3.3 V)
2A	GND	-	0	Ground 0 V
3A	not connected	-	-	Pin left unconnected
4A	not connected	-	-	Pin left unconnected
5A	X_LCD_VSYNC	I/O	VDD_3V3	Display vertical synchronization pulse
6A	not connected	-	-	Pin left unconnected
7A	GND	-	0	Ground 0 V
8A	X_LCD_REV	O	VDD_3V3	REV signal for display
9A	X_LCD_SPL	O	VDD_3V3	SPL/SPR signal for display
10A	X_LCD_DRDY	O	VDD_3V3	Data enable signal for display
11A	not connected	-	-	Pin left unconnected
12A	GND	-	0	Ground 0 V
13A	X_LCD_LD0	I/O	VDD_3V3	Input/Output data 0 to display
14A	X_LCD_LD2	I/O	VDD_3V3	Input/Output data 2 to display
15A	X_LCD_LD3	I/O	VDD_3V3	Input/Output data 3 to display
16A	X_LCD_LD5	I/O	VDD_3V3	Input/Output data 5 to display
17A	GND	-	0	Ground 0 V
18A	X_LCD_LD8	I/O	VDD_3V3	Input/Output data 8 to display
19A	X_LCD_LD10	I/O	VDD_3V3	Input/Output data 10 to display
20A	X_LCD_LD11	I/O	VDD_3V3	Input/Output data 11 to display
21A	X_LCD_LD13	I/O	VDD_3V3	Input/Output data 13 to display
22A	GND	-	0	Ground 0 V
23A	X_LCD_LD17	I/O	VDD_3V3	Input/Output data 17 to display
24A	X_LCD_LD18	I/O	VDD_3V3	Input/Output data 18 to display
25A	X_LCD_LD19	I/O	VDD_3V3	Input/Output data 19 to display
26A	X_LCD_LD21	I/O	VDD_3V3	Input/Output data 21 to display
27A	GND	-	0	Ground 0 V
28A	#CS0_3V3	O	VDD_3V3	Chip Select 0 output
29A	#CS1_3V3	O	VDD_3V3	Chip Select 1 output
30A	#CS4_3V3	O	VDD_3V3	Chip Select 4 output
31A	EB1_3V3	O	VDD_3V3	Active low external enable byte signal that controls D[7:0]
32A	GND	-	0	Ground 0 V

33A	#OE_3V3	O	VDD_3V3	Memory Output Enable
34A	LBA_3V3	O	VDD_3V3	Load Burst Address
35A	BCLK_3V3	O	VDD_3V3	Burst Clock
36A	A2_3V3	O	VDD_3V3	Address-Line A2
37A	GND	-	0	Ground 0 V
38A	A4_3V3	O	VDD_3V3	Address-Line A4
39A	A5_3V3	O	VDD_3V3	Address-Line A5
40A	A7_3V3	O	VDD_3V3	Address-Line A7
41A	A10_3V3	O	VDD_3V3	Address-Line A10
42A	GND	-	0	Ground 0 V
43A	A12_3V3	O	VDD_3V3	Address-Line A12
44A	A13_3V3	O	VDD_3V3	Address-Line A13
45A	A15_3V3	O	VDD_3V3	Address-Line A15
46A	A18_3V3	O	VDD_3V3	Address-Line A18
47A	GND	-	0	Ground 0 V
48A	A20_3V3	O	VDD_3V3	Address-Line A20
49A	A21_3V3	O	VDD_3V3	Address-Line A21
50A	A23_3V3	O	VDD_3V3	Address-Line A23
51A	D0	I/O	VDD_3V3	Data_Bus D0
52A	GND	-	0	Ground 0 V
53A	D2	I/O	VDD_3V3	Data_Bus D2
54A	D3	I/O	VDD_3V3	Data_Bus D3
55A	D5	I/O	VDD_3V3	Data_Bus D5
56A	D8	I/O	VDD_3V3	Data_Bus D8
57A	GND	-	0	Ground 0 V
58A	D10	I/O	VDD_3V3	Data_Bus D10
59A	D11	I/O	VDD_3V3	Data_Bus D11
60A	D13	I/O	VDD_3V3	Data_Bus D13
61A	VDD_1V8	-	VDD_1V8	1.8V supply voltage
62A	GND	-	0	Ground 0 V
63A	not connected	-	-	Pin left unconnected
64A	not connected	-	-	Pin left unconnected
65A	not connected	-	-	Pin left unconnected
66A	not connected	-	-	Pin left unconnected
67A	GND	-	0	Ground 0 V
68A	not connected		-	Pin left unconnected
69A	X_FEC_TDATA3	O	VDD_3V3	Fast Ethernet Transmit Data 3
70A	X_FEC_RX_ER R	I	VDD_3V3	Fast Ethernet Receive Data Error
71A	X_FEC_RDATA2	I	VDD_3V3	Fast Ethernet Receive Data 2
72A	GND	-	0	Ground 0 V

73A	X_FEC_MDC	O	VDD_3V3	Fast Ethernet Management Data Clock
74A	X_FEC_TX_CLK	I	VDD_3V3	Fast Ethernet Transmit Clock signal
75A	X_FEC_RDATA0	I	VDD_3V3	Fast Ethernet Receive Data 0
76A	X_FEC_RX_CLK	I	VDD_3V3	Fast Ethernet Receive Clock signal
77A	GND	-	0	Ground 0 V
78A	X_CSI_D6	I	VDD_3V3	Camera Sensor D6
79A	X_CSI_D8	I	VDD_3V3	Camera Sensor D8
80A	X_CSI_D9	I	VDD_3V3	Camera Sensor D9
81A	X_CSI_D11	I	VDD_3V3	Camera Sensor D11
82A	GND	-	0	Ground 0 V
83A	X_CSI_D14	I	VDD_3V3	Camera Sensor D14
84A	X_CSI_MCLK	O	VDD_3V3	Camera Sensor Master Clock
85A	X_CSI_VSYNC	I	VDD_3V3	Camera Sensor vertical sync
86A	X_CSI_PIXCLK	I	VDD_3V3	Camera Sensor pixel clock
87A	GND	-	0	Ground 0 V
88A	VDD_3V3	-	VDD_3V3	CSI and FEC supply voltage (3.3V)
89A	X_FEC_TX_EN	O	VDD_3V3	Fast Ethernet transmit enable signal
90A	X_KEY_COL0	I/O	VDD_3V3	Keypad Port Column 0
91A	X_KEY_COL1	I/O	VDD_3V3	Keypad Port Column 1
92A	GND	-	0	Ground 0 V
93A	X_KEY_COL2	I/O	VDD_3V3	Keypad Port Column 2
94A	X_KEY_COL3	I/O	VDD_3V3	Keypad Port Column 3
95A	not connected	-	-	Pin left unconnected
96A	X_GPIO2_6	I/O	VDD_3V3	GPIO2_6
97A	GND	-	0	Ground 0 V
98A	X_GPIO2_7	I/O	VDD_3V3	GPIO2_7
99A	X_GPIO2_23	I/O	VDD_3V3	GPIO2_23
100A	X_GPIO2_24	I/O	VDD_3V3	GPIO2_24

PIN ROW X1B				
PIN #	SIGNAL	I/O	SL	DESCRIPTION
1B	VDD_ALIVE	-	VDD_ALIVE	VDD-ALIVE from LDO of power-supply (1.2 V)
2B	X_VSTBY	O	VDD_3V3	I/O signal to PMIC
3B	X_OWIRE	I/O	VDD_3V3	One-Wire bus
4B	GND	-	0	Ground 0 V
5B	X_LCD_HSYNC	I/O	VDD_3V3	Display horizontal synchronization pulse
6B	not connected	-	-	Pin left unconnected
7B	X_LCD_CONTRAST	O	VDD_3V3	Contrast control for display
8B	X_LCD_CLS	O	VDD_3V3	CLS signal for display
9B	GND	-	0	Ground 0 V
10B	X_LCD_FPSHIFT	O	VDD_3V3	Display Shift Clock
11B	not connected	-	-	Pin left unconnected
12B	not connected	-	-	Pin left unconnected
13B	X_LCD_LD1	I/O	VDD_3V3	Input/Output data 1 to display
14B	GND	-	0	Ground 0 V
15B	X_LCD_LD4	I/O	VDD_3V3	Input/Output data 4 to display
16B	X_LCD_LD6	I/O	VDD_3V3	Input/Output data 6 to display
17B	X_LCD_LD7	I/O	VDD_3V3	Input/Output data 7 to display
18B	X_LCD_LD9	I/O	VDD_3V3	Input/Output data 9 to display
19B	GND	-	0	Ground 0 V
20B	X_LCD_LD12	I/O	VDD_3V3	Input/Output data 12 to display
21B	X_LCD_LD14	I/O	VDD_3V3	Input/Output data 14 to display
22B	X_LCD_LD15	I/O	VDD_3V3	Input/Output data 15 to display
23B	X_LCD_LD16	I/O	VDD_3V3	Input/Output data 16 to display
24B	GND	-	0	Ground 0 V
25B	X_LCD_LD20	I/O	VDD_3V3	Input/Output data 20 to display
26B	X_LCD_LD22	I/O	VDD_3V3	Input/Output data 22 to display
27B	X_LCD_LD23	I/O	VDD_3V3	Input/Output data 23 to display
28B	#CS3_3V3	O	VDD_3V3	Chip Select 3 output
29B	GND	-	0	Ground 0 V
30B	#CS5_3V3	O	VDD_3V3	Chip Select 5 output
31B	EB0_3V3	O	VDD_3V3	WEIM enable byte signal
32B	#RW_3V3	O	VDD_3V3	WEIM Read/Write signal
33B	ECB_WAIT_3V3	I	VDD_3V3	WEIM End Current Burst / Wait signal
34B	GND	-	0	Ground 0 V
35B	A0_3V3	O	VDD_3V3	Address-Line A0
36B	A1_3V3	O	VDD_3V3	Address-Line A1
37B	A3_3V3	O	VDD_3V3	Address-Line A3
38B	A6_3V3	O	VDD_3V3	Address-Line A6

39B	GND	-	0	Ground 0 V
40B	A8_3V3	O	VDD_3V3	Address-Line A8
41B	A9_3V3	O	VDD_3V3	Address-Line A9
42B	A11_3V3	O	VDD_3V3	Address-Line A11
43B	A14_3V3	O	VDD_3V3	Address-Line A14
44B	GND	-	0	Ground 0 V
45B	A16_3V3	O	VDD_3V3	Address-Line A16
46B	A17_3V3	O	VDD_3V3	Address-Line A17
47B	A19_3V3	O	VDD_3V3	Address-Line A19
48B	A22_3V3	O	VDD_3V3	Address-Line A22
49B	GND	-	0	Ground 0 V
50B	A24_3V3	O	VDD_3V3	Address-Line A24
51B	A25_3V3	O	VDD_3V3	Address-Line A25
52B	D1	I/O	VDD_3V3	Data_Bus D1
53B	D4	I/O	VDD_3V3	Data_Bus D4
54B	GND	-	0	Ground 0 V
55B	D6	I/O	VDD_3V3	Data_Bus D6
56B	D7	I/O	VDD_3V3	Data_Bus D7
57B	D9	I/O	VDD_3V3	Data_Bus D9
58B	D12	I/O	VDD_3V3	Data_Bus D12
59B	GND	-	0	Ground 0 V
60B	D14	I/O	VDD_3V3	Data_Bus D14
61B	D15	I/O	VDD_3V3	Data_Bus D15
62B	#X_FL_WP	I	VDD_3V3	NOR-Flash write-protect signal
63B	not connected	-	-	Pin left unconnected
64B	GND	-	0	Ground 0 V
65B	not connected	-	-	Pin left unconnected
66B	not connected	-	-	Pin left unconnected
67B	not connected	-	-	Pin left unconnected
68B	not connected	-	-	Pin left unconnected
69B	GND	-	0	Ground 0 V
70B	X_FEC_RDATA1	I	VDD_3V3	Fast Ethernet Receive Data 1
71B	X_FEC_RDATA3	I	VDD_3V3	Fast Ethernet Receive Data 3
72B	X_FEC_MDIO	I/O	VDD_3V3	Fast Ethernet Management Data Input/Output
73B	X_FEC_CRS	I	VDD_3V3	Fast Ethernet Carrier Sense enable
74B	GND	-	0	Ground 0 V
75B	X_FEC_RX_DV	I	VDD_3V3	Fast Ethernet Receive data valid signal
76B	X_FEC_COL	I	VDD_3V3	Fast Ethernet Collision signal
77B	X_FEC_TX_ERR	O	VDD_3V3	Fast Ethernet Transmit Data Error
78B	X_CSI_D7	I	VDD_3V3	Camera Sensor D7
79B	GND	-	0	Ground 0 V

80B	X_CSI_D10	I	VDD_3V3	Camera Sensor D10
81B	X_CSI_D12	I	VDD_3V3	Camera Sensor D12
82B	X_CSI_D13	I	VDD_3V3	Camera Sensor D13
83B	X_CSI_D15	I	VDD_3V3	Camera Sensor D15
84B	GND	-	0	Ground 0 V
85B	X_CSI_HSYNC	I	VDD_3V3	Camera Sensor horizontal sync
86B	X_FEC_TDATA0	O	VDD_3V3	Fast Ethernet Transmit Data 0
87B	X_FEC_TDATA1	O	VDD_3V3	Fast Ethernet Transmit Data 1
88B	X_FEC_TDATA2	O	VDD_3V3	Fast Ethernet Transmit Data 2
89B	GND	-	0	Ground 0 V
90B	X_KEY_ROW0	I/O	VDD_3V3	Keypad Port Row 0
91B	X_KEY_ROW1	I/O	VDD_3V3	Keypad Port Row 1
92B	X_KEY_ROW2	I/O	VDD_3V3	Keypad Port Row 2
93B	X_KEY_ROW3	I/O	VDD_3V3	Keypad Port Row 3
94B	GND	-	0	Ground 0 V
95B	not connected	-	-	Pin left unconnected
96B	not connected	-	-	Pin left unconnected
97B	not connected	-	-	Pin left unconnected
98B	not connected	-	-	Pin left unconnected
99B	GND	-	0	Ground 0 V
100B	X_CLKO	O	VDD_3V3	Clock out signal selected from internal clock signals

PIN ROW X1C				
PIN #	SIGNAL	I/O	SL	DESCRIPTION
1C	VIN	-	Power	Main Power Input (3.6 V - 5.5 V)
2C	VIN	-	Power	Main Power Input (3.6 V - 5.5 V)
3C	GND	-	0	Ground 0 V
4C	VIN	-	Power	Main Power Input (3.6 V - 5.5 V)
5C	VIN	-	Power	Main Power Input (3.6 V - 5.5 V)
6C	X_BKUP_SUPPLY	-	-	Backup power supply for the ext. RTC
7C	GND	-	0	Ground 0 V
8C	VDD_3V3	-	VDD_3V3	Power for 3.3 V devices
9C	VDD_3V3	-	VDD_3V3	Power for 3.3 V devices
10C	VDD_3V3	-	VDD_3V3	Power for 3.3 V devices
11C	VDD_3V3	-	VDD_3V3	Power for 3.3 V devices
12C	GND	-	0	Ground 0 V
13C	X_MVDD_BKUP	-	MVDD_BKUP	alternate MPLL supply for i.MX35x
14C	X_PVCC_BKUP	-	PVCC_BKUP	alternate PPLL supply for i.MX35x
15C	not connected	-	-	Pin left unconnected
16C	not connected	-	-	Pin left unconnected
17C	GND	-	0	Ground 0 V
18C	not connected	-	-	Pin left unconnected
19C	not connected	-	-	Pin left unconnected
20C	not connected	-	-	Pin left unconnected
21C	not connected	-	-	Pin left unconnected
22C	GND	-	0	Ground 0 V
23C	X_SCK4	I/O	VDD_3V3	SSI serial clock
24C	X_STXFS4	I/O	VDD_3V3	SSI serial transmit frame sync
25C	X_STXD4	O	VDD_3V3	SSI serial transmit Data
26C	X_SRXD4	I	VDD_3V3	SSI serial receive Data
27C	GND	-	0	Ground 0 V
28C	not connected	-	-	Pin left unconnected
29C	not connected	-	-	Pin left unconnected
30C	not connected	-	-	Pin left unconnected
31C	not connected	-	-	Pin left unconnected
32C	GND	-	0	Ground 0 V
33C	X_ETH_LINK	O	VDD_3V3	Ethernet Link & Activity Indicator (Open Drain)
34C	X_ETH_SPEED	O	VDD_3V3	Ethernet Speed Indicator (Open Drain)
35C	X_ETH_RX-	I/O	VDD_3V3	Receive negative input (normal) Transmit negative output (reversed)
36C	X_ETH_TX-	I/O	VDD_3V3	Transmit negative output (normal) Receive negative input (reversed)

37C	GND	-	0	Ground 0 V
38C	#X_ETH_INT	O	VDD_3V3	Ethernet Phy interrupt output
39C	#X_CPU_DE	I	VDD_3V3	JTAG debug enable
40C	X_CPU_RTCK	O	VDD_3V3	JTAG test clock
41C	#X_CPU_TRST	I	VDD_3V3	JTAG test reset
42C	GND	-	0	Ground 0 V
43C	X_SCKT	I/O	VDD_3V3	Audio transmitter serial clock
44C	X_FST	I/O	VDD_3V3	Audio frame sync for transmitter
45C	X_HCKT	I/O	VDD_3V3	Audio high frequency clock for transmitter
46C	X_SCKR	I/O	VDD_3V3	Audio receiver serial clock
47C	GND	-	0	Ground 0 V
48C	X_FSR	I/O	VDD_3V3	Audio frame sync for receiver
49C	VDD_3V3	-	VDD_3V3	SD reference voltage (3.3 V)
50C	X_SD2_CLK	O	VDD_3V3	Clock for MMC/SD/SDIO 2 card
51C	X_SD2_CMD	I/O	VDD_3V3	SD2 CMD line connect to card
52C	GND	-	0	Ground 0 V
53C	X_USBPHY1_VBUS	I/O	5V (SW3)	USB1 VBUS Voltage
54C	X_USBPHY1_DM	I/O	VDD_3V3	USB1 transceiver cable interface, D-
55C	X_USBPHY1_DP	I/O	VDD_3V3	USB1 transceiver cable interface, D+
56C	X_USBPHY1_UID	I/O	VDD_3V3	USB1 on the go transceiver cable ID resistor connection
57C	GND	-	0	Ground 0 V
58C	not connected	-	-	Pin left unconnected
59C	X_USBOTG_CLK	I	VDD_3V3	USB OTG clock signal
60C	X_USBH2_CLK	I	VDD_3V3	USB Host2 clock signal
61C	X_USBOTG_DIR	I	VDD_3V3	USB OTG data direction
62C	GND	-	0	Ground 0 V
63C	X_USBOTG_DATA2	I/O	VDD_3V3	USB OTG data line 2
64C	X_USBOTG_DATA4	I/O	VDD_3V3	USB OTG data line 4
65C	X_USBOTG_DATA6	I/O	VDD_3V3	USB OTG data line 6
66C	not connected	-	VDD_3V3	Pin left unconnected
67C	GND	-	0	Ground 0 V
68C	X_SD1_DATA0	I/O	VDD_3V3	SD/MMC 1 Data0 line in all modes also used to detect busy state
69C	X_SD1_DATA1	I/O	VDD_3V3	SD/MMC 1 Data1 line in 4/8-bit mode also used to detect interrupt in 1/4-bit mode
70C	X_SD1_DATA2	I/O	VDD_3V3	SD/MMC 1 Data2 line or Read wait in 4-bit mode Read wait in 1-bit mode
71C	X_SD1_DATA3	I/O	VDD_3V3	SD/MMC 1 Data3 line in 4/8-bit mode or configured as card detection pin may be configured as card detection pin in 1-bit mode
72C	GND	-	0	Ground 0 V

73C	X_UART1_RTS	I	VDD_3V3	Request to send UART 1
74C	X_UART1_CTS	O	VDD_3V3	Clear to send UART 1
75C	X_UART1_RI	I/O	VDD_3V3	Ring Indicator UART 1
76C	X_UART1_DCD	I/O	VDD_3V3	Data carrier detect UART1
77C	GND	-	0	Ground 0 V
78C	not connected	-	-	Pin left unconnected
79C	not connected	-	-	Pin left unconnected
80C	not connected	-	-	Pin left unconnected
81C	not connected	-	-	Pin left unconnected
82C	GND	-	0	Ground 0 V
83C	X_I2C3_SCL	I/O	VDD_3V3	I²C 3 Serial Clock
84C	X_I2C3_SDA	I/O	VDD_3V3	I²C 3 Serial Data
85C	X_I2C1_DAT	I/O	VDD_3V3	I²C 1 Serial Data
86C	X_CSPI1_SCLK	I/O	VDD_3V3	SPI 1 clock
87C	GND	-	0	Ground 0 V
88C	X_CSPI1_SS0	I/O	VDD_3V3	SPI 1 Chip select 0
89C	X_CSPI1_SPI_RDY	I/O	VDD_3V3	SPI 1 SPI data ready in Master mode
90C	X_CSPI2_MOSI	I/O	VDD_3V3	SPI 2 Master data out; slave data in
91C	X_CSPI2_SCLK	I/O	VDD_3V3	SPI 2 clock
92C	GND	-	0	Ground 0 V
93C	not connected	-	-	Pin left unconnected
94C	not connected	-	-	Pin left unconnected
95C	not connected	-	-	Pin left unconnected
96C	not connected	-	-	Pin left unconnected
97C	GND	-	0	Ground 0 V
98C	X_BOOT0	I/O	VDD_3V3	Boot-Mode 0
99C	X_BOOT1	I/O	VDD_3V3	Boot-Mode 1
100C	VDD_3V3	-	VDD_3V3	Boot-Mode reference voltage (3.3 V)

PIN ROW X1D				
PIN #	SIGNAL	I/O	SL	DESCRIPTION
1D	VIN	-	Power	Main Power Input (3.6 V - 5.5 V)
2D	VIN	-	Power	Main Power Input (3.6 V – 5.5 V)
3D	GND	-	0	Ground 0 V
4D	not connected	-	-	Pin left unconnected
5D	#X_MASTER_RESET	I	VDD_3V3	Master Reset Input/Reset button
6D	#X_RESET_MCU	O	VDD_3V3	Reset Output from reset unit
7D	X_FUSE_VDD	-	FUSE_VDD	Fusebox write (program) Supply Voltage (3.3 V)
8D	X_TOUT	O	VDD_3V3	Open-Drain Thermostat Output of U3 (DS75)
9D	GND	-	0	Ground 0 V
10D	not connected	-	-	Pin left unconnected
11D	not connected	-	-	Pin left unconnected
12D	not connected	-	-	Pin left unconnected
13D	not connected	-	-	Pin left unconnected
14D	GND	-	0	Ground 0 V
15D	X_EN_VDD_3V3	I	VIN	Enable for 3.3 V power switch
16D	X_EN_VDD_1V8	I	VIN	Enable for 1.8 V power switch
17D	X_EN_VDD_1V375	I	VIN	Enable for 1.375 V power switch
18D	X_EN_LDO1_2	I	VIN	Enable for power-supply LDO (3.3 V,1.8 V)
19D	GND	-	0	Ground 0 V
20D	X_EN_VDD_ALIVE	I	VIN	Enable for VDD_ALIVE LDO (1.2 V)
21D	not connected	-	-	Pin left unconnected
22D	X_UART2_RXD	I	VDD_3V3	Serial Data receive line UART 2
23D	X_UART2_TXD	O	VDD_3V3	Serial Data transmit line UART 2
24D	GND	-	0	Ground 0 V
25D	X_UART2_RTS	I	VDD_3V3	Request to send UART 2
26D	X_UART2_CTS	O	VDD_3V3	Clear to send UART 2
27D	X_CAPTURE	I	VDD_3V3	Timer input capture
28D	X_COMPARE	O	VDD_3V3	Timer output compare
29D	GND	-	0	Ground 0 V
30D	X_CAN2_TX	O	VDD_3V3	CAN 2 transmit
31D	X_CAN2_RX	I	VDD_3V3	CAN 2 receive
32D	X_CAN1_TX	O	VDD_3V3	CAN 1 transmit
33D	X_CAN1_RX	I	VDD_3V3	CAN 1 receive
34D	GND	-	0	Ground 0 V
35D	X_ETH_RX+	I/O	VDD_3V3	Receive positive input (normal) Transmit positive output (reversed)

36D	X_ETH_TX+	I/O	VDD_3V3	Transmit positive output (normal) Receive positive input (reversed)
37D	VDD_3V3	-	VDD_3V3	JTAG reference voltage (3.3 V)
38D	X_CPU_TCK	I	VDD_3V3	JTAG clock
39D	GND	-	0	Ground 0 V
40D	X_CPU_TDI	I	VDD_3V3	JTAG Data In
41D	X_CPU_TDO	O	VDD_3V3	JTAG Data Out
42D	X_CPU_TMS	I	VDD_3V3	JTAG Mode select
43D	X_JTAG_MODE	I	VDD_3V3	JTAG Mode
44D	GND	-	0	Ground 0 V
45D	X_MLB_CLK	I	VDD_3V3	Media local bus clock input
46D	X_MLB_DAT	I/O	VDD_3V3	Media local bus data input/output
47D	X_MLB_SIG	I/O	VDD_3V3	Media local bus signal information I/O
48D	VDD_3V3	-	VDD_3V3	SD/MMC reference voltage (3.3 V)
49D	GND	-	0	Ground 0 V
50D	X_SD2_DATA0	I/O	VDD_3V3	SD/MMC 2 Data0 line in all modes also used to detect busy state
51D	X_SD2_DATA1	I/O	VDD_3V3	SD/MMC 2 Data1 line in 4/8-bit mode also used to detect interrupt in 1/4-bit mode
52D	X_SD2_DATA2	I/O	VDD_3V3	SD/MMC 2 Data2 line or Read wait in 4-bit mode Read wait in 1-bit mode
53D	X_SD2_DATA3	I/O	VDD_3V3	SD/MMC 2 Data3 line in 4/8-bit mode or configured as card detection pin may be configured as card detection pin in 1-bit mode
54D	GND	-	0	Ground 0 V
55D	X_USBOTG_PWR	O	VDD_3V3	USB Generic Power switch output
56D	X_USBOTG_OC	I	VDD_3V3	USB Generic Over Current input
57D	X_USBPHY2_DP	I/O	VDD_3V3	USB2 transceiver cable interface, D+
58D	X_USBPHY2_DM	I/O	VDD_3V3	USB2 transceiver cable interface, D-
59D	GND	-	0	Ground 0 V
60D	X_USBOTG_STP	O	VDD_3V3	USB OTG stop signal
61D	X_USBOTG_NXT	I	VDD_3V3	USB OTG next signal
62D	X_USBOTG_DATA0	I/O	VDD_3V3	USB OTG data line 0
63D	X_USBOTG_DATA1	I/O	VDD_3V3	USB OTG data line 1
64D	GND	-	0	Ground 0 V
65D	X_USBOTG_DATA3	I/O	VDD_3V3	USB OTG data line 3
66D	X_USBOTG_DATA5	I/O	VDD_3V3	USB OTG data line 5
67D	X_USBOTG_DATA7	I/O	VDD_3V3	USB OTG data line 7
68D	X_SD1_CMD	I/O	VDD_3V3	SD1 CMD line connect to card
69D	GND	-	0	Ground 0 V
70D	X_SD1_CLK	O	VDD_3V3	Clock for MMC/SD/SDIO 1 card
71D	not connected	-	-	Pin left unconnected

72D	X_UART1_TXD	O	VDD_3V3	Serial data transmit signal UART 1
73D	X_UART1_RXD	I	VDD_3V3	Serial data receive signal UART 1
74D	GND	-	0	Ground 0 V
75D	X_UART1_DSR	I/O	VDD_3V3	Data set ready UART1
76D	X_UART1_DTR	I/O	VDD_3V3	Data terminal ready
77D	not connected	-	-	Pin left unconnected
78D	not connected	-	-	Pin left unconnected
79D	GND	-	0	Ground 0 V
80D	not connected	-	-	Pin left unconnected
81D	not connected	-	-	Pin left unconnected
82D	X_#IRQRTC	O	VDD_3V3	Interrupt Output from RTC U1 (RTC-8564JE)
83D	not connected	-	-	Pin left unconnected
84D	GND	-	0	Ground 0 V
85D	X_I2C1_CLK	I/O	VDD_3V3	I²C 1 Serial Clock
86D	X_CSPI1_MOSI	I/O	VDD_3V3	SPI 1 Master data out; slave data in
87D	X_CSPI1_MISO	I/O	VDD_3V3	SPI 1 Master data in; slave data out
88D	X_CSPI1_SS1	I/O	VDD_3V3	SPI 1 Chip select 1
89D	GND	-	0	Ground 0 V
90D	X_CSPI2_MISO	I/O	VDD_3V3	SPI 2 Master data in; slave data out
91D	X_CSPI2_SPI_RDY	I/O	VDD_3V3	SPI 2 SPI data ready in Master mode
92D	X_CSPI2_SS0	I/O	VDD_3V3	SPI 2 Chip select 0
93D	not connected	-	-	Pin left unconnected
94D	GND	-	0	Ground 0 V
95D	not connected	-	-	Pin left unconnected
96D	X_BOOT3	I/O	VDD_3V3	Boot-Mode 3
97D	X_BOOT4	I/O	VDD_3V3	Boot-Mode 4
98D	X_BOOT5	I/O	VDD_3V3	Boot-Mode 5
99D	GND	-	0	Ground 0 V
100D	X_PWMO	O	VDD_3V3	Pulse Width Modulator Output

3 Jumpers

For configuration purposes, the phyCORE-i.MX35 has 18 solder jumpers, some of which have been installed prior to delivery. *Figure 5* illustrates the numbering of the solder jumper pads, while *Figure 6* and *Figure 7* indicate the location of the solder jumpers on the board. 13 solder jumpers are located on the top side of the module (opposite side of connectors) and 5 solder jumpers are located on the bottom side of the module (connector side). *Table 2* below provides a functional summary of the solder jumpers, their default positions, and possible alternative positions and functions. A detailed description of each solder jumper can be found in the applicable section listed in the table.

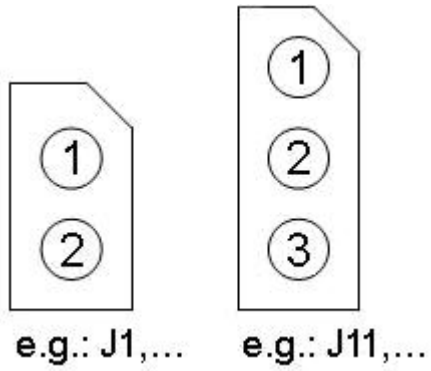

Figure 5: Typical Jumper Pad Numbering Scheme

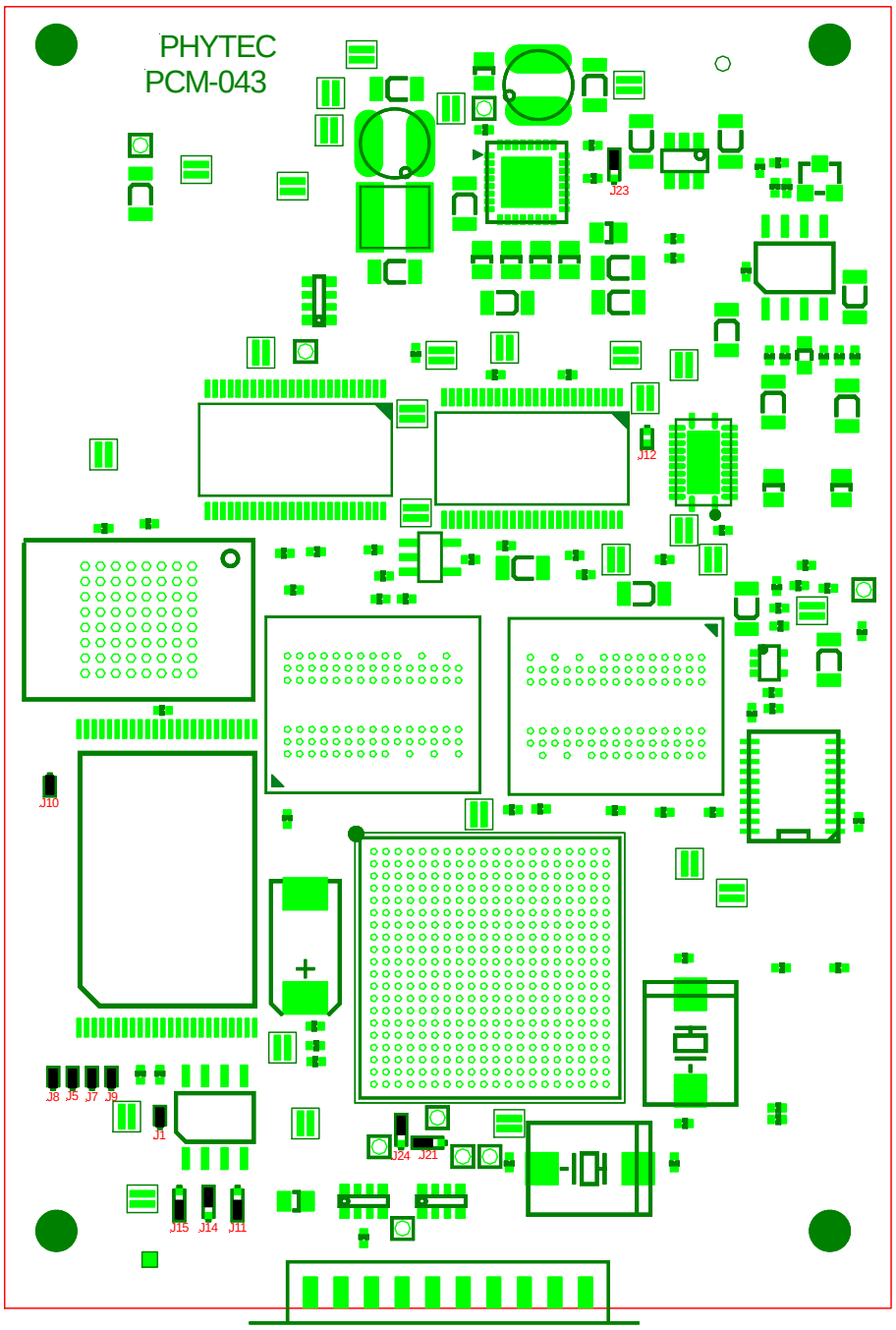

Figure 6: Jumper Locations (Top View)

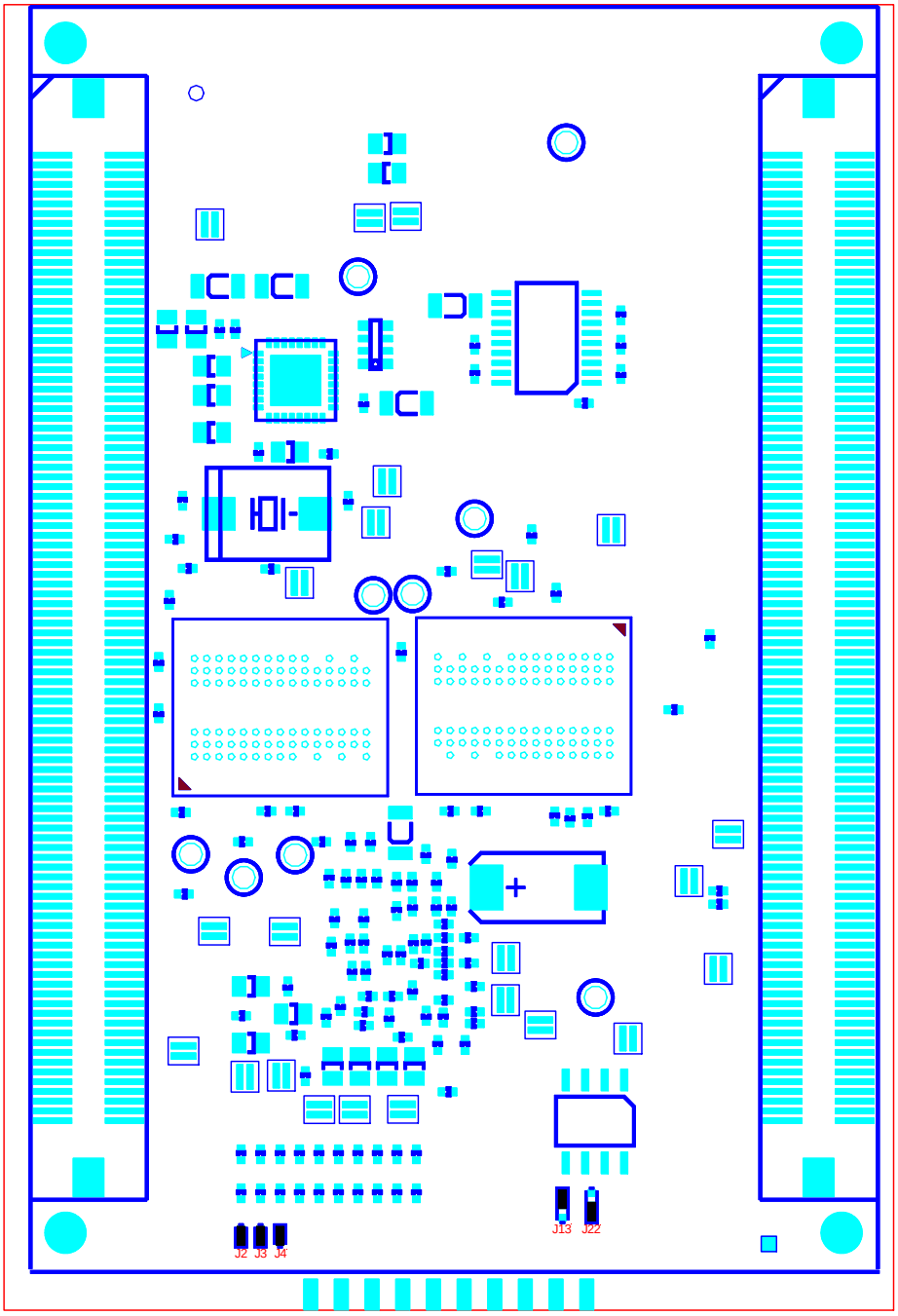

Figure 7: Jumper Locations (Bottom View)

The jumpers (J = solder jumper) have the following functions:

Table 2: Jumper settings

	Default Setting		Alternative Setting		See Section
J1	closed	EEPROM U2 is not write protected	open	EEPROM U2 is write protected	7.5.2
J2	closed	10k pull-down resistor to Dip-Switch for boot select X_BOOT2 (NOR/NAND)	open	X_BOOT2 is not connected to Dip-Switch	6.1.2
J3	closed	10k pull-down resistor to Dip-Switch for boot select X_BOOT3 (MEM_TYPE[0])	open	X_BOOT3 is not connected to DIP-Switch	
J4	closed	10k pull-down resistor to Dip-Switch for boot select X_BOOT4 (MEM_TYPE[1])	open	X_BOOT4 is not connected to DIP-Switch	
J5	closed	Connects NFRB-signal from the i.MX35x to R/#B2 pin of the NAND-Flash	open	NFRB-signal from the i.MX35x is not connected to R/#B2 pin of the NAND-Flash	
J7	closed	Connects NFRB-signal from the i.MX35x to R/#B1 pin of the NAND-Flash	open	NFRB-signal from the i.MX35x is not connected to R/#B1 pin of the NAND-Flash	
J8	closed	Connects NFRB-signal from the i.MX35x to R/#B3 pin of the NAND-Flash	open	NFRB-signal from the i.MX35x is not connected to R/#B3 pin of the NAND-Flash	
J9	closed	Connects NFRB-signal from the i.MX35x to R/#B pin of the NAND-Flash	open	NFRB-signal from the i.MX35x is not connected to R/#B pin of the NAND-Flash	
J10	closed	#CS1_3V3 is connected to NANDF_CE3_3V3 to use alternate function NF_CE3	open	#CS1_3V3 is not connected to NANDF_CE3_3V3	
J11	2 + 3	EEPROM A2 is connected to GND (low)	1 + 2	EEPROM A2 is connected to VDD_3V3 (high)	7.5.1
J12	closed	only 1 DDR bank populated, CSD1 can be used as CS3_3V3 connected to the molex connector	open	2 DDR banks populated, CSD1 is used for the 2nd DDR bank, signal is not connected to the molex connector	
J13	2 + 3	DS75 A2 is connected to GND (low)	1 + 2	DS75 A2 is connected to VDD_3V3 (high)	
J14	2 + 3	EEPROM A1 is connected to VDD_3V3 (high)	1 + 2	EEPROM A1 is connected to GND (low)	7.5.1
J15	2 + 3	EEPROM A0 is connected to GND (low)	1 + 2	EEPROM A0 is connected to VDD_3V3 (high)	

J22	2 + 3	DS75 A1 is connected to VDD_3V3 (high)	1 + 2	DS75 A1 is connected to GND (low)	

4 Power Requirements

The phyCORE-i.MX35 normally operates off of one voltage supply denoted as **VIN**. The TPS650241 primary on-board voltage regulator operates off of VIN and generates all on-board supply voltages.

The phyCORE-i.MX Carrier Board generates VIN. VIN is sourced from either the wall socket input, or a battery.

The input voltage VIN should be 5 V, with a nominal current allowance of at least 3 A.

See Table 1 from section 2 above for applicable VIN power pins on the phyCORE-connector.

Caution!
Connect all VIN input pins to your power supply.

As a general design rule we recommend connecting all GND pins which are neighboring signals being used in the application circuitry.

The i.MX35x CPU is supplied by different power domains.

Table 3: i.MX35 default power input voltages

POWER OUTPUT	POWER-DOMAIN	STARTUP VOLTAGE-LEVEL
Power switch 1 of U17	VDD_3V3	3.3 V
Power switch 2 of U17	VDD_1V8	1.8 V
Power switch 3 of U17	VDD_1V375	1.375 V
LDO 1 of U17	LDO_3V3	3.3 V
LDO 2 of U17	LDO_1V5	1.5 V
LDO VDD_ALIVE of U17	VDD_ALIVE	1.2 V

Note:
Phytec recommends to use the different power sources that are connected to the molex connectors of the phyCORE-i.MX35 only as reference.
The current that could be externally drawn from the VCC_3V3 supply is max 500 mA..

5 Real Time Clock U1 Backup-Voltage

In case of a power fail or a user off event the backup-voltage X_BKUP_SUPPLY provides power to the I²C Real Time Clock U1 (RTC8564JE). In this case a backup coincell could supply the RTC via X_BKUP_SUPPLY.

6 System Configuration

Although most features of the Freescale phyCORE-i.MX35 microcontroller are configured and/or programmed during the initialization routine, other features, which impact program execution, must be configured prior to initialization via pin termination.

6.1 System Startup Configuration

During the reset cycle the i.MX35 processor reads the state of selected controller signals to determine the basic system configuration. The configuration circuitries (pull-up or pull-down resistors) are located on the phyCORE module. They are already set, so no further settings are necessary.

6.1.1 Power-Up-Mode

Note:
The i.MX35x controller has a defined power up sequence. *Refer to the i.MX35 Data Sheet, chapter 3.3 Power-Up sequence.*

6.1.2 Boot Mode Select

The i.MX35x controller has different boot modes, which can be selected. The system boot mode of the processor is determined by the configuration of the five external input pins, BOOT[4:0].

Table 4: Basic Boot Modes of i.MX35x Module

Boot Mode Selection		**Boot Mode / Device**
BOOT 1	BOOT 0	
0	0	Internal boot
1	0	External boot
1	1	Enter wait mode

Table 5: Advanced Boot Modes of i.MX35x Module

Boot Mode Selection					**Boot Mode / Device**
BOOT 4	BOOT 3	BOOT 2	BOOT 1	BOOT 0	
0	0	0	1	0	Boot from NOR Flash
0	0	1	1	0	Boot from NAND-Flash (3 address cycles)
0	1	1	1	0	Boot from NAND-Flash (4 address cycles)
1	0	1	1	0	Boot from NAND-Flash (5 address cycles)
1	1	1	1	0	Boot from NAND-Flash (6 address cycles)

The phyCORE-i.MX35 module comes with a standard boot configuration of **'00010'**, so the system will boot from the 16-bit NOR-Flash at CS0.

7 System Memory

The phyCORE-i.MX35 provides three types of on-board memory:

- DDR2-SDRAM: 128MByte (up to 256MByte)
- NAND Flash: 1GByte (up to 32GByte)
- NOR Flash: 32MByte (up to 64MByte)
- I²C-EEPROM: 32KB (up to 32KByte)

It should be noted that the DDR2-SDRAM has a dedicated memory bus to the i.MX35x microcontroller. The DDR2-SDRAM bus is therefore not made available at the phyCORE-connector X1.

7.1 Memory Model

The i.MX35x memory map is summarized in *Table 6* below. *For a detailed view of the memory map please consult the Freescale i.MX35 User's Manual*.

Table 6: i.MX35 Memory Map

ADDRESS	CHIP-SELECT	FUNCTION
0x8000 0000 – 0x8FFF FFFF	CSD0	DDR2-SDRAM Bank 0 (U6, U7)
0x9000 0000 – 0x9FFF FFFF	CSD1	not used on phyCORE-i.MX35
0xA000 0000 – 0xA7FF FFFF	WEIM CS0 (flash 128)[1]	NOR-Flash (U9)
0xA800 0000 – 0xAFFF FFFF	WEIM CS1 (flash 64)	multiplexed with NANDF_CE3
0xB000 0000 – 0xB1FF FFFF	WEIM CS2 (SRAM)	used as CSD0
0xB200 0000 – 0xB3FF FFFF	WEIM CS3	not used on phyCORE-i.MX35
0xB400 0000 – 0xB5FF FFFF	WEIM CS4	not used on phyCORE-i.MX35
0xB600 0000 – 0xB7FF FFFF	WEIM CS5	not used on phyCORE-i.MX35
0xBB00 0000 – 0xBB00 11FF	NFC memory region[1] (4K, NAND Flash)	NAND-Flash (U10)

1. Can be used as a boot memory region

7.2 DDR2-SDRAM (U6-U7)

The phyCORE-i.MX35 has one bank of DDR2-SDRAMs on the i.MX35x module.

The RAM bank is comprised of two 16-bit wide DDR2-SDRAM chips, configured for 32-bit access, and operating at 133MHz. In lower density configurations, U6 and U7 populate the module and are accessed via SDRAM memory bank 0 using chip select signal /CSD0 starting at 0x8000 0000.
Actually there is no RAM bank 1 for the i.MX35x. So the /CSD1 chip select line is freed and can be used as /CS3.

Typically the DDR2-SDRAM initialization is performed by a boot loader or operating system following a power-on reset and must not be changed at a later point by any application code. When writing custom code independent of an operating system or boot loader, SDRAM must be initialized by accessing the appropriate SDRAM configuration registers on the i.MX35x controller. *Refer to the i.MX35 User Manual for accessing and configuring these registers.*

7.3 NOR-Flash (U9)

The phyCORE-i.MX35 can be populated with an Intel Strata Flash at U9. This NOR-Flash is connected to /CS0 which is located at memory address 0xA000 0000. The entire Flash can be write protected by pulling the x_/FL_WP signal, located at the phyCORE-connector X1 on pin 62B, low.

The following NOR-Flash devices can be used on the phyCORE-i.MX35:

Table 7: Compatible NOR Flash Devices

MANUFACTURER	NOR FLASH P/N	DENSITY (MBYTE)
Intel/Numonyx	PC28F640P33	8
Intel/Numonyx	PC28F128P33	16
Intel/Numonyx	PC28F256P33	32

7.4 NAND Flash Memory (U10)

Use of Flash as non-volatile memory on the phyCORE-i.MX35 provides an easily reprogrammable means of code storage. The following Flash devices can be used on the phyCORE-i.MX35:

Table 8: Compatible NAND Flash Devices

MANUFACTURER	NAND FLASH P/N	DENSITY (MBYTE)
Numonyx	NAND01G-xxx	1024
Numonyx	NAND02G-xxx	2048

Additionally, any parts that are footprint (TSOP) and functionally compatible with the NAND Flash devices listed above may also be used with the phyCORE-i.MX35.

These Flash devices are programmable with 3.3 V. No dedicated programming voltage is required.

As of the printing of this manual these NAND Flash devices generally have a life expectancy of at least 100,000 erase/program cycles and a data retention rate of 10 years.

7.5 I²C EEPROM (U2)

The phyCORE-i.MX35 is populated with a ST 24W32C[1] non-volatile 32 KByte EEPROM (U2) with an I²C interface to store configuration data or other general purpose data. This device is accessed through I²C port 1 on the i.MX35x. The serial clock signal and serial data signal for I²C port 1 are made available at the phyCORE-connector as X_I2C1_DAT on X1 pin 85C and X_I2C1_CLK on X1 pin 85D.

Three solder jumpers are provided to set the lower address bits: J11, J14, and J15. *Refer to section 7.5.1 for details on setting these jumpers.*

Write protection to the device is accomplished via jumper J1. By default this jumper is closed, allowing write access to the EEPROM. Removing this jumper will cause the EEPROM to enter write protect mode, thereby disabling write access to the device. *Refer to section 7.5.2 for further details on setting this jumper.*

1: *See the manufacturer's data sheet for interfacing and operation.*

7.5.1 Setting the EEPROM Lower Address Bits (J11, J14, J15)

The 32 KB I²C EEPROM populating U2 on the phyCORE-module has the capability of configuring the lower address bits A0, A1, and A2. The four upper address bits of the device are fixed at '1010' (*see ST 24W32C data sheet).* The remaining three lower address bits of the seven bit I²C device address are configurable using jumpers J11, J14 and J15. J15 sets address bit A0, J14 address bit A1, and J11 address bit A2.

Table 9 below shows the resulting seven bit I²C device address for the eight possible jumper configurations.

Table 9: U2 EEPROM I²C Address via J11, J14, and J15[1]

U2 I²C Device Address	J11	J14	J15
1010 010	**2 + 3**	**2 + 3**	**2 + 3**
1010 011	2 + 3	2 + 3	1 + 2
1010 000	2 + 3	1 + 2	2 + 3
1010 001	2 + 3	1 + 2	1 + 2
1010 110	1 + 2	2 + 3	2 + 3
1010 111	1 + 2	2 + 3	1 + 2
1010 100	1 + 2	1 + 2	2 + 3
1010 101	1 + 2	1 + 2	1 + 2

1: *Defaults are in **bold blue** text*

7.5.2 EEPROM Write Protection Control (J1)

Jumper J1 controls write access to the EEPROM (U2) device. Closing this jumper allows write access to the device, while opening this jumper enables write protection.

The following configurations are possible:

Table 10: EEPROM Write Protection States via J1[1]

EEPROM WRITE PROTECTION STATE	J1
Write access allowed	**closed**
Write protected	open

1: *Defaults are in **bold blue** text*

8 RS-232

8.1 RS232 Transceiver (U12)

One high-speed RS-232 transceiver supporting 460kbps data rates populates the phyCORE-i.MX35 at U12. This device converts the signal levels for:

- RXD/TXD/RTS/CTS (UART2)

The RS-232 interface enables connection of the module to a COM port on a host-PC. In this instance the RxD line of the transceiver is connected to the TxD line of the COM port; while the TxD line of the transceiver is connected to the RxD line of the COM port. The ground potential of the phyCORE-i.MX35 circuitry needs to be connected to the applicable ground pin on the COM port as well.

The phyCORE-i.MX35 does not convert the remaining available UART (UART1) provided by the i.MX35x MCU to RS-232 levels. The TTL level signals are made available at the phyCORE-connector X1 (*see Table 1*). External RS-232 transceivers must be supplied by the user if the additional UART requires RS-232 levels.

The maximum baud rate of UART2 is limited to 460,800 bps when used with the on-board MAX3380 RS-232 transceiver.

8.1.1 UART2 Routing (RN4)

RN4 is used to route the signals of UART2 serial interface through the RS-232 transceiver or around the RS-232 transceiver when populated. When RN4 is not populated UART2_RXD_TTL, UART2_TXD_TTL, UART2_RTS_TTL and UART2_CTS_TTL are routed through the RS-232 transceiver U12 and come out as X_UART2_RXD, X_UART2_TXD, x_UART2_RTS and x_UART2_CTS at the phyCORE-connector pins X1 pin 22D, X1 pin 23D, X1 pin 25D, X1 pin 26D. If U12 does not populate the module, RN4 is populated to route the TTL level signals to these same pins.

The standard phyCORE-i.MX35 module will have U12 populated, thereby routing the RS-232 level signals to the phyCORE-connector. Be sure the phyCORE-i.MX35 configuration you are working with before interfacing these signals outside of the module as incorrect voltage levels will likely cause damage to on-board and off-board components.

The following configurations are possible:

Table 11: RN4 UART2 Signal Routing[1]

SIGNAL CONFIGURATION	RN4
X_UART2_RXD, X_UART2_TXD, X_UART2_ RTS, X_ UART2_CTS as RS-232 level signals at X1 pin 22D, X1 pin 23D, X1 pin 25D and X1 pin 26D	**not populated**
X_UART2_RXD, X_UART2_TXD, X_UART2_ RTS, X_ UART2_CTS as TTL level signals at X1 pin 22D, X1 pin 23D, X1 pin 25D and X1 pin 26D	populated

1 : *Defaults are in **bold blue** text*

9 USB

The i.MX35x microcontroller has one USB 2.0 Host interface and one USB 2.0 OTG interface both with integrated USB-Phys.

9.1 USB-OTG

With the phyCORE-i.MX35 USB-OTG is realized with the internal high-speed USB-OTG-Phy of the i.MX35x. This Phy supports data rates up to 480Mbps. An external USB Standard-A (for USB host), USB Standard-B (for USB device), or USB mini-AB (for USB OTG) connector and a 5 V VBUS power supply is all that is needed to interface the phyCORE-i.MX35 USB OTG functionality. The applicable interface signals (D+/D-/VBUS/ID) can be found in the phyCORE-connector pin-out *Table 1.*
Also the whole USB-OTG interface is connected to the phyCORE-connector so that there is the possibility to use different USB-Phys.

9.2 USB-Host

With the phycore-i.MX35 USB-Host is realized with the internal full-speed USB-Host-Phy of the i.MX35x microcontroller. This Phy supports data rates up to 12Mbps. An external USB Standard-A (for USB host), USB Standard-B (for USB device), or USB mini-AB (for USB OTG) connector is all that is needed to interface the phyCORE-i.MX35 USB Host functionality. The applicable interface signals (D+/D-) can be found in the phyCORE-connector pin-out *Table 1.*

10 Ethernet Controller / Ethernet-Phy (U5)

Connection of the phyCORE-i.MX35 to the world wide web (WWW) or a local area network (LAN) is possible with the internal 10/100 Mbps Fast Ethernet controller. With this Ethernet controller an external transceiver interface and transceiver function are required to complete the interface to the media. Therefor the i.MX35x uses an Ethernet-Phy (U5).

The Ethernet-Phy provides MII/RMII/SMII interfaces to transmit and receive data. In addition the PHY also supports HP Auto-MDIX technology, eliminating the need for the consideration of a direct connect LAN cable, or a cross-over patch cable. It detects the TX and RX pins of the connected device and automatically configures the PHY TX and RX pins accordingly. The Ethernet-Phy also features LinkMD cable diagnostics, which allows detection of common cabling plant problems such as open and short circuits.

The physical memory area for the Fast Ethernet controller is defined in *Table 12*.

Table 12: Fast Ethernet Controller Memory Map

ADDRESS	FUNCTION
0x5003_8 + 0x000-1FF	Control/Status Registers
0x5003_8 + 0x200-3FF	MIB Block Counters

Connection to an external Ethernet transformer should be done using very short signal traces. The TPI+/TPI- and TPO+/TPO- signals should be routed as 100 Ohm differential pairs. The same applies for the signal lines after the transformer circuit. The carrier board layout should avoid any other signal lines crossing the Ethernet signals.

Caution!
Please note the datasheet of the Ethernet-Phy when creating the Ethernet transformer circuitry.

11 CAN

The i.MX35x provides two CAN interfaces (protocol specification version 2.0B). Its programmable bit rate can be up to 1Mbyte/sec. All available signals (X_CAN1_RX, X_CAN1_TX, X_CAN2_RX, X_CAN2_TX) are connected to the molex connector.

To use the CAN functionality of the i.MX35x you need an additional CAN transceiver and a CAN connector for each of the two CAN interfaces which are provided by the phyCORE-i.MX35 module.

Table 13: CAN Controller Memory Map

Address	Funktion
0x53FE_4000 - 0x53FE_7FFF	Controller Area Network (CAN)-1
0x53FE_8000 - 0x53FE_BFFF	Controller Area Network (CAN)-2

For further details of the Controller Area Network of i.MX35x please refer to the IMX35 Reference Manual, chapter 24, Controller Area Network (FlexCAN).

12 JTAG Interface (X2)

The phyCORE-i.MX35 is equipped with a JTAG interface for downloading program code into the external flash, internal controller RAM or for debugging programs currently executing. The JTAG interface extends out to a 2.0 mm pitch pin header at X2 on the edge of the module PCB. *Figure 8* and *Figure 9* show the position of the debug interface (JTAG connector X2) on the phyCORE-module.

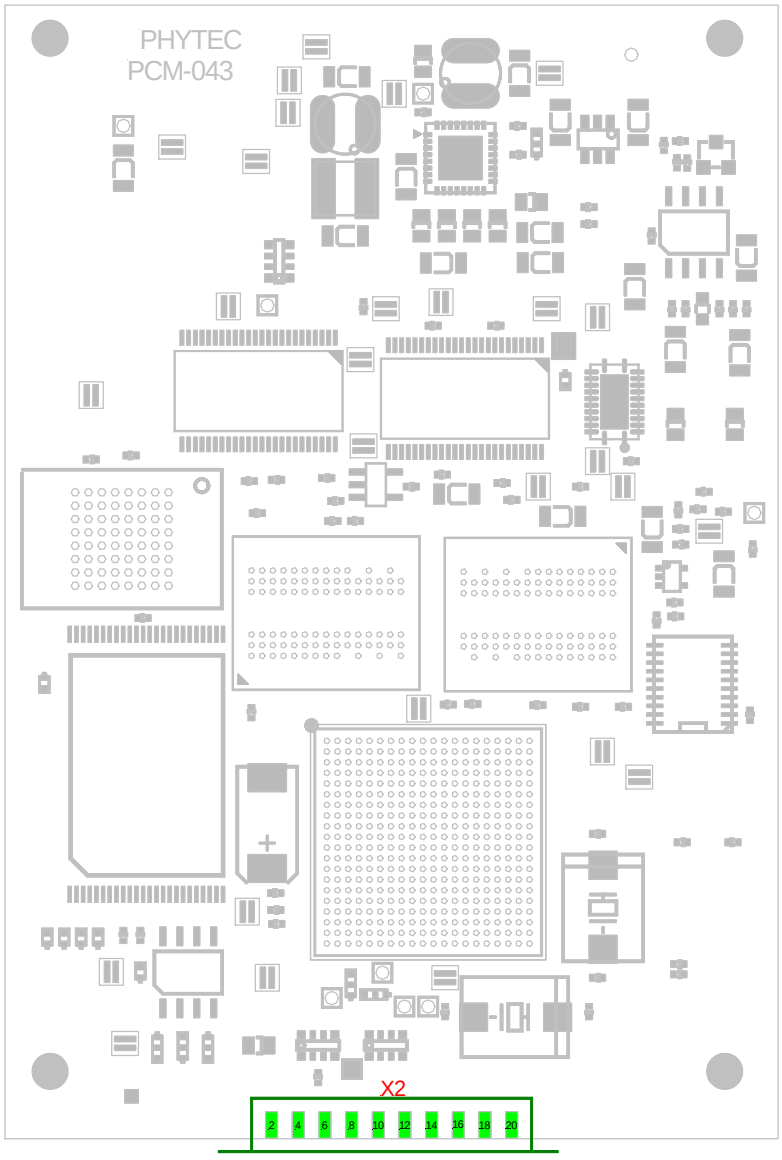

Figure 8: JTAG Interface at X2 (Top View)

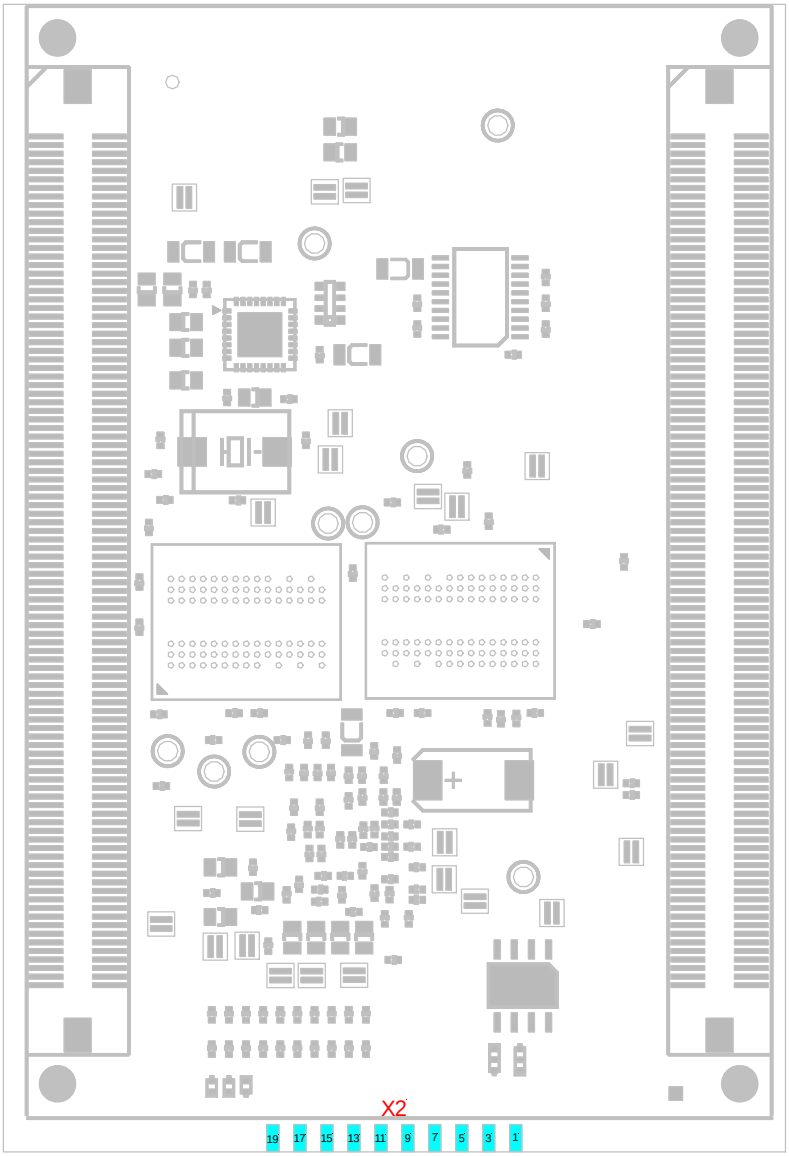

Figure 9: JTAG Interface at X2 (Bottom View)

Pin 1 of the JTAG connector X2 is on the connector side of the module. Pin 2 of the JTAG connector is on the controller side of the module.

Note:
The JTAG connector X2 only populates phyCORE-i.MX35 modules with order code PCM-043-D. JTAG connector X2 is not populated on phyCORE modules with order code PCM-043. However, all JTAG signals are also accessible at the phyCORE-connector X1 (Molex connectors). We recommend integration of a standard (2.54 mm pitch) pin header connector in the user target circuitry to allow easy program updates via the JTAG interface. *See Table 14 for details on the JTAG signal pin assignment.*

Table 14: JTAG Connector X2 Signal Assignment

SIGNAL	PIN ROW*		SIGNAL
	A	B	
VCC(VDD_3V3)	2	1	VTREF (VDD_3V3 via 100 Ohm)
GND	4	3	#X_CPU_TRST
GND	6	5	X_CPU_TDI
GND	8	7	X_CPU_TMS
GND	10	9	X_CPU_TCK
GND	12	11	X_CPU_RTCKRTCK (10k Ohm pulldown)
GND	14	13	X_CPU_TDO
GND	16	15	#X_RESET_MCU
GND	18	17	#X_CPU_DE
GND	20	19	J_DBGACK (10k Ohm pulldown)

*Note:
Row A is on the controller side of the module and row B is connector side of the module

PHYTEC offers a JTAG-Emulator adapter (order code JA-002) for connecting the phyCORE-i.MX35 to a standard emulator. The JTAG-Emulator adapter extends the signals of the module's JTAG connector to a standard ARM connector with 2.54 mm pin pitch. The JA-002 therefore functions as an adapter for connecting the module's non-ARM-compatible JTAG connector U15 to standard Emulator connectors.

13 Technical Specifications

The physical dimensions of the phyCORE-i.MX35 are represented in *Figure 10*. The module's profile is approximately ***8.6 mm*** thick, with a maximum component height of ***4.1 mm*** on the bottom (connector) side of the PCB and approximately ***3.25 mm*** on the top (microcontroller) side. The board itself is approximately ***1.25 mm*** thick.

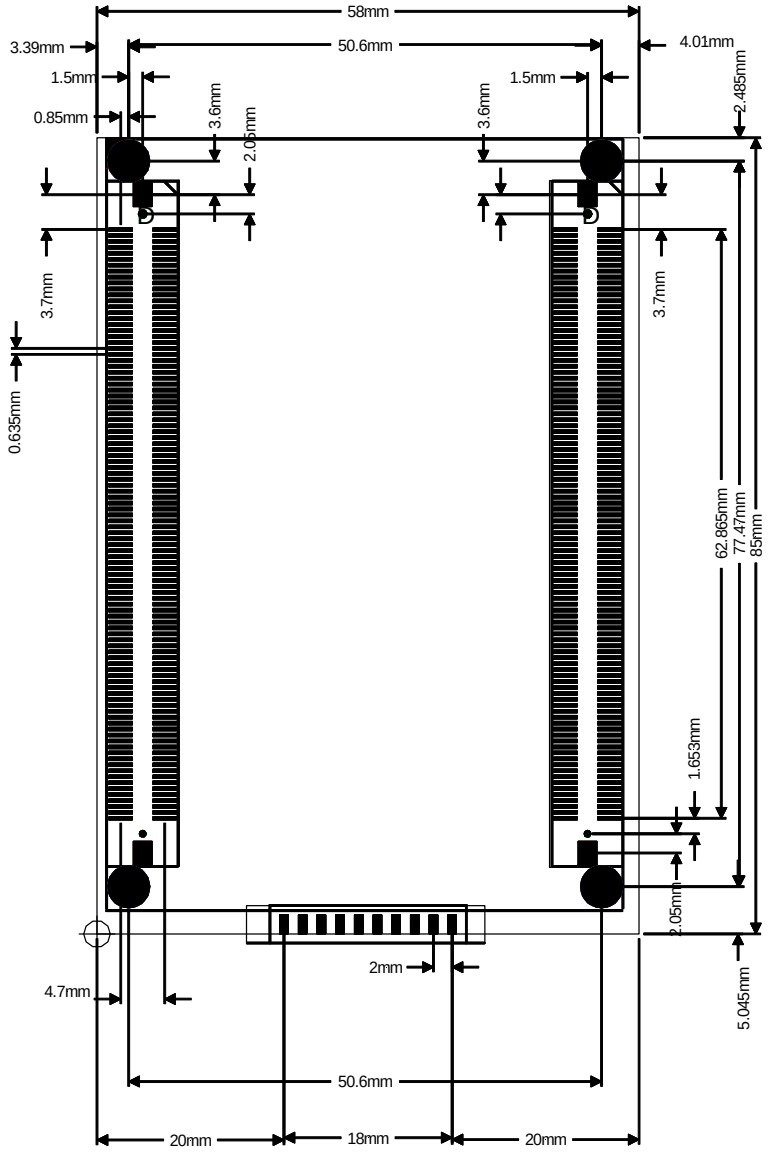

Figure 10: Physical Dimensions of phyCORE-i.MX35 Module

Additional specifications :

•	*Dimensions:*	*85 mm x 58 mm*
•	*Weight:*	*approximately 30 g with all optional components mounted on the circuit board*
•	*Storage temperature:*	*-55°C to +125°C*
•	*Operating temperature:*	*0°C to +70°C (standard)* *-40°C to +85°C (optional)*
•	*Humidity:*	*95 % r.F. not condensed*
•	*Operating voltage:*	*VIN 5 V*
•	*Power consumption:* *VIN / 600 mA max* *****	*Conditions:* ***VIN = 5 V*** *32 MByte Flash, 128 MB DDR2-RAM, 1 GB NAND-Flash, Ethernet, 532 MHz CPU frequency at 20°C*

These specifications describe the standard configuration of the phyCORE-i.MX35 as of the printing of this manual.

*		
- booting UBoot:	~235 mA (~1,175W)	(max value)
- UBoot Prompt:	~220 mA (~1,1W)	(norm. operation value)
- RAM-Test in UBoot:	~210 mA (~1,05W)	(max value)
- Linux Prompt:	~145 mA (~0,725W)	(norm. operation value)
- Ping over Ethernet:	~145 mA (~0,725W)	(max value)
- incl. display, displaytest:	~146 mA (~0,73W)	(max value)

14 Hints for Handling the phyCORE-i.MX35

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

15 The phyCORE i.MX35 on the i.MX Carrier Board

In this chapter you will find the information about using the phyCORE-i.MX35 module with the phyCORE i.MX Carrier Board.
You will get an overview of how the phyCORE-i.MX35 module works with the phyCORE-i.MX Carrier Board, how both boards are connected together over the phyMAPPER and you will also find all settings that have to be done for a speedy and secure start-up of your i.MX35 module.

In this chapter you will only find specialized information of how the phyCORE-i.MX35 module works with the phyCORE-i.MX Carrier Board. *For further information about the Carrier Board please refer to the i.MX Carrier Board Hardware Manual.*

15.1 Concept of the phyCORE-i.MX Development Kits

Phytec decided to use one i.MX Carrier Board for different i.MX modules. Because every i.MX module has different features and therefore a different pinning it is necessary to map the signals of the modules to the right place on the Carrier Board.
For this every i.MX module comes with a phyMAPPER that is mapping the signals of the i.MX module to the i.MX Carrier Board.
An example of the concept is shown in *Figure 11* below. *For further information about the concept of the i.MX Carrier Board refer to the i.MX Carrier Board Hardware Manual.*

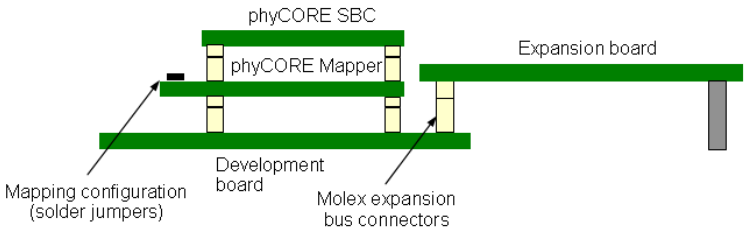

Figure 11: phyCORE-i.MX35 Carrier Board Connection Using the phyMAP-i.MX35

15.2 phyMAP-i.MX35

The phyMAP-i.MX35 is responsible for mapping the signals from the various phyCORE-i.MX modules to the phyCORE-i.MX Carrier Board. Signal differences at the connectors on the phyCORE-i.MX modules, along with signal differences between the phyCORE-i.MX module connectors and i.MX Carrier Board connector do not allow for direct connection of the phyCORE-i.MX modules into a single, standardized Carrier Board. To allow for the use of a single Carrier Board, despite the signal differences, the phyMAP-i.MX35 board serves as the gateway to properly map signals from the i.MX Carrier Board Molex connectors to the various phyCORE-i.MX module connectors.

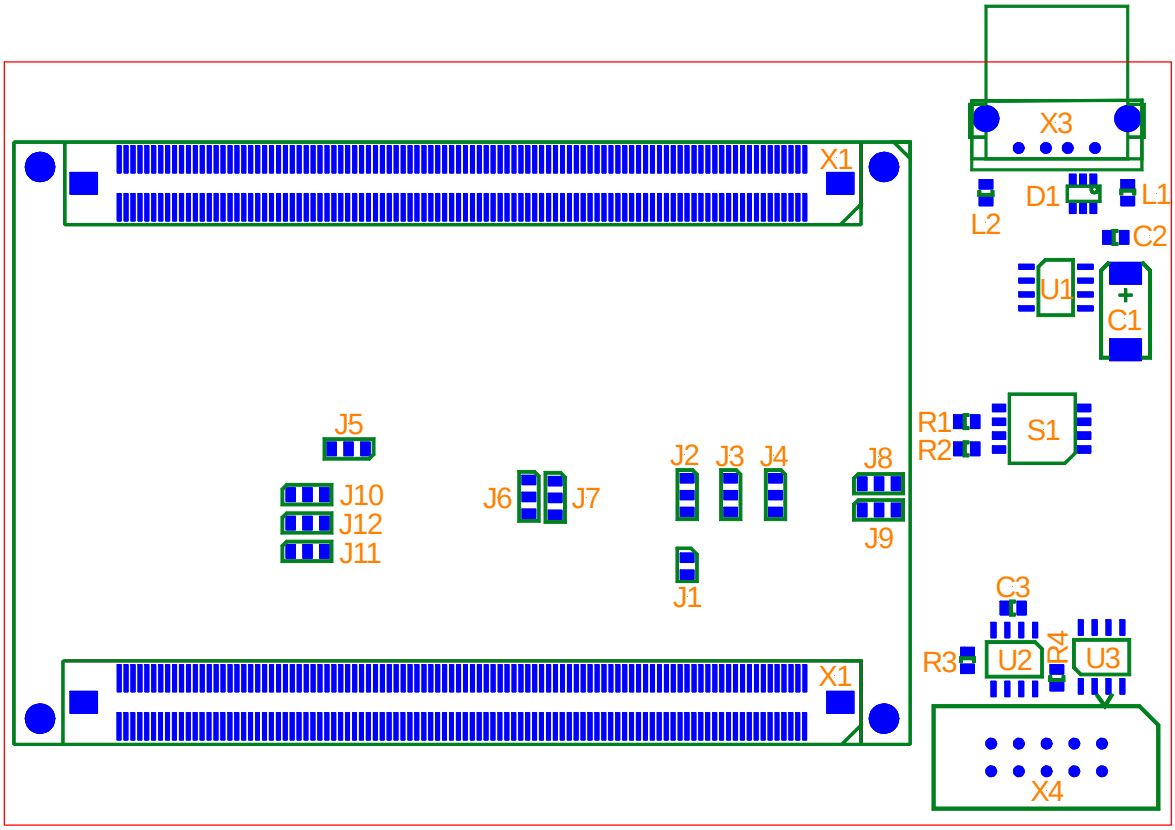

Figure 12: phyMAP-i.MX35 Top View

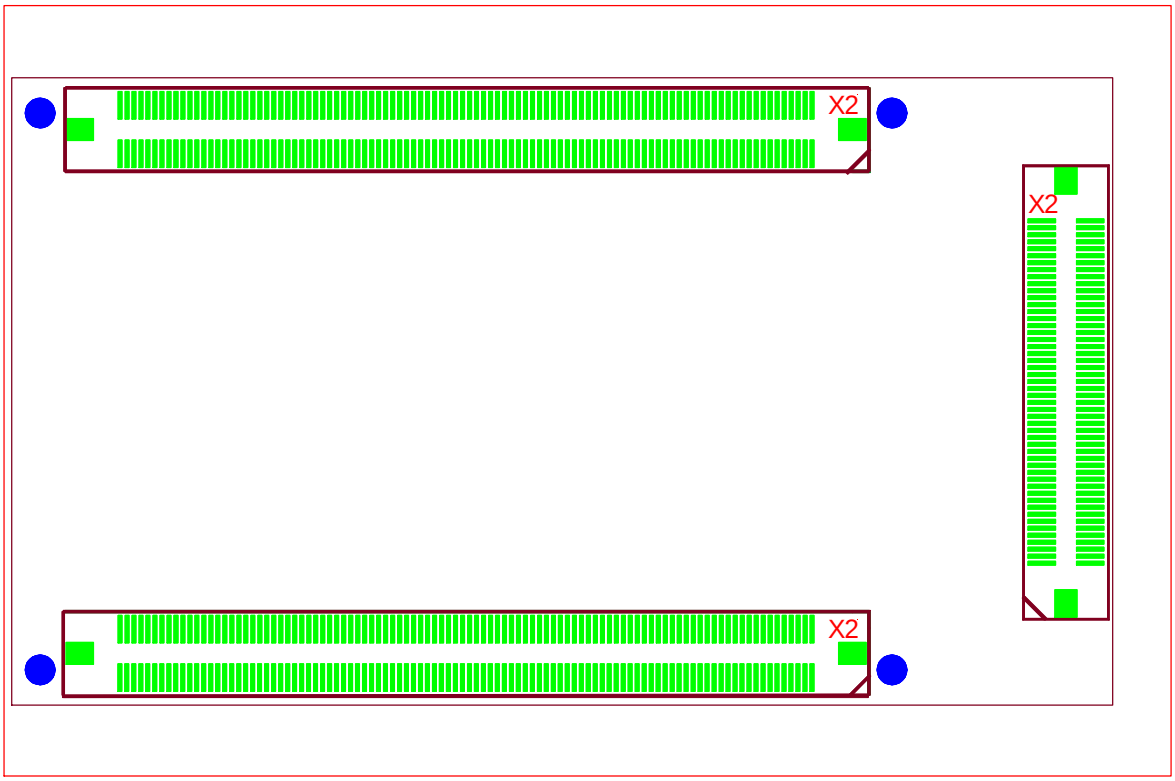

Figure 13: phyMAP-i.MX35 Bottom View

15.2.1 phyMAP-i.MX35 Jumper Settings

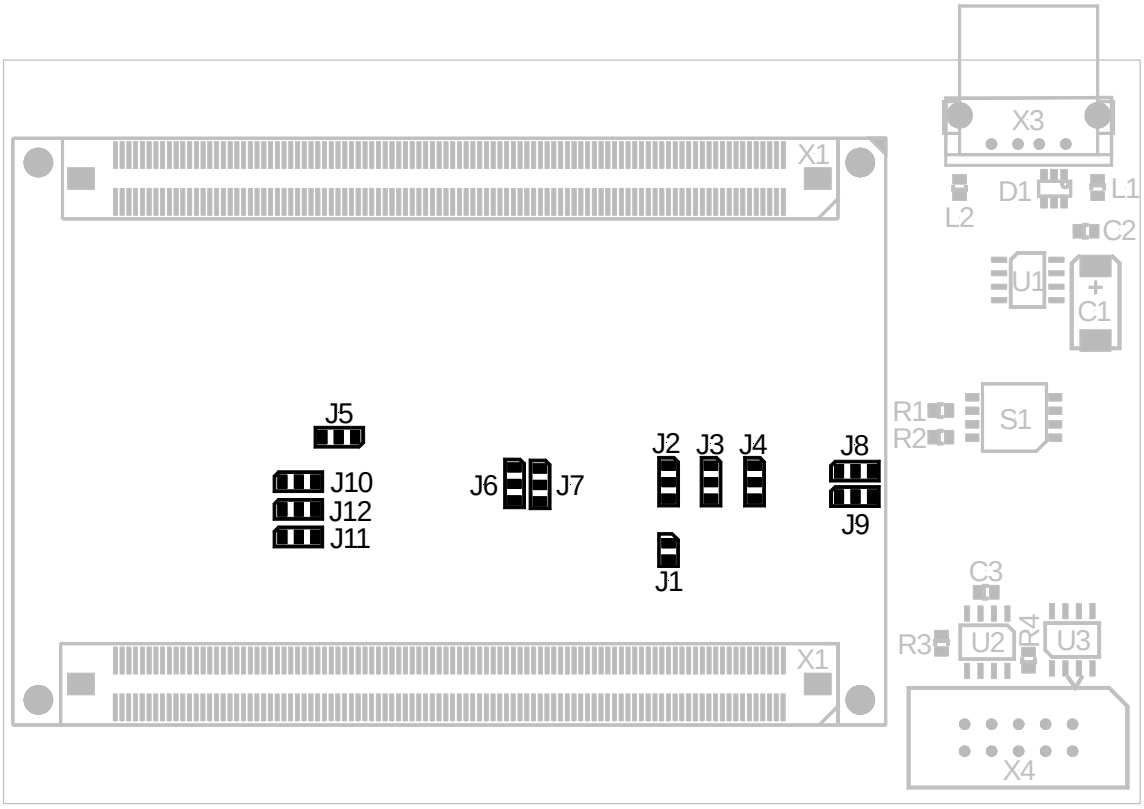

Figure 14: Jumper Location on PMA-005

There are 12 solder jumpers (0805) available on the phyMAP-i.MX35 Mapper. They are used to set different functions partially in relation with the i.MX Carrier Board.
An individual description of the jumpers and a list of all jumper settings you will find subsequent.

J1 With jumper J1 the two FETs Q17 and Q18 on the i.MX Carrier Board can be enabled or disabled. They allow a current flow to charge a battery connected to X21 on the Carrier Board. If J1 is opened there is no current flow. If J1 is closed the FETs and also the battery charge path are active.

J2 If this jumper is set to 1+2 the FETs Q13 and Q14 of the i.MX Carrier Board are disabled. In this case there is no power supply connection from the wall charger or POE to VIN. If J2 is set to 2+3 the power supply is connected to VIN. It is necessary to set J2 to 1+2 if you want to supply your board with a battery.

J3 If this jumper is set to 1+2 the FETs Q15 and Q16 of the i.MX Carrier Board are disabled. In this case there is no power supply connection from the battery connector X21 to VIN. If J3 is set to 2+3 the battery supply is connected to VIN. It is necessary to set J2 to 1+2 if you want to supply your board via the wall charger or POE.

J4 With this jumper you can select the backup power supply of the module. If it is set to 1+2 the backup power supply device is the goldcap C161 of the Carrier Board. If J4 is set to 2+3 the backup power is provided by a Li-Cell at connector X20 of the Carrier Board.

J5 Selects whether the One-Wire or the PMIC-Ready function of the i.MX35 is used. Setting 1+2 connects the One-Wire function to the baseboard connector, setting 2+3 connects the PMIC-Ready function to the baseboard.

J6 This jumper selects where the signal X_USBH2_OC of the i.MX35 is connected to. If the USB-Host interface of the phyMAP-i.MX35 mapper is used this jumper is set to 2+3. If the USB-Host interface of the i.MX Carrier Board is used the jumper is set to 1+2.

J7 This jumper selects where the signal X_USBH2_PWR of the i.MX35 is connected to. If the USB-Host interface of the phyMAP-i.MX35 mapper is used this jumper is set to 2+3. If the USB-Host interface of the i.MX Carrier Board is used the jumper is set to 1+2.

J8 This jumper selects where the signal X_USBPHY2_DM of the i.MX35 is connected to. If the USB-Host interface of the phyMAP-i.MX35 mapper is used this jumper is set to 2+3. If the USB-Host interface of the i.MX Carrier Board is used the jumper is set to 1+2.

J9 This jumper selects where the signal X_USBPHY2_DP of the i.MX35 is connected to. If the USB-Host interface of the phyMAP-i.MX35 mapper is used this jumper is set to 2+3. If the USB-Host interface of the i.MX Carrier Board is used the jumper is set to 1+2.

J10 Jumper J10 selects whether the signal X_SD2_DATA3 is used as data3 signal of SD2 interface on the i.MX Carrier Board or if the multiplexed CAN1_TX signal is used for the additional CAN interface on the i.MX35 mapper board. If the jumper is set to 1+2 the SD2 signal is connected to the baseboard. If the jumper is set to 2+3 the CAN signal is used with the CAN interface on the mapper.

J11 Jumper J11 selects whether the signal X_SD2_DATA2 is used as data2 signal of SD2 interface on the i.MX Carrier Board or if the multiplexed CAN1_RX signal is used for the additional CAN interface on the i.MX35 mapper board. If the jumper is set to 1+2 the SD2 signal is connected to the baseboard. If the jumper is set to 2+3 the CAN signal is used with the CAN interface on the mapper.

J12 Jumper J12 selects whether the signal X_SD2_DATA1 is used as data1 signal of SD2 interface on the i.MX Carrier Board or if the multiplexed GPIO is used for the additional CAN interface on the i.MX35 mapper board to enable or disable the CAN function. If the jumper is set to 1+2 the SD2 signal is connected to the baseboard. If the jumper is set to 2+3 the GPIO signal is used with the CAN interface on the mapper.

Table 15: Jumper Settings of PMA-005

JUMPER	SETTING	DESCRIPTION
J1	open closed	Battery charger path on PCM-970 not active Battery charger path on PCM-970 active
J2	1+2 2+3	FETs Q13, Q14 on PCM-970 disabled FETs Q13, Q14 on PCM-970 enabled
J3	1+2 2+3	FETs Q15, Q16 on PCM-970 disabled FETs Q15, Q16 on PCM-970 enabled
J4	1+2 2+3	x_BKUP_SUPPLY supplied by X_VBAT x_BKUP_SUPPLY supplied by X_LICELL
J5	1+2 2+3	X_OWIRE connected to X_1WIRE X_OWIRE connected to X_PMIC_RDY
J6	1+2 2+3	USB Host on Mapper is not used USB Host on Mapper is used
J7	1+2 2+3	USB Host on Mapper is not used USB Host on Mapper is used
J8	1+2 2+3	USB Host on Mapper is not used USB Host on Mapper is used
J9	1+2 2+3	USB Host on Mapper is not used USB Host on Mapper is used
J10	1+2 2+3	CAN on Mapper is not used CAN on Mapper is used
J11	1+2 2+3	CAN on Mapper is not used CAN on Mapper is used
J12	1+2 2+3	X_SD2_DATA1 is mapped to PCM-970 X_SD2_DATA1 is used as GPIO for CAN enable

15.2.2 phyMAP-i.MX35 Signal Mapping

In the following table you will find all signals of the phyCORE-i.MX35 module (PCM-043) connected through the phyMAP-i.MX35 mapper (PMA-005) to the phyCORE-i.MX Carrier Board (PCM-970).
Take care that there are some signals connected to jumpers on the phyMAP-i.MX35 mapper. With this signals it depends on the individual jumper setting where this signals are connected to. This signals are in **bold** text.

Table 16: PMA-005 Mapping List

Signal Name on PMA-005 Mapper	X1 Pin #	mapped to	X2 Pin #	Signal Name on i.MX Carrier Board
A0_3V3	35B	<->	27B	x_A0
A1_3V3	36B	<->	28A	x_A1
A2_3V3	36A	<->	28B	x_A2
A3_3V3	37B	<->	29A	x_A3
A4_3V3	38A	<->	30A	x_A4
A5_3V3	39A	<->	30B	x_A5
A6_3V3	38B	<->	31A	x_A6
A7_3V3	40A	<->	31B	x_A7
A8_3V3	40B	<->	32B	x_A8
A9_3V3	41B	<->	33A	x_A9
A10_3V3	41A	<->	33B	x_A10
A11_3V3	42B	<->	34A	x_A11
A12_3V3	43A	<->	35A	x_A12
A13_3V3	44A	<->	35B	x_A13
A14_3V3	43B	<->	36A	x_A14
A15_3V3	45A	<->	36B	x_A15
A16_3V3	45B	<->	37B	x_A16
A17_3V3	46B	<->	38A	x_A17
A18_3V3	46A	<->	38B	x_A18
A19_3V3	47B	<->	39A	x_A19
A20_3V3	48A	<->	40A	x_A20
A21_3V3	49A	<->	40B	x_A21
A22_3V3	48B	<->	41A	x_A22
A23_3V3	50A	<->	41B	x_A23
A24_3V3	50B	<->	42B	x_A24
A25_3V3	51B	<->	43A	x_A25
BCLK_3V3	35A	<->	4E	x_EXP005

D0	51A	<->	43B	x_D0
D1	52B	<->	44A	x_D1
D2	53A	<->	45A	x_D2
D3	54A	<->	45B	x_D3
D4	53B	<->	46A	x_D4
D5	55A	<->	46B	x_D5
D6	55B	<->	47B	x_D6
D7	56B	<->	48A	x_D7
D8	56A	<->	48B	x_D8
D9	57B	<->	49A	x_D9
D10	58A	<->	50A	x_D10
D11	59A	<->	50B	x_D11
D12	58B	<->	51A	x_D12
D13	60A	<->	51B	x_D13
D14	60B	<->	52B	x_D14
D15	61B	<->	53B	x_D15
EB0_3V3	31B	<->	55B	x_/EB0
EB1_3V3	31A	<->	56B	x_/EB1
ECB_WAIT_3V3	33B	<->	5E	x_EXP006
LBA_3V3	34A	<->	54A	x_LBA
VDD_ALIVE	1B	<->	44E	x_EXP069
VDD_1V8	61A	<->	43E	x_EXP067
X_BKUP_SUPPLY	6C	<->	6C	x_VBAT
X_BOOT0	98C	<->	53C	x_BOOT_MODE0
X_BOOT1	99C	<->	53D	x_BOOT_MODE1
X_BOOT2	98D	<->	100B, 36F	x_switch, x_EXP057
X_BOOT3	96D	<->	37F	x_EXP058
X_BOOT4	97D	<->	38F	x_EXP060
X_CAN2_RX	31D	<->	38D	x_CAN_RXD
X_CAN2_TX	30D	<->	37D	x_CAN_TXD
X_CAPTURE	27D	<->	50F	x_EXP079
X_CLKO	100B	<->	47F	x_EXP074
X_COMPARE	28D	<->	50E	x_EXP078
X_CPU_RTCK	40C	<->	42D	x_CPU_RTCK
X_CPU_TCK	38D	<->	40D	x_CPU_TCK
X_CPU_TDI	40D	<->	39C	x_CPU_TDI
X_CPU_TDO	41D	<->	40C	x_CPU_TDO
X_CPU_TMS	42D	<->	41C	x_CPU_TMS

X_CSI_D6	78A	<->	73A	x_CSI_D0
X_CSI_D7	78B	<->	74A	x_CSI_D1
X_CSI_D8	79A	<->	75A	x_CSI_D2
X_CSI_D9	80A	<->	75B	x_CSI_D3
X_CSI_D10	80B	<->	76A	x_CSI_D4
X_CSI_D11	81A	<->	76B	x_CSI_D5
X_CSI_D12	81B	<->	77B	x_CSI_D6
X_CSI_D13	82B	<->	78A	x_CSI_D7
X_CSI_D14	83A	<->	78B	x_CSI_D8
X_CSI_D15	83B	<->	79A	x_CSI_D9
X_CSI_HSYNC	85B	<->	73B	x_CSI_HSYNC
X_CSI_MCLK	84A	<->	69A	x_CSI_MCLK
X_CSI_PIXCLK	86A	<->	71B	x_CSI_PCLK
X_CSI_VSYNC	85A	<->	72B	x_CSI_VSYNC
X_CSPI1_MISO	87D	<->	25E	x_EXP038
X_CSPI1_MOSI	86D	<->	24E	x_EXP037
X_CSPI1_SCLK	86C	<->	23E	x_EXP035
X_CSPI1_SPI_RDY	89C	<->	27F	x_EXP042
X_CSPI1_SS0	88C	<->	26F	x_EXP041
X_CSPI1_SS1	88D	<->	26E	x_EXP040
X_CSPI2_MISO	90D	<->	96B	x_MISO
X_CSPI2_MOSI	90C	<->	95B	x_MOSI
X_CSPI2_SCLK	91C	<->	97B	x_SPICLK
X_CSPI2_SPI_RDY	91D	<->	28F	x_EXP044
X_CSPI2_SS0	92D	<->	98B	x_CE
X_EN_LDO1_2	18D	<->	43F	x_EXP068
X_EN_VDD_1V8	16D	<->	41F	x_EXP065
X_EN_VDD_1V375	17D	<->	42F	x_EXP066
X_EN_VDD_3V3	15D	<->	40F	x_EXP063
X_ETH_LINK	33C	<->	32D	x_ETH_/LED1
X_ETH_RX+	35D	<->	30C	x_ETH_TPI+
X_ETH_RX-	35C	<->	31C	x_ETH_TPI-
X_ETH_SPEED	34C	<->	33D	x_ETH_/LED2
X_ETH_TX+	36D	<->	30D	x_ETH_TPO+
X_ETH_TX-	36C	<->	31D	x_ETH_TPO-
X_FEC_COL	76B	<->	16E	x_EXP024
X_FEC_CRS	73B	<->	15E	x_EXP022
X_FEC_MDC	73A	<->	15F	x_EXP023

X_FEC_MDIO	72B	<->	16F	x_EXP025
X_FEC_RDATA0	75A	<->	8E	x_EXP011
X_FEC_RDATA1	70B	<->	9E	x_EXP013
X_FEC_RDATA2	71A	<->	10E	x_EXP014
X_FEC_RDATA3	71B	<->	11E	x_EXP016
X_FEC_RX_CLK	76A	<->	6E	x_EXP008
X_FEC_RX_DV	75B	<->	13E	x_EXP019
X_FEC_RX_ERR	70A	<->	14E	x_EXP021
X_FEC_TDATA0	86B	<->	7F	x_EXP010
X_FEC_TDATA1	87B	<->	8F	x_EXP012
X_FEC_TDATA2	88B	<->	10F	x_EXP015
X_FEC_TDATA3	69A	<->	11F	x_EXP017
X_FEC_TX_CLK	74A	<->	6F	x_EXP009
X_FEC_TX_EN	89A	<->	12F	x_EXP018
X_FEC_TX_ERR	77B	<->	13F	x_EXP020
X_FSR	48C	<->	73D	x_EXP089
X_FST	44C	<->	74C	x_EXP090
X_FUSE_VDD	7D	<->	6D	x_iMX_FUSE
X_GPIO2_6	96A	<->	58C, 76D	X_LED, x_EXP094
X_GPIO2_7	98A, (38C)	<->	75D	x_EXP092
X_GPIO2_23	99A	<->	95A, 77D	x_SD_W, x_EXP095
X_GPIO2_24	100A	<->	94A, 78D	x_SD_D, x_EXP097
X_HCKT	45C	<->	75C	x_EXP091
X_I2C1_CLK	85D	<->	39E	x_EXP061
X_I2C1_DAT	85C	<->	40E	x_EXP062
X_I2C3_SCL	83C	<->	99A	x_I2C_SCL
X_I2C3_SDA	84C	<->	100A	x_I2C_SDA
X_JTAG_MODE	43D	<->	43C	x_CPU_SJC_MOD
X_KEY_COL0	90A	<->	48D	x_KEY_COL0
X_KEY_COL1	91A	<->	49C	x_KEY_COL1
X_KEY_COL2	93A	<->	50C	x_KEY_COL2
X_KEY_COL3	94A	<->	50D	x_KEY_COL3
X_KEY_ROW0	90B	<->	45C	x_KEY_ROW0
X_KEY_ROW1	91B	<->	45D	x_KEY_ROW1
X_KEY_ROW2	92B	<->	46C	x_KEY_ROW2
X_KEY_ROW3	93B	<->	46D	x_KEY_ROW3
X_LCD_CLS	8B	<->	8B	x_LC_D3_CLS
X_LCD_CONTRAST	7B	<->	7B	x_LC_CONTRAST

X_LCD_DRDY	10A	<->	10A	x_LC_DRDY0
X_LCD_FPSHIFT	10B	<->	10B	x_LC_BCLK
X_LCD_HSYNC	5B	<->	11A	x_LC_FPLINE
X_LCD_LD0	13A	<->	13A	x_LC_D0
X_LCD_LD1	13B	<->	13B	x_LC_D1
X_LCD_LD2	14A	<->	14A	x_LC_D2
X_LCD_LD3	15A	<->	15A	x_LC_D3
X_LCD_LD4	15B	<->	15B	x_LC_D4
X_LCD_LD5	16A	<->	16A	x_LC_D5
X_LCD_LD6	16B	<->	16B	x_LC_D6
X_LCD_LD7	17B	<->	17B	x_LC_D7
X_LCD_LD8	18A	<->	18A	x_LC_D8
X_LCD_LD9	18B	<->	18B	x_LC_D9
X_LCD_LD10	19A	<->	19A	x_LC_D10
X_LCD_LD11	20A	<->	20A	x_LC_D11
X_LCD_LD12	20B	<->	20B	x_LC_D12
X_LCD_LD13	21A	<->	21A	x_LC_D13
X_LCD_LD14	21B	<->	21B	x_LC_D14
X_LCD_LD15	22B	<->	22B	x_LC_D15
X_LCD_LD16	23B	<->	23B	x_LC_D16
X_LCD_LD17	23A	<->	23A	x_LC_D17
X_LCD_LD18	24A	<->	17F	x_EXP026
X_LCD_LD19	25A	<->	18F	x_EXP028
X_LCD_LD20	25B	<->	20F	x_EXP031
X_LCD_LD21	26A	<->	19E	x_EXP029
X_LCD_LD22	26B	<->	20E	x_EXP030
X_LCD_LD23	27B	<->	21F	x_EXP033
X_LCD_REV	8A	<->	8A	x_LC_D3_REV
X_LCD_SPL	9A	<->	9A	x_LC_D3_SPL
X_LCD_VSYNC	5A	<->	5B	x_LC_FPFRAME
X_MLB_CLK	45D	<->	71A, 23F	x_SNAPSHOT, x_EXP036
X_MLB_DAT	46D	<->	70A, 25F	x_TRIGGER, x_EXP039
X_MLB_SIG	47D	<->	70B, 21E	x_CSI_ENABLE, x_EXP032
X_MVDD_BKUP	13C	<->	45E	x_EXP070
X_OWIRE	3B	<->	58D	x_1Wire
X_PVCC_BKUP	14C	<->	46E	x_EXP072
X_PWMO	100D	<->	46F	x_EXP073
X_SCKR	46C	<->	76C	x_EXP093
X_SCKT	43C	<->	73C	x_EXP088
X_SCK4	23C	<->	21D	x_BITCLK

X_SD1_CLK	70D	<->	91A	x_SD1_CLK
X_SD1_CMD	68D	<->	90B	x_SD1_CMD
X_SD1_DATA0	68C	<->	91B	x_SD1_DATA0
X_SD1_DATA1	69C	<->	92B	x_SD1_DATA1
X_SD1_DATA2	70C	<->	93A	x_SD1_DATA2
X_SD1_DATA3	71C	<->	93B	x_SD1_DATA3
X_SD2_CLK	50C	<->	68C	x_EXP080
X_SD2_CMD	51C	<->	68D	x_EXP081
X_SD2_DATA0	50D	<->	69C	x_EXP082
X_SD2_DATA1	51D	<->	70C	x_EXP083
X_SD2_DATA2	52D	<->	70D	x_EXP084
X_SD2_DATA3	53D	<->	71C	x_EXP085
X_SRXD4	26C	<->	22D	x_SDATA_IN
X_STXD4	25C	<->	20D	x_SDATA_OUT
X_STXFS4	24C	<->	23D	x_SYNC
X_TOUT	8D	<->	48E	x_EXP075
X_UART1_CTS	74C	<->	61D	x_CTS_DCE1_TTL
X_UART1_DCD	76C	<->	63D	x_DCD_DCE1_TTL
X_UART1_DSR	75D	<->	63C	x_DSR_DCE1_TTL
X_UART1_DTR	76D	<->	64C	x_DTR_DCE1_TTL
X_UART1_RI	75C	<->	62D	x_RI_DCE1_TTL
X_UART1_RTS	73C	<->	60D	x_RTS_DCE1_TTL
X_UART1_RXD	73D	<->	61C	x_RXD_DCE1_TTL
X_UART1_TXD	72D	<->	60C	x_TXD_DCE1_TTL
X_UART2_CTS	26D	<->	65C	x_CTS_RS232
X_UART2_RTS	25D	<->	66C	x_RTS_RS232
X_UART2_RXD	22D	<->	65D	x_RXD_RS232
X_UART2_TXD	23D	<->	66D	x_TXD_RS232
X_USBH2_CLK	60C	<->	83A	x_USBHOST2_CLK
X_USBH2_OC	33D	<->	72D	x_EXP087
X_USBH2_PWR	32D	<->	71D	x_EXP086
X_USBOTG_CLK	59C	<->	30E	x_EXP046
X_USBOTG_DATA0	62D	<->	31F	x_EXP049
X_USBOTG_DATA1	63D	<->	31E	x_EXP048
X_USBOTG_DATA2	63C	<->	32F	x_EXP050
X_USBOTG_DATA3	65D	<->	33F	x_EXP052
X_USBOTG_DATA4	64C	<->	33E	x_EXP051
X_USBOTG_DATA5	66D	<->	35F	x_EXP055

X_USBOTG_DATA6	65C	<->	34E	x_EXP053
X_USBOTG_DATA7	67D	<->	35E	x_EXP054
X_USBOTG_DIR	61C	<->	28E	x_EXP043
X_USBOTG_NXT	61D	<->	30F	x_EXP047
X_USBOTG_OC	56D	<->	36D	x_USB_HS_FAULT
X_USBOTG_PWR	55D	<->	35D	x_USB_HS_/PSW
X_USBOTG_STP	60D	<->	29E	x_EXP045
X_USBPHY1_DM	54C	<->	34C	x_UDM
X_USBPHY1_DP	55C	<->	35C	x_UDP
X_USBPHY1_UID	56C	<->	36C	x_UID
X_USBPHY1_VBUS	53C	<->	33C	x_VBUS
X_USBPHY2_DM	58D	<->	38E	x_EXP059
X_USBPHY2_DP	57D	<->	36E	x_EXP056
X_VSTBY	2B	<->	79C	x_EXP098
#CS0_3V3	28A	<->	1E	x_EXP000
#CS1_3V3	29A	<->	1F	x_EXP001
#CS3_3V3	28B	<->	2F	x_EXP002
#CS4_3V3	30A	<->	3E	x_EXP003
#CS5_3V3	30B	<->	3F	x_EXP004
#OE_3V3	33A	<->	53A	x_/OE
#RW_3V3	32B	<->	55A	x_/WR
#X_CPU_DE	39C	<->	41D	x_CPU_/DE
#X_CPU_TRST	41C	<->	43D	x_CPU_/TRST
#X_EN_VDD_ALIVE	20D	<->	45F	x_EXP071
#X_FL_WP	62B	<->	49E	x_EXP077
#X_IRQRTC	82D	<->	48F	x_EXP076
#X_MASTER_RESET	5D	<->	5D	x_/Reset_Btn
#X_RESET_MCU	6D	<->	44C, 4D	x_/RESET_3V3

Note:
Signals in **bold** text are connected to jumpers. The mapping of this signals could differ from the mapping list. Please check the positions of the affected jumpers to find out how the signals are mapped.

15.2.3 phyMAP-i.MX35 USB-Host Interface

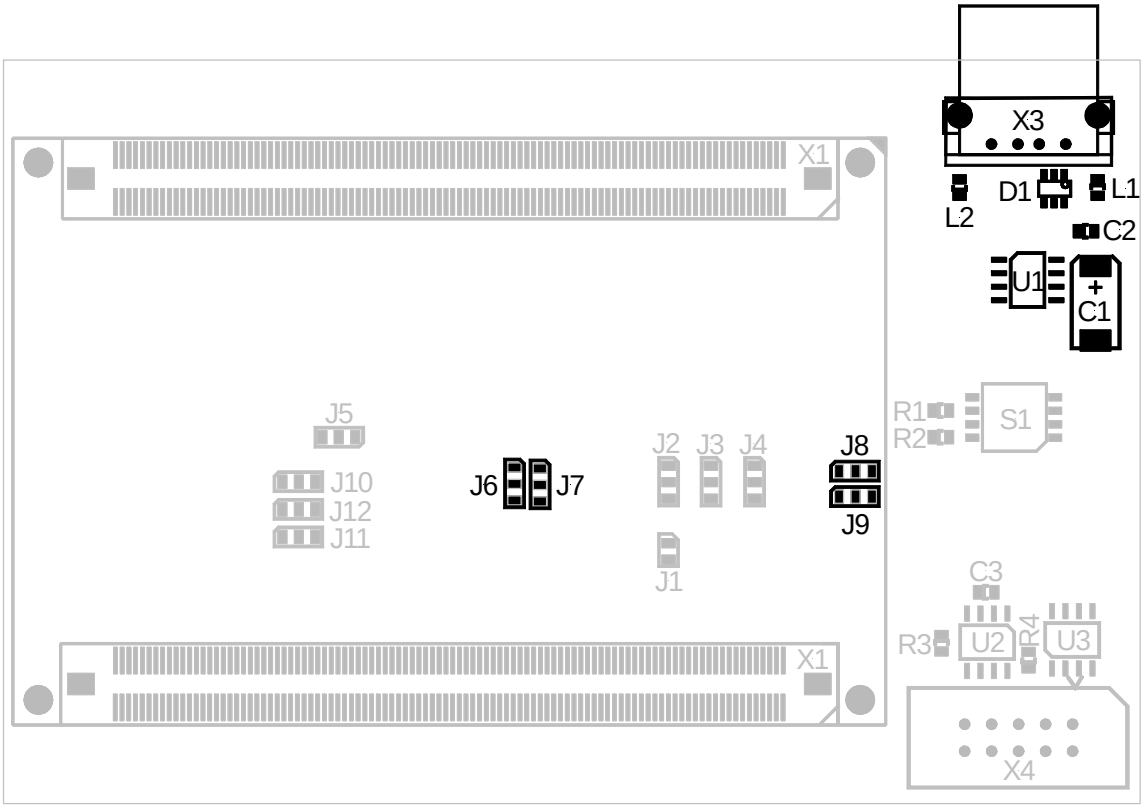

Figure 15: PMA-005 USB-Host Interface

With the phyCORE-i.MX Carrier Board PCB versions 1280.0, 1280.1 and 1280.2 there is no possibility to use the onboard USB-Host interface with the phyCORE-i.MX35 module. That's why Phytec decided to put a separate USB-Host interface on the i.MX35 mapper board. This USB-Host interface is populated when the pyhCore-i.MX35 module should be used with phyCore-i.MX Carrier Board version before 1280.3.
After a workaround with PCB version 1280.3 it is possible that the phyCORE-i.MX35 module uses the USB-Host interface of the phyCORE-i.MX Carrier Board. This functionality is given with PCB version 1280.3 or higher.

To have a decision which USB-Host interface should be used, there are solder jumpers located on the mapper board that can be set.

Table 17: PMA-005 USB-Host Jumper Settings

J6	1+2 2+3	USB Host on Carrier Board is used USB Host on Mapper is used
J7	1+2 2+3	USB Host on Carrier Board is used USB Host on Mapper is used
J8	1+2 2+3	USB Host on Carrier Board is used USB Host on Mapper is used
J9	1+2 2+3	USB Host on Carrier Board is used USB Host on Mapper is used

For further information of the separate jumpers J6 to J9 please refer to chapter 15.2.1, "phyMAP-i.MX35 Jumper Settings".

Note:
The USB-Host interface is only populated with the Upgrade (UPG) version of the phyMAP-i.MX35 mapper.

15.2.4 phyMAP-i.MX35 CAN Interface

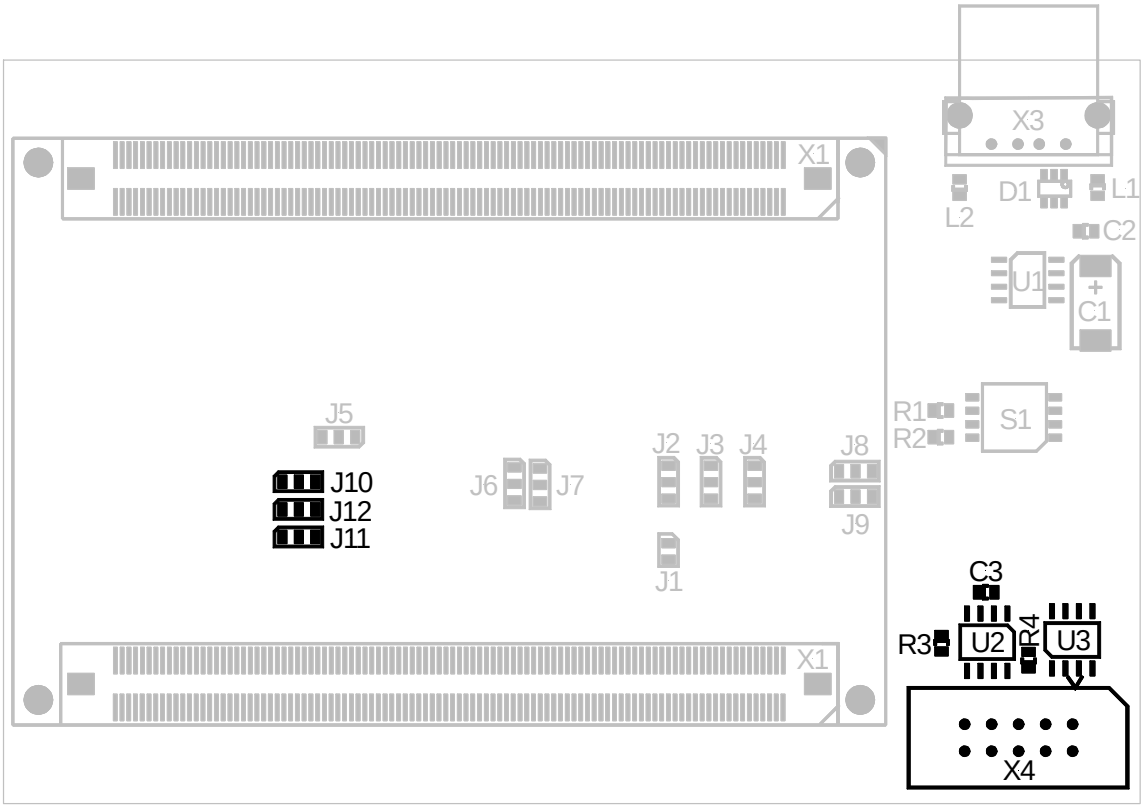

Figure 16: PMA-005 CAN Interface

The i.MX35x microcontroller provides two CAN controllers. Because there is only one CAN interface available on the i.MX Carrier Board, Phytec designed a second CAN interface on the i.MX35 mapper board. With this interface the CAN1 controller is used.
Its signals are multiplexed with the SD2-Card interface. Jumpers J10 to J12 can select whether the CAN1 interface is used or the SD2 signals are mapped to the Carrier Board.

Table 18: PMA-005 CAN Jumper Settings

J10	1+2 2+3	X_SD2_DATA3 is mapped to PCM-970 CAN1 on Mapper is used
J11	1+2 2+3	X_SD2_DATA2 is mapped to PCM-970 CAN1 on Mapper is used
J12	1+2 2+3	X_SD2_DATA1 is mapped to PCM-970 X_SD2_DATA1 is used as GPIO for CAN enable

15.2.5 phyMAP-i.MX35 Boot Select Switch

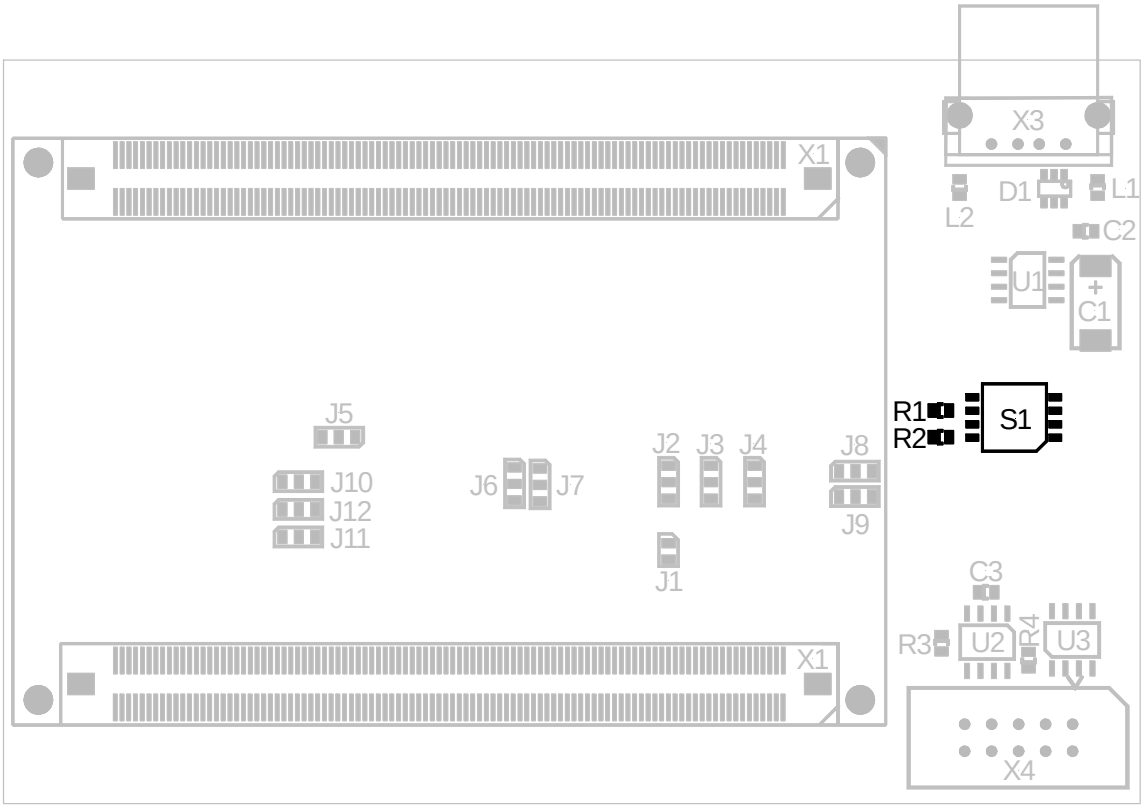

Figure 17: PMA-005 Boot Select Dip-Switch

The i.MX35x controller is able to boot from different devices as described in *chapter 6.1.2* Boot Mode Select. To have a choice from which device the controller should boot, the boot signals BOOT0 to BOOT4 are connected to two different dip-switches. These two switches are S5 on the i.MX35 Carrier Board and S1 on the phyMAP-i.MX35 mapper.

With S1 on the i.MX35 mapper board it is possible to select the status of BOOT3 and BOOT 4. F*or detailed information see Table 19 and Table 20 below.*

Table 19: x_BOOT3 Selection

STATE OF SW NUMBER 1	STATE OF SW NUMBER 2	STATE OF X_BOOT3
ON	OFF	1
OFF	ON	0

Table 20: x_BOOT4 Selection

STATE OF SW NUMBER 3	STATE OF SW NUMBER 4	STATE OF X_BOOT4
ON	OFF	1
OFF	ON	0

15.2.6 phyMAP-i.MX35 Mapper Physical Dimensions

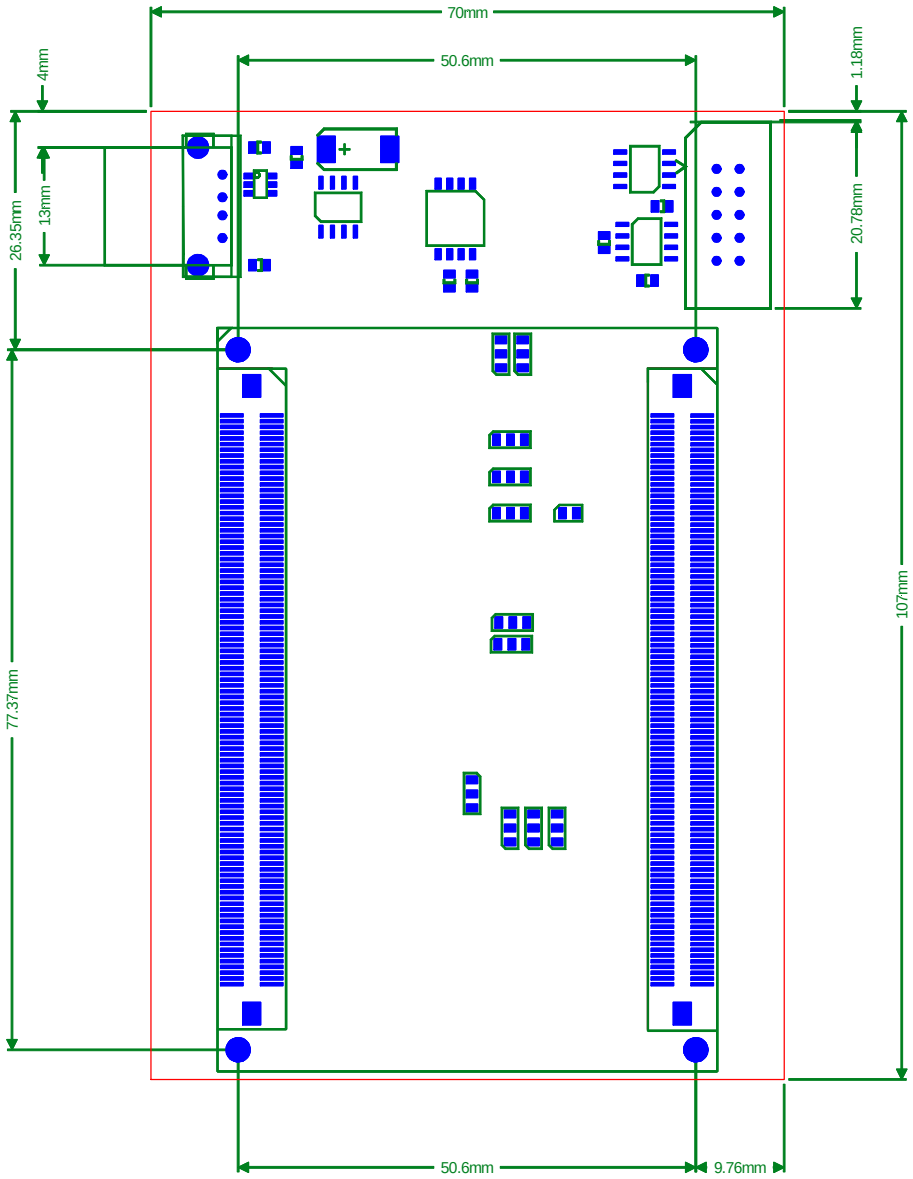

Figure 18: Physical Dimensions of phyMAP-i.MX35 Mapper

15.3 Cooperation of phyCORE-i.MX35 and phyCORE-i.MX Carrier Board

In this chapter you will find specific information and settings to adapt the i.MX Carrier Board to the i.MX35 module.
For information about the general functionality of the various interfaces of the phyCORE-i.MX Carrier Board, please refer to the phyCORE-i.MX Carrier Board Hardware Manual.

15.3.1 Power Supply

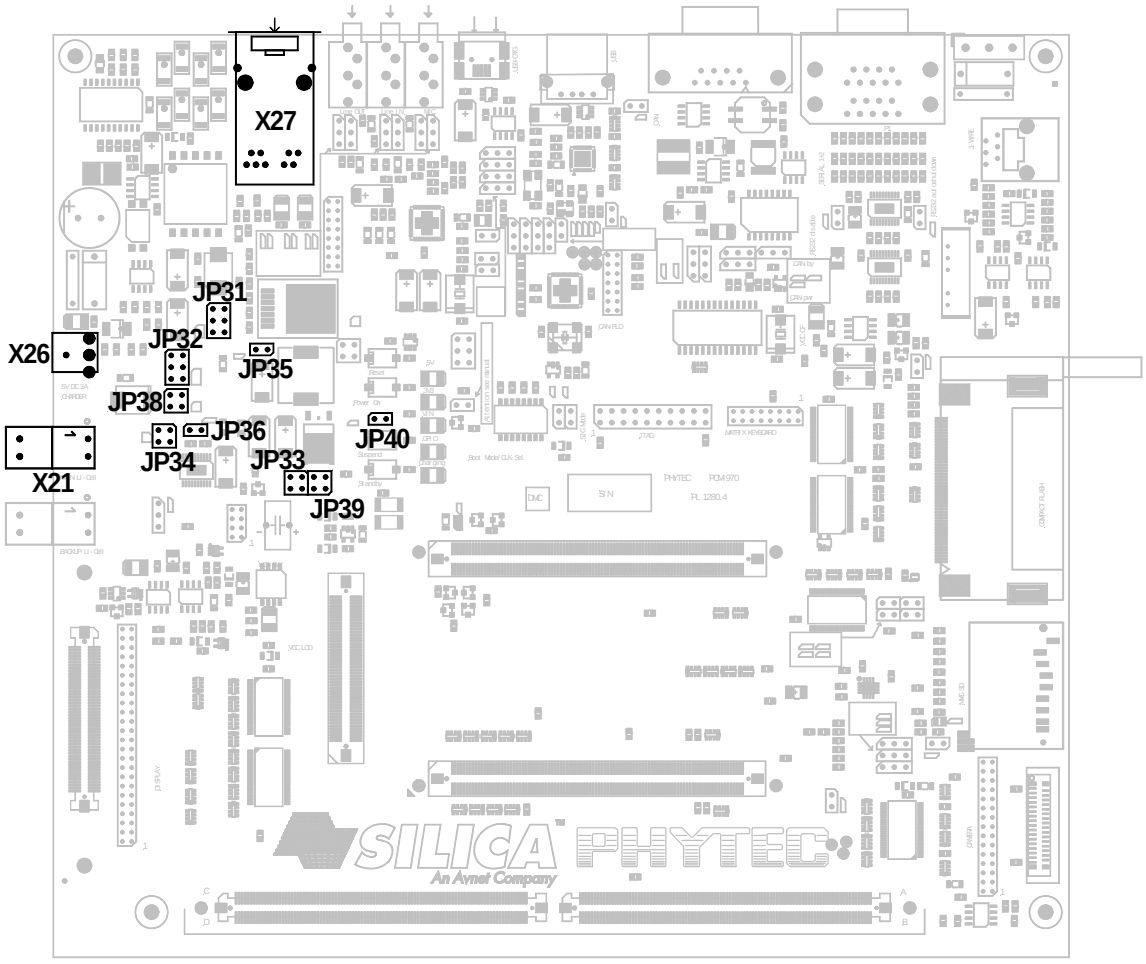

Figure 19: pyhCORE-i.MX Carrier Board and phyCORE-i.MX35 Power Supply

Subsequent you will find the different jumper settings for the three power supply modes described in the phyCORE-i.MX Carrier Board Hardware Manual.

Caution!
With the phyCORE-i.MX35 module there is no Power Management IC MC13783 provided. So compared to the phyCORE modules i.MX31 and i.MX27 there have to be different jumper settings on the phyCORE-i.MX Carrier Board. Also battery charging is not provided with the i.MX35 module.

15.3.1.1 Power Supply via Power Plug

Table 21 below shows the jumper settings to supply the phyCORE-i.MX35 module and the phyCORE-i.MX Carrier Board with a wall charger at X26 of the i.MX Carrier Board.

Table 21: Jumper settings for i.MX35 Power Supply via Power Plug[1]

JUMPER	SETTING	DESCRIPTION
JP31	1+3,2+4 **3+5,4+6**	Power source is Power Over Ethernet (POE) **Power source is 5V adapter**
JP32	1+3,2+4 **3+5,4+6**	No power switching, direct supply of VCC_3V3 **Separate supply path**
JP33	1+2,3+4 **Open,Open**	No power switching, direct supply from VCC_3V3 **Separate supply path**
JP34	1+2,3+4 **Open,Open**	No power switching, direct supply from VCC_3V3 **Separate supply path**
JP35	**Open** Closed	**VCC_5V Power Supply is enabled** VCC_5V Power Supply is disabled
JP36	Open **Closed**	VCC_3V3 Power Supply is disabled **VCC_3V3 Power Supply is enabled**
JP38	**1+2,3+4** Open,Open	**Power switching, supply from 5V adapter or POE** No power switching, direct supply from VCC_3V3
JP39	1+2,3+4 **Open,Open**	Power switching active, Battery charge path closed **No power switching, direct supply from VCC_3V3**
JP40	**Open** Closed	**No power switching active, minimum circuit** Power switching active

1: *Settings for the phyCORE-i.MX35 power supply via power plug are in **bold blue***

15.3.1.2 Power Supply via Power over Ethernet

Table 22 below shows the jumper settings to supply the phyCORE-i.MX35 module and the phyCORE-i.MX Carrier Board with Power over Ethernet at X27.

Table 22: Jumper Settings for i.MX35 Power Supply via POE[2]

JUMPER	SETTING	DESCRIPTION
JP31	**1+3,2+4**	**Power source is Power Over Ethernet (POE)**
	3+5,4+6	Power source is 5V adapter
JP32	1+3,2+4	No power switching, direct supply of VCC_3V3
	3+5,4+6	**Separate supply path**
JP33	1+2,3+4	No power switching, direct supply from VCC_3V3
	Open,Open	**Separate supply path**
JP34	1+2,3+4	No power switching, direct supply from VCC_3V3
	Open,Open	**Separate supply path**
JP35	**Open**	**VCC_5V Power Supply is enabled**
	Closed	VCC_5V Power Supply is disabled
JP36	Open	VCC_3V3 Power Supply is disabled
	Closed	**VCC_3V3 Power Supply is enabled**
JP38	**1+2,3+4**	**Power switching, supply from 5V adapter or POE**
	Open,Open	No power switching, direct supply from VCC_3V3
JP39	1+2,3+4	Power switching active, Battery charge path closed
	Open,Open	**No power switching, direct supply from VCC_3V3**
JP40	**Open**	**No power switching active, minimum circuit**
	Closed	Power switching active

2: *Settings for the phyCORE-i.MX35 power supply via Power over Ethernet are in **bold blue***

15.3.1.3 Power Supply via Battery

Table 23 below shows the jumper settings to supply the phyCORE-i.MX35 module and the phyCORE-i.MX Carrier Board with a battery at X21 of the i.MX Carrier Board.

Table 23: Jumper Settings for i.MX35 Power Supply via Battery[3]

JUMPER	SETTING	DESCRIPTION
JP31	1+3,2+4 3+5,4+6 **Open,Open**	Power source is Power Over Ethernet (POE) Power source is 5V adapter **No Power supply from wall charger or POE**
JP32	1+3,2+4 **3+5,4+6**	No power switching, direct supply of VCC_3V3 **Separate supply path**
JP33	**1+2,3+4** Open,Open	**No power switching, direct supply from VCC_3V3** Separate supply path
JP34	1+2,3+4 **Open,Open**	No power switching, direct supply from VCC_3V3 **Separate supply path**
JP35	**Open** Closed	**VCC_5V Power Supply is enabled** VCC_5V Power Supply is disabled
JP36	Open **Closed**	VCC_3V3 Power Supply is disabled **VCC_3V3 Power Supply is enabled**
JP38	1+2,3+4 **Open,Open**	Power switching, supply from 5V adapter or POE **No power switching, direct supply from VCC_3V3**
JP39	1+2,3+4 **Open,Open**	Power switching active, Battery charge path closed **No power switching, direct supply from VCC_3V3**
JP40	**Open** Closed	**No power switching active, minimum circuit** Power switching active

Note:
Instead of setting JP33 to 1+2, 2+3 there is the possibility to set solder jumper J3 of the phyMAP-i.MX35 mapper to 2+3. In this case the two FETs Q15 and Q16 of the i.MX Carrier Board will connect battery power to VIN.

3: *Settings for the phyCORE-i.MX35 power supply via battery are in **bold blue***

15.3.2 CAN Interface

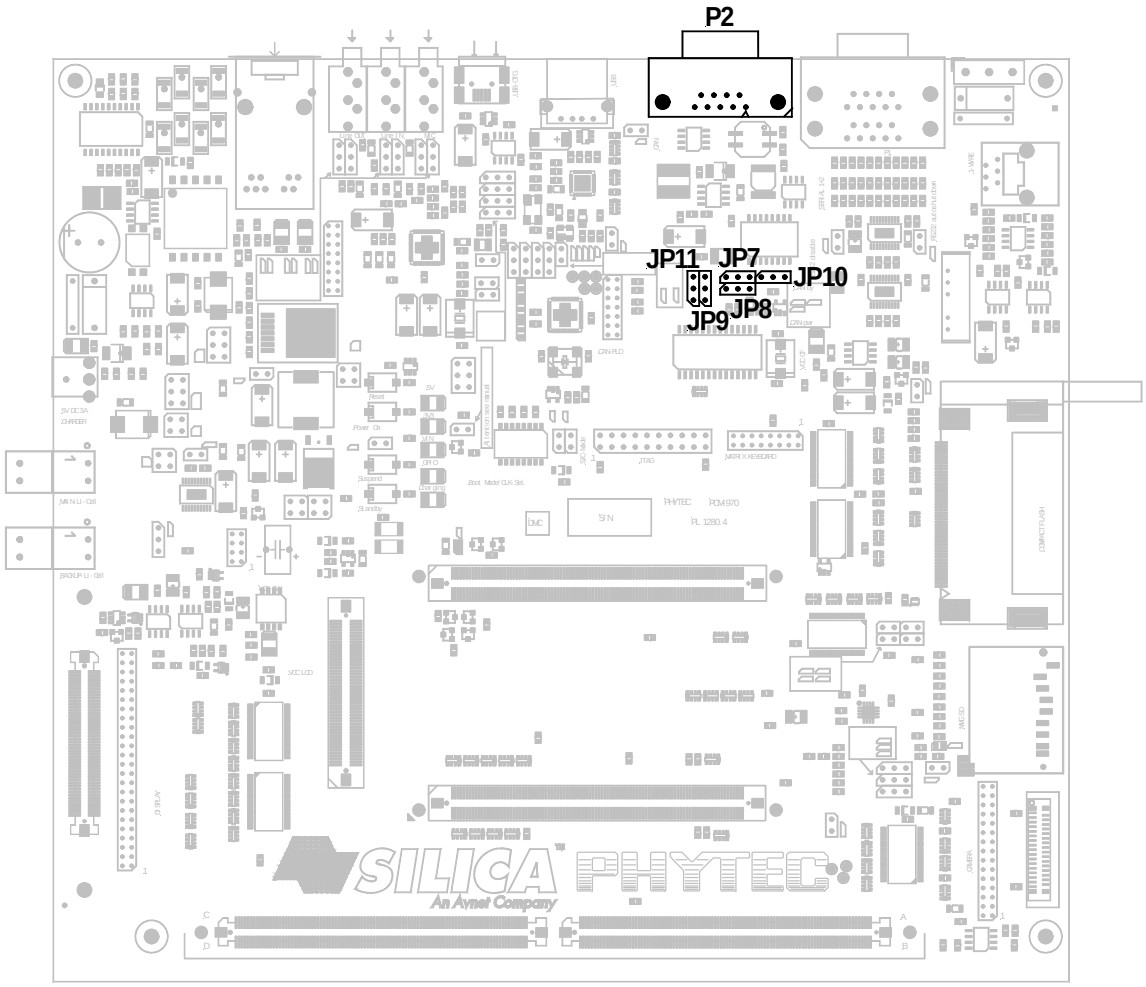

Figure 20: phyCORE-i.MX Carrier Board CAN Interface

The phyCORE-i.MX35 provides two CAN controllers. The CAN1 interface is realized on the phyMAP-i.MX35 mapper. *For further information about CAN1 please have a look at chapter 15.2.4 phyMAP-i.MX35 CAN Interface*.

The CAN2 interface is located on the i.MX Carrier Board. Because the i.MX35x controller already has an integrated CAN controller, the CAN controller populated on the Carrier Board will not be used. *Refer to Table 24 below for the jumper settings of the CAN2 interface.*

Table 24: CAN2 Interface Jumper Settings[4]

JUMPER	SETTING	DESCRIPTION
JP7	1 + 2 **2 + 3**	CANTxD signal is routed to the CAN transceiver **x_CAN_TxD signal is routed to the CAN transceiver**
JP8	**1 + 2** 2 + 3	**Digital Isolator is supplied by VCC_CAN** Digital Isolator supply is VCC_5V
JP9	**1 + 2** 2 + 3	**CANV- is connected to GND of i.MX Carrier Board** CANV- is not connected to GND of i.MX Carrier Board
JP10	1 + 2 **2 + 3**	CANRxd signal is routed to the CAN transceiver **x_CAN_RxD signal is routed to the CAN transceiver**
JP11	**1 + 2** 2 + 3	**CANV+ is connected to VCC_5V of i.MX Carrier Board** CANV+ is connected to CAN_OUT (external supply)

4: *Default settings for the phyCORE-i.MX35 CAN2 interface are in **bold blue***

15.3.3 Push Buttons and LEDs

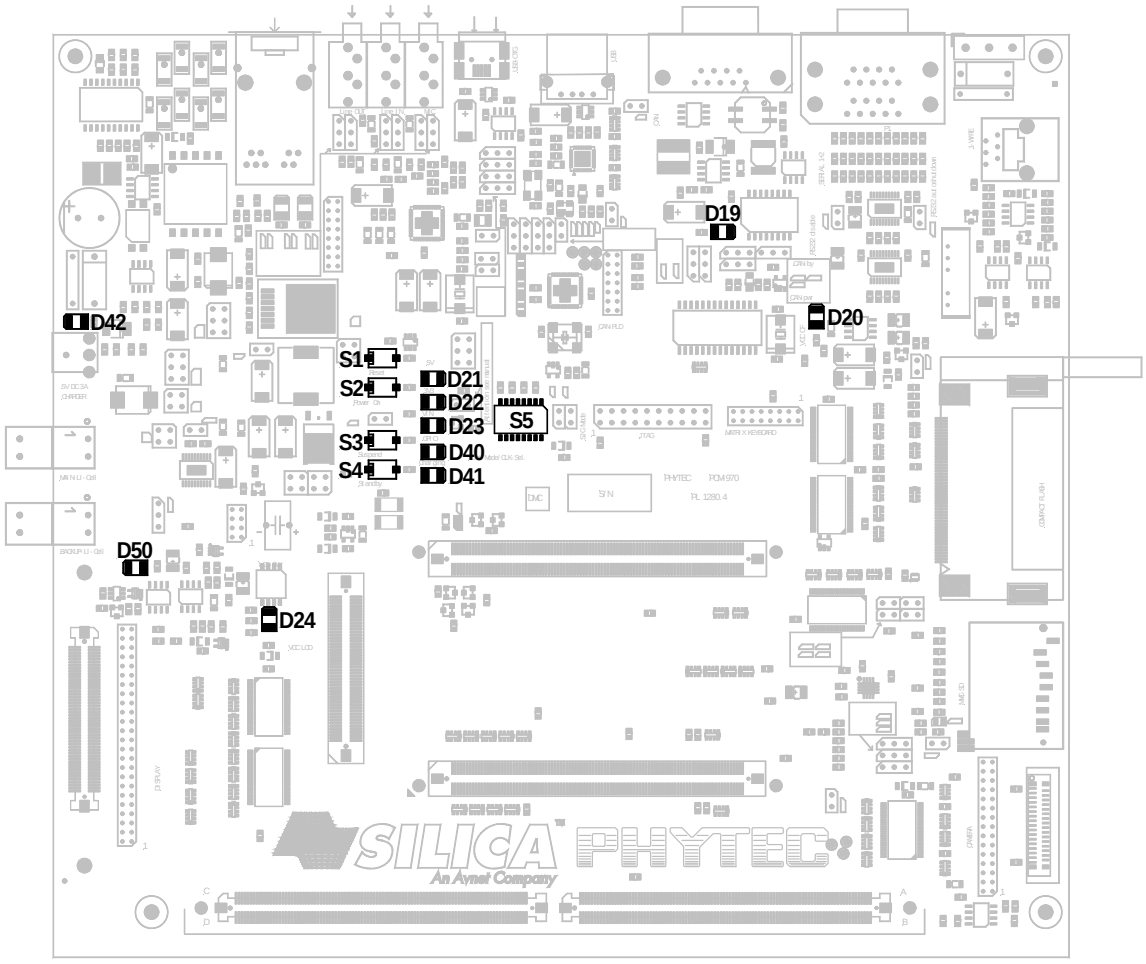

Figure 21: phyCORE-i.MX Carrier Board Buttons and LEDs

The phyCORE-i.MX35 module does not use the MC13783 power management IC so the push buttons S2, S3 and S4 are not supported. Also D20 and D41 should not be supported with the i.MX35 module.

The GPIO signal to drive D40 high or low is the X_GPIO2_6 signal of the i.MX35 module.

15.3.3.1 Boot-Mode and Clock Selection

Note:
Clock selection is not available with the i.MX35 module.

The i.MX35x controller is able to boot from different devices as described in *chapter 6.1.2* Boot Mode Select. To have a choice from which device the controller should boot the boot signals BOOT0 to BOOT4 are connected to two different dip-switches. These two switches are S5 on the i.MX Carrier Board and S1 on the phyMAP-i.MX35 mapper.

With S5 on the i.MX Carrier Board it is possible to select the status of BOOT0, BOOT1 and BOOT2. *For detailed information see Table 25, Table 26 and Table 27* below.

Note:
A standard Boot Configuration is already set on the i.MX35 module. Here you can change the Boot Mode to an alternatively mode. For standard Boot Configuration all dip switches have to be in OFF position.

Table 25: x_BOOT_MODE0 Selection

STATE OF SW NUMBER 3	STATE OF SW NUMBER 4	STATE OF X_BOOT0
ON	OFF	0
OFF	ON	1

Table 26: x_BOOT_MODE1 Selection

STATE OF SW NUMBER 5	STATE OF SW NUMBER 6	STATE OF X_BOOT1
ON	OFF	0
OFF	ON	1

Table 27: x_Switch

STATE OF SW NUMBER 7	STATE OF SW NUMBER 8	STATE OF X_BOOT2
ON	OFF	0
OFF	ON	1

15.3.4 Keypad Interface

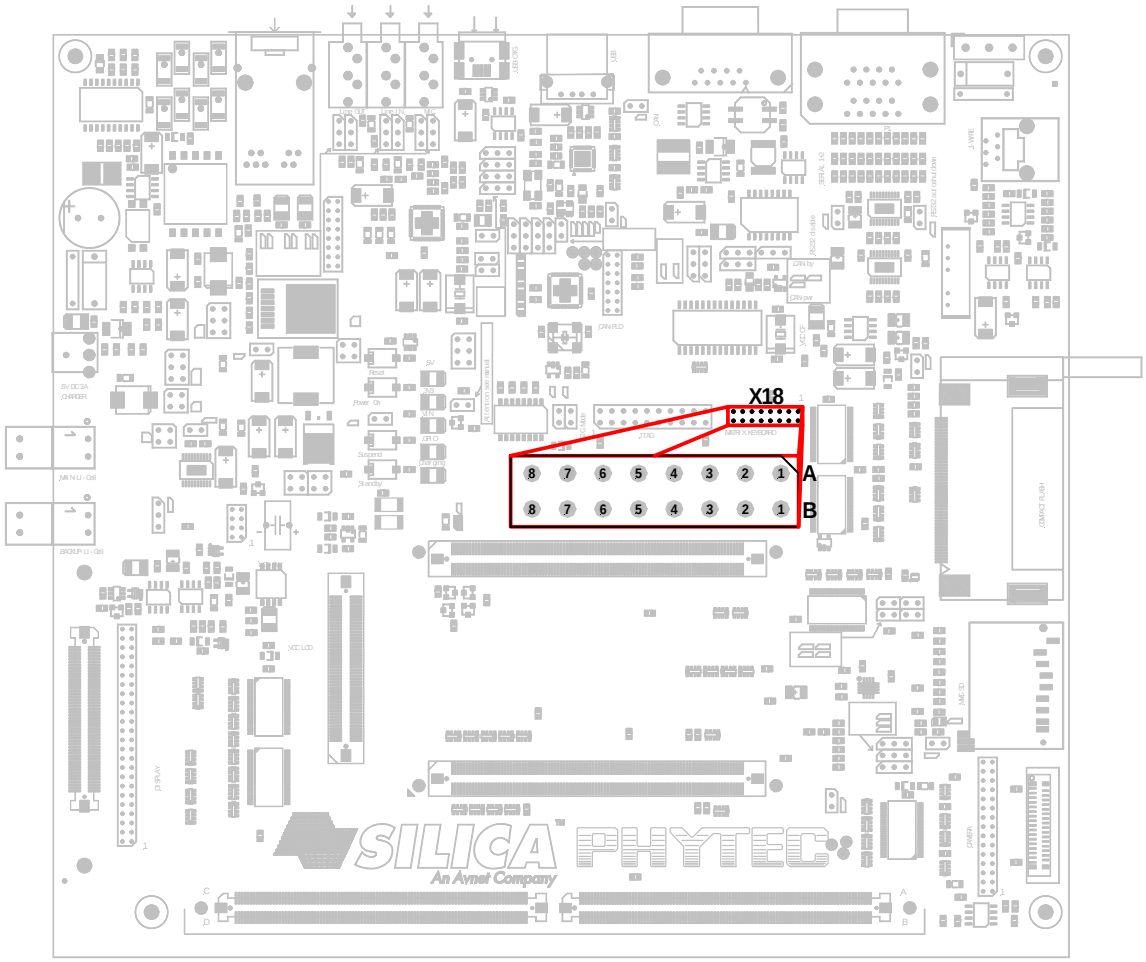

Figure 22: phyCORE-i.MX Carrier Board Keypad Interface

Although the phyCORE-i.MX Carrier Board supports a 6x6 keypad matrix interface, the i.MX35 module only provides a 4x4 matrix. So only the first four of the row and column lines (ROW0 to ROW3 and COL0 to COL3) are used.

15.3.5 Compact Flash Card

Note:
Compact Flash Card is not supported by the phyCORE-i.MX35 module, because there is no PCMCIA controller provided with the i.MX35x microcontroller.

15.3.6 Security Digital Card/ MultiMedia Card

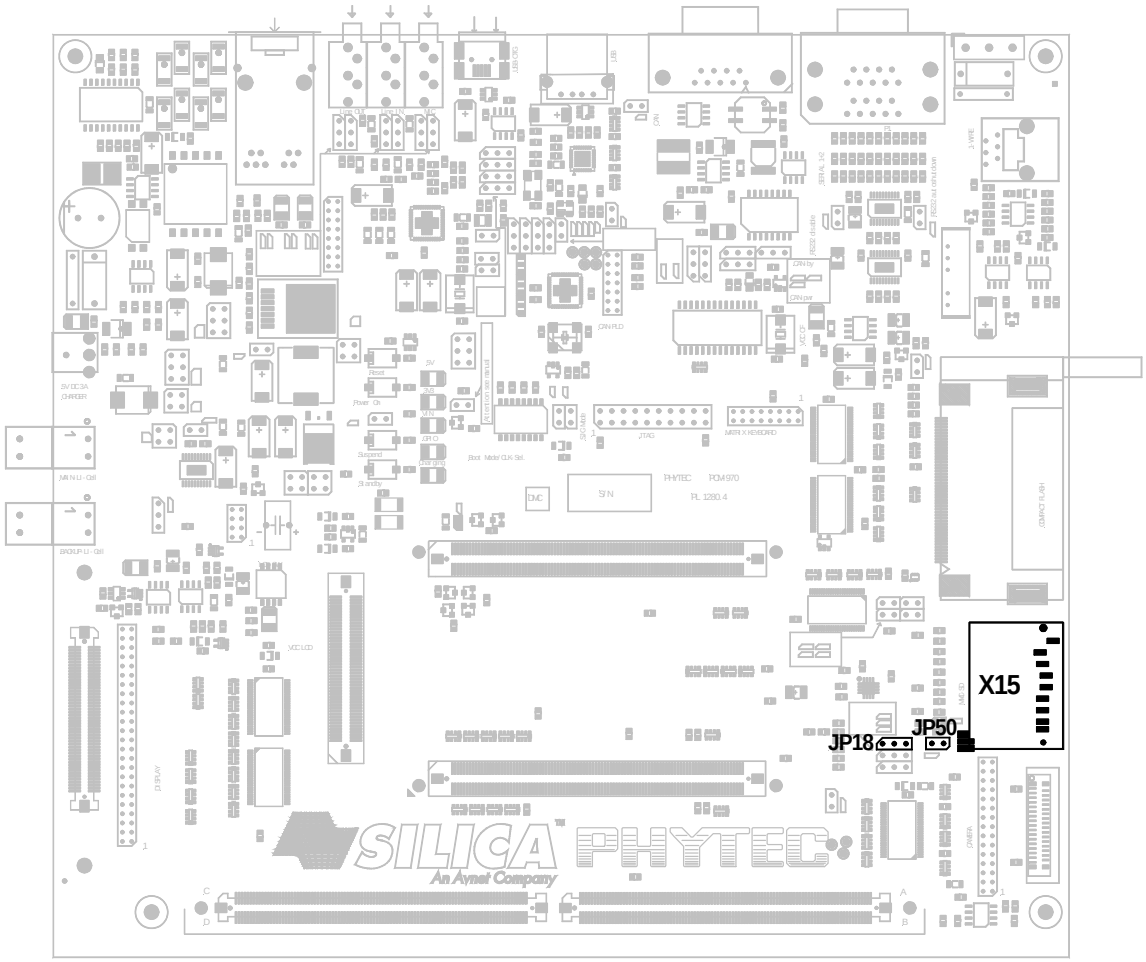

Figure 23: phyCORE-i.MX Carrier Board SD/MMC Card Interface

The MMC_DETECT signal is connected to GPIO signal X_GPIO2_24 of the i.MX35 module. MMC_WP is connected to GPIO signal X_GPIO2_23.

Table 28: SD/MMC Interface Jumper Settings for i.MX35 Module[5]

JUMPER	SETTING	DESCRIPTION
JP50	**2 + 3** 1 + 2	**MMC_WP signal of SD/MMC Interface is connected to GPIO** MMC_WP signal of SD/MMC Interface is not connected to GPIO
JP18	**2 + 3** 1 + 2	**Level shifter U25 is enabled** Level shifter U25 is disabled

5 : *Default settings for the phyCORE-i.MX35 SD/MMC interface are in **bold blue***

15.3.7 Audio and Touchscreen

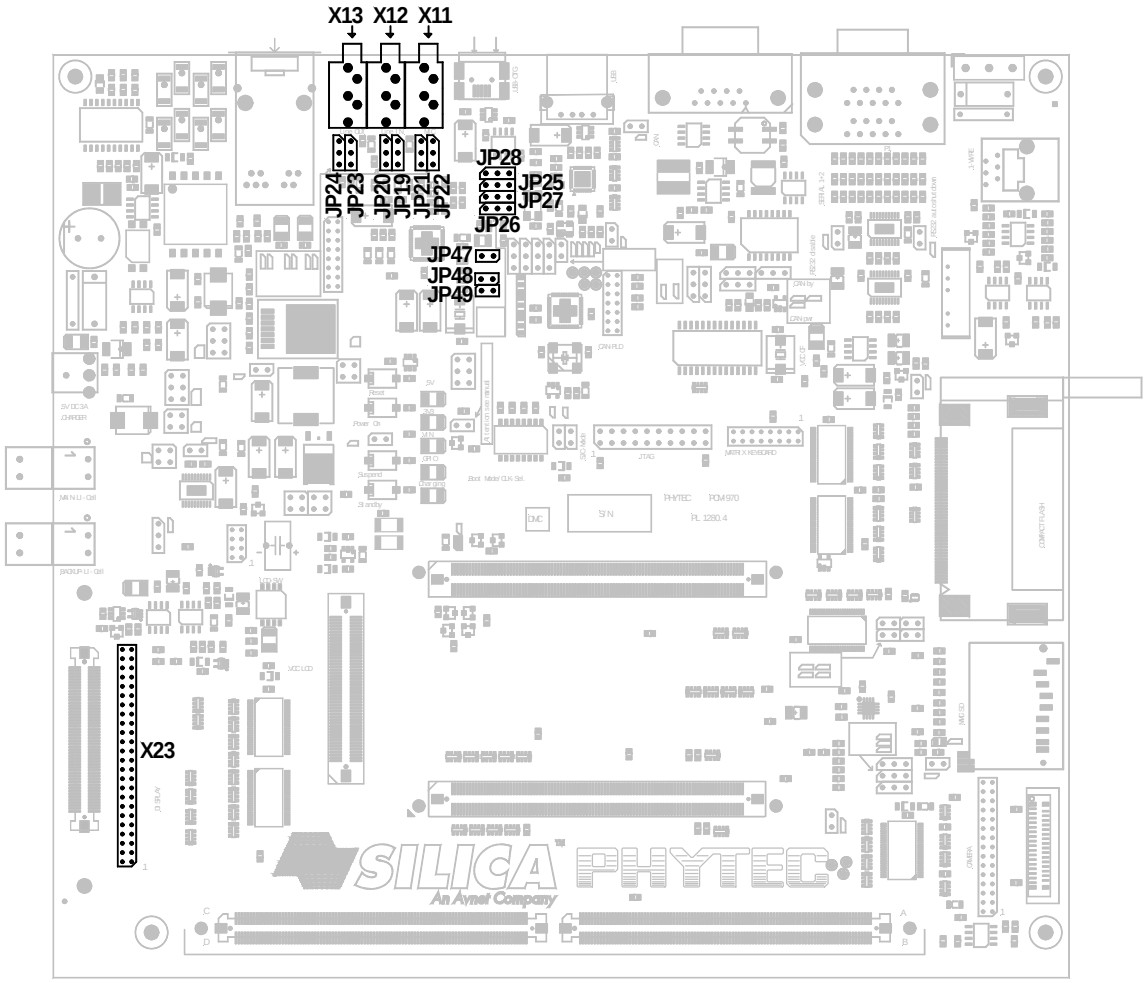

Figure 24: phyCORE-i.MX Carrier Board Audio/Touch Interface

With the phyCORE-i.MX35 module there is no audio/touchscreen device onboard, so the i.MX35 module has to use the audio/touchscreen device (U24) on the i.MX Carrier Board.
To select that this device should be used, there are a variety of jumpers which have to be set.

A detailed list of all jumper settings you will find in *Table 29* below.

Table 29: Audio/Touchscreen Interface Jumper Settings for i.MX35 Module[6]

JUMPER	SETTING	DESCRIPTION
JP21	2 + 3 **1 + 2**	x_MC1RIN is connected to X11 **MIC1 is connected to X11**
JP22	2 + 3 **1 + 2**	x_MC1LIN is connected to X11 **MIC2 is connected to X11**
JP19	2 + 3 **1 + 2**	x_RXOUTL is connected to X12 **LINE_INR is connected to X12**
JP20	2 + 3 **1 + 2**	x_RXOUTR is connected to X12 **LINE_INL is connected to X12**
JP23	2 + 3 **1 + 2**	x_RXINL is connected to X13 **LINE_OUTR is connected to X13**
JP24	2 + 3 **1 + 2**	x_RXINR is connected to X13 **LINE_OUTL is connected to X13**
JP25	2 + 3 **1 + 2**	x_TSY1 is connected to X23 **TP_Y- is connected to X23**
JP26	2 + 3 **1 + 2**	x_TSX2 is connected to X23 **TP_X+ is connected to X23**
JP27	2 + 3 **1 + 2**	x_TSY2 is connected to X23 **TP_Y+ is connected to X23**
JP28	2 + 3 **1 + 2**	X_TSX1 is connected to X23 **TP_X- is connected to X23**
JP47	open **closed**	Reset is held high, no asserting by GPIO of i.MX module **Reset can be asserted by GPIO of i.MX module**
JP48	open **closed**	No access to IRQ via GPIO of i.MX module **Access to IRQ via GPIO of i.MX module**
JP49	open **closed**	No access to PENDOWN via GPIO of i.MX module **Access to PENDOWN via GPIO of i.MX module**

6. *Settings for the phyCORE-i.MX35 audio/touchscreen interface are in **bold blue***

15.3.8 USB Host

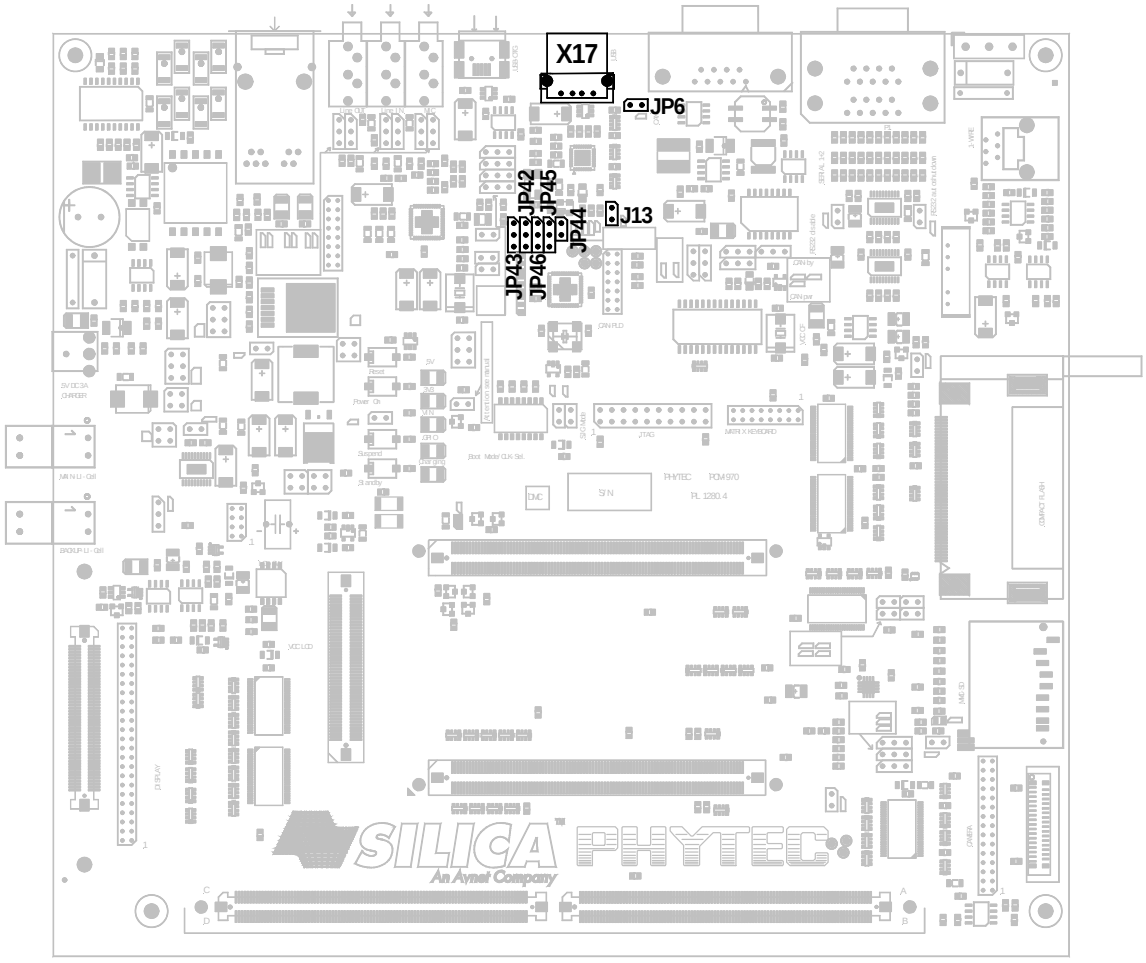

Figure 25: phyCORE-iMX Carrier Board USB-Host Interface

The i.MX35x controller comes with an integrated USB-Host-Phy, so that there is nothing more needed than an USB connector.
So the USB Host Transceiver (U26) that is realized on the i.MX Carrier Board is not needed with the phyCORE-i.MX35 module. There is a possibility to bypass the USB Host Transceiver (U24) via the jumpers JP42 to JP46 on the i.MX Carrier Board.

For further details and jumper settings have a look at Table 30.

Table 30: UBS Host Interface Jumper Settings for i.MX35 Module[7]

JUMPER	SETTING	DESCRIPTION
JP13	open **closed**	USB Host transceiver U26 is disabled, USB Host is out of operation **USB Host transceiver U26 is active, USB Host is in operation**
JP6	open **closed**	Reset pin is held HIGH, no Reset asserted **Reset pin is connected to GPIO2_0, Reset can be asserted**
JP42	1+2 **2+3**	USB Host is managed on the i.MX baseboard **USB Host is managed on the i.MX module**
JP43	1+2 **2+3**	USB Host is managed on the i.MX baseboard **USB Host is managed on the i.MX module**
JP44	**open** closed	**USB Host is managed on the i.MX module** USB Host is managed on the i.MX baseboard
JP45	1+2 **2+3**	USB Host is managed on the i.MX baseboard **USB Host is managed on the i.MX module**
JP46	1+2 **2+3**	USB Host is managed on the i.MX baseboard **USB Host is managed on the i.MX module**

7: *Settings for the phyCORE-i.MX35 USB-Host interface are in **bold blue***

15.3.9 LCD Connectors

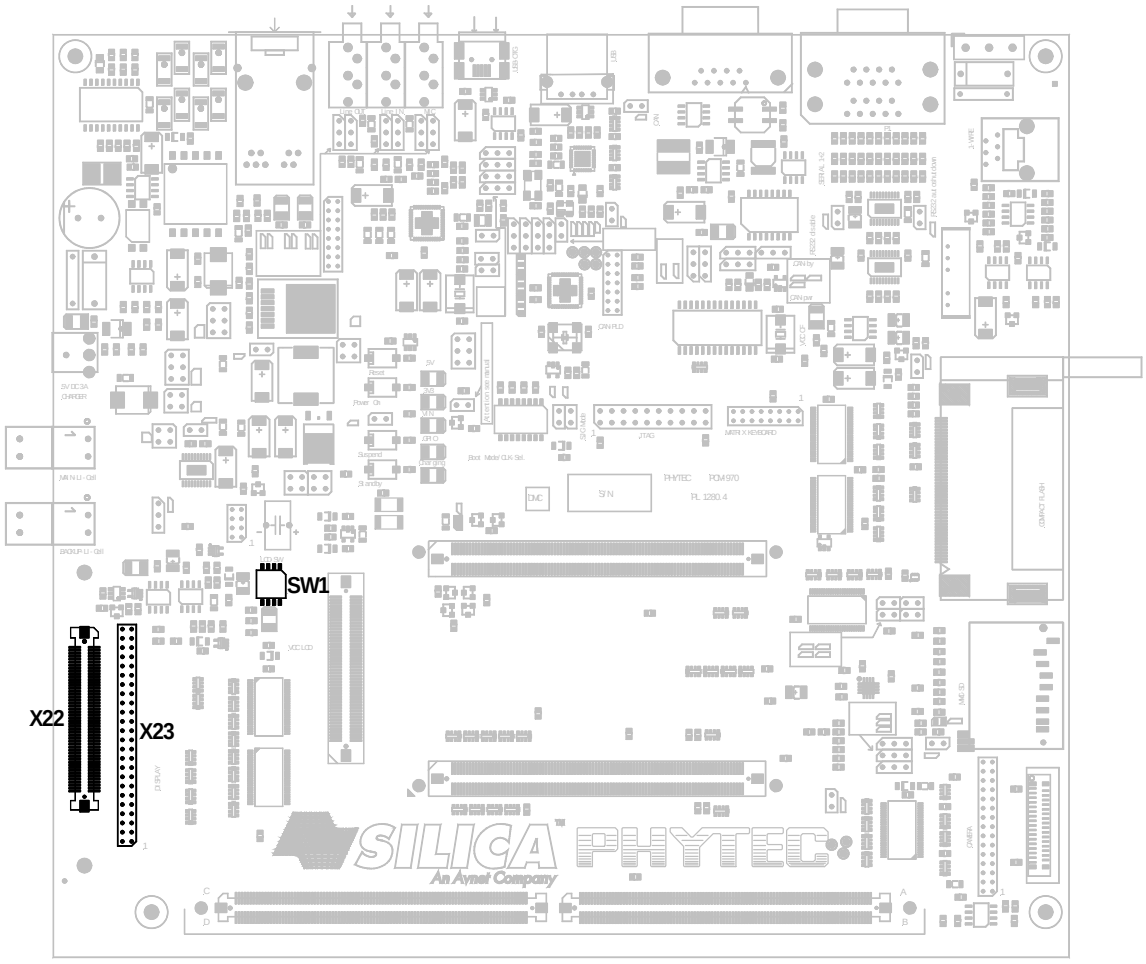

Figure 26: phyCORE-i.MX Carrier Board LCD Interfaces

The phyCORE-i.MX35 module comes with a 24-bit LCD interface. This 24-bit LCD interface is fully connected to the molex connectors X1 of the i.MX35 module and can be used in the customers application.
The phyCORE-i.MX Carrier Board has to support different i.MX modules, also modules with less than 24-bit LCD interfaces. That's why Phytec designed LCD connectors for 18-bit LCD interfaces but also for 24-bit LCDs.
So only the first 18-bits of the phyCORE-i.MX35 modules LCD interface (LD0 to LD17) are used on the i.MX Carrier Board LCD connectors.

15.3.9.1 Serial LCD

Note:
Serial LCD is not supported by the phyCORE-i.MX35 module, because the i.MX35x microcontroller does not provide Serial LCD.

15.3.10 Camera Interface

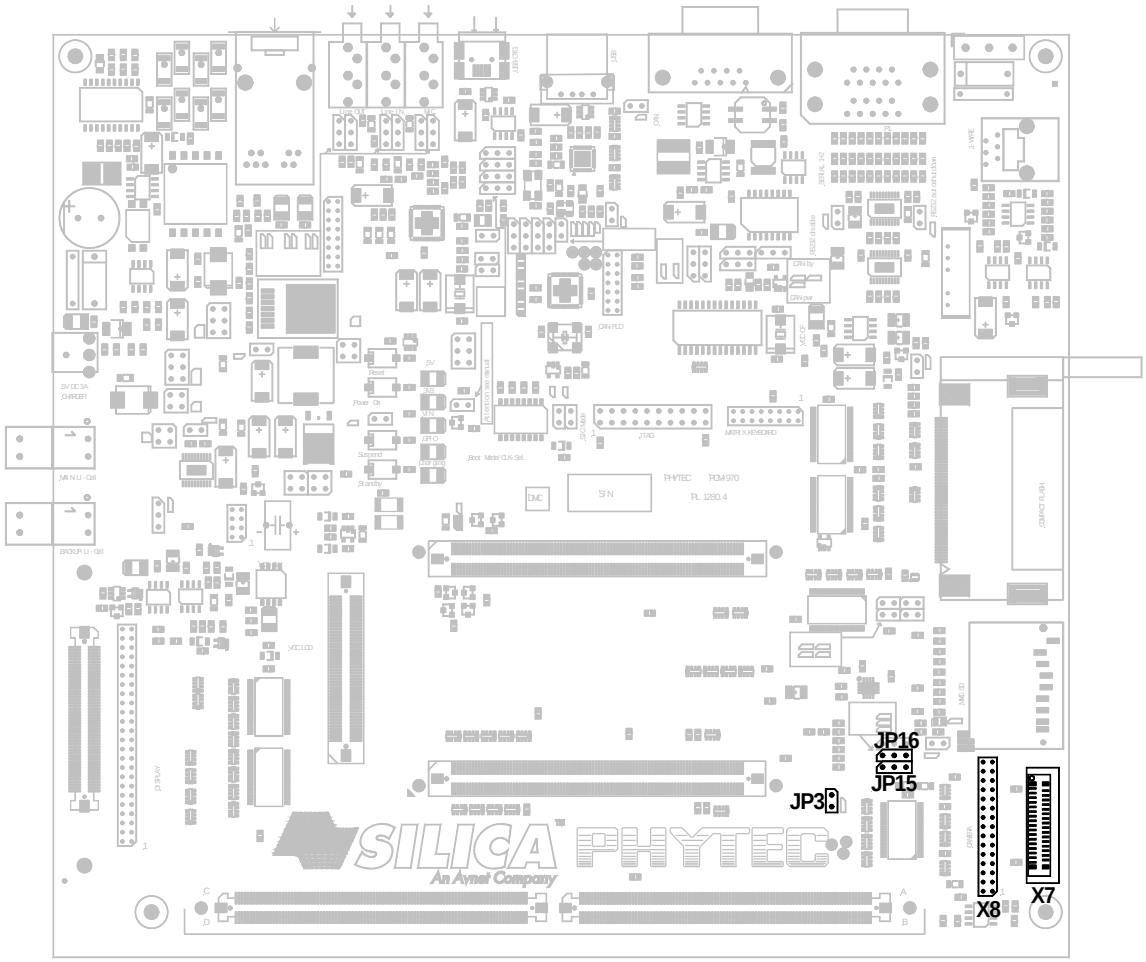

Figure 27: phyCORE-i.MX Carrier Board Camera Interface

The camera interface can be managed by the signal x_CSI_ENABLE connected to GPIO3_5 of the i.MX35 module.

Table 31: Camera Interface Jumper Settings for i.MX35 Module

JUMPER	SETTING	DESCRIPTION
JP3	closed **open**	Outputs of level shifter U12 are enabled, CSI is active **Outputs of U12 are disabled or GPIO x_CSI_ENABLE can be used to control U12**
JP16	**1 + 2** 2 + 3	Jumper settings to chance camera sensor specific I²C address. *For more information refer to the manual of the used camera sensor.*
JP15	**1 + 2** 2 + 3	**Use of Camera Connector X7 with VCC_CAM supply (3.3 V)** Use of Camera Connector X8 with external VCC_CAM_EXT supply

15.3.10.1 PHYTEC Camera Connector

Note:
The phyCORE-i.MX35 module uses a 10-bit camera interface (CSI_D6 to CSI_D15) at the Camera Connectors.

15.3.11 JTAG Interface

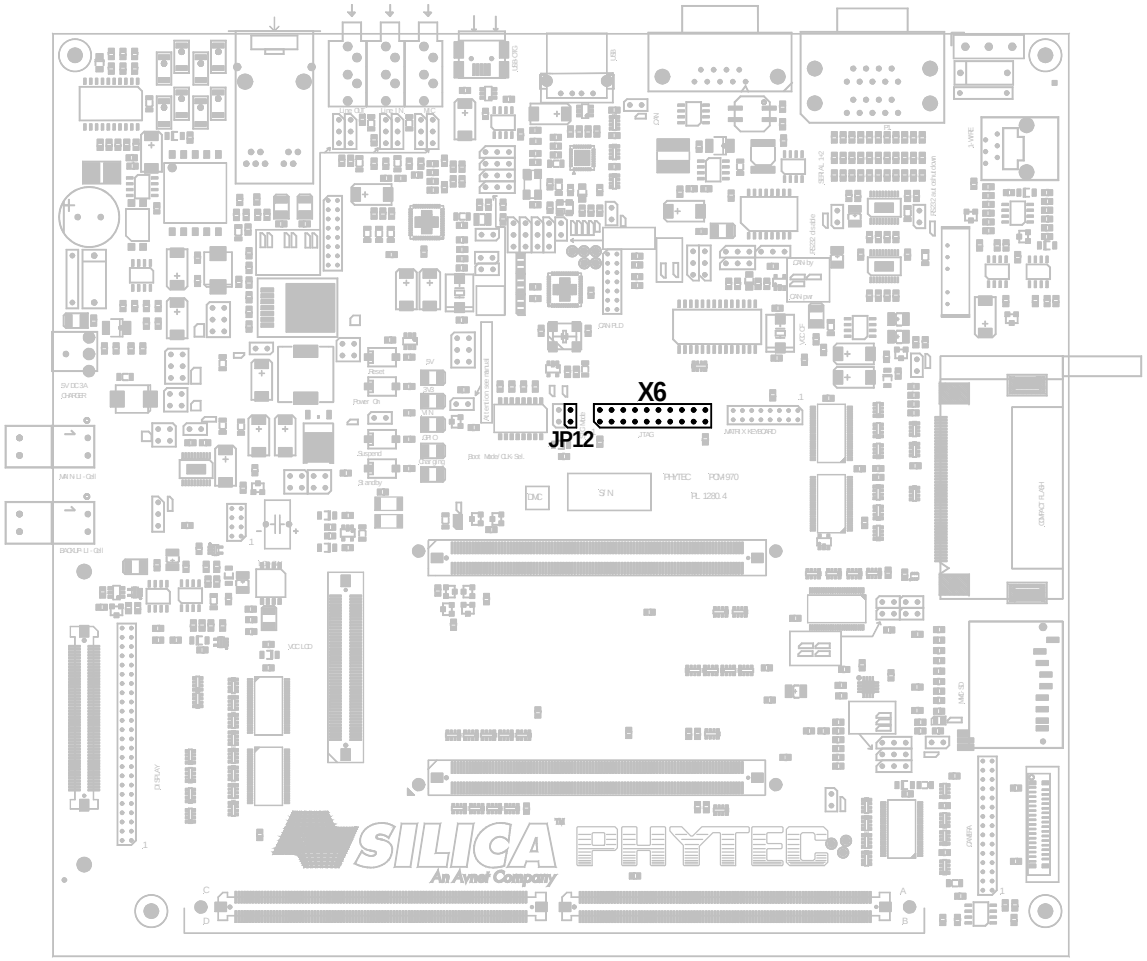

Figure 28: phyCORE-iMX Carrier Board JTAG Interface

Two JTAG modes are provided by the phyCORE-i.MX35 module dependent on the status of the sjc_mod signal of the i.MX35x controller.
Jumper JP12 can be used to select the JTAG mode the controller should operate in.

Table 32: JTAG Jumper Settings for phyCORE-i.MX35 Module[8]

JUMPER	SETTING	NAME	DESCRIPTION
JP12	**closed**	**Daisy chain ALL**	**For common software debug (High speed, production)**
	open	SJC only	IEEE 1149.1 JTAG compatible mode

8: *Default settings for the phyCORE-i.MX35 JTAG mode are in **bold blue***

15.3.12 Complete Jumper Setting List for phyCORE-i.MX35 on the i.MX Carrier Board

The following table contains all jumper settings that can be set on the phyCORE-i.MX Carrier Board. Also it shows the default jumper settings for using the phyCORE-i.MX35 module with the i.MX Carrier Board. These default jumper settings are normally done prior to delivery.

Table 33: Jumper Settings for i.MX35 Module on i.MX Carrier Board[9]

JUMPER	SETTING	DESCRIPTION
JP1	**Open**	**RS-232 transceivers are enabled**
	Closed	RS-232 transceivers are disabled
JP2	**Open**	**RS-232 auto shutdown is disabled**
	Closed	RS-232 auto shutdown is enabled
JP3	**Open**	**Camera interface is managed by x_CSI_ENABLE**
	Closed	Camera interface is always enabled
JP4	**Open**	**Compact Flash is in overwrite mode**
	Closed	Compact Flash is usable
JP5	Open	Compact-Flash is Slave
	Closed	**Compact-Flash is Master**
JP6	**Open**	**USBH2 transceiver Reset is not controllable**
	Closed	USBH2 transceiver Reset is controllable via GPIO
JP7	1+2	CAN is managed on the Carrier Board
	2+3	**CAN is managed on the module**
JP8	**1+2**	**CAN signals is are on the level VCC_CAN (from mapper)**
	2+3	CAN signals is are on the level VCC_5V
JP9	**1+2**	**CAN is supplied via on Board 5 V Power-Supply**
	2+3	CAN is supplied via an external Power-Supply
JP10	1+2	CAN is managed on the Carrier Board
	2+3	**CAN is managed on the module**
JP11	**1+2**	**CAN is supplied via on Board Power-Supply**
	2+3	CAN is supplied via an external Power-Supply
JP12	Open	Only the System JTAG Controller
	Closed	**All core's TAPS in a single daisy chain**
JP13	**Open**	**USB Host transceiver is disabled**
	Closed	USB Host transceiver is enabled
JP14	**Open**	**VCC_FUSE = 2.775 V (no FUSE programming)**
	Closed	VCC_FUSE = 3.3 V (use only for FUSE programming)
JP15	**1+2**	**Camera interface supplied via on-board 3.3 V supply**
	2+3	Camera interface is supplied via external supply

9: *Default settings are in **bold blue***

JP16	**1+2** 2+3	**CMOS-Sensor I²C address is 0x55** CMOS-Sensor I²C Address is 0x33
JP17	open **Closed**	Compact Flash expansion connector is enabled **Compact Flash expansion connector is disabled**
JP18	1+2 **2+3**	MMC driver is disabled **MMC driver is enabled**
JP19	**1+2** 2+3	**Stereo output is managed on the baseboard** Stereo output is managed on the module
JP20	**1+2** 2+3	**Stereo output is managed on the baseboard** Stereo output is managed on the module
JP21	**1+2** 2+3	**Stereo MIC is managed on the baseboard** Stereo MIC is managed on the module
JP22	**1+2** 2+3	**Stereo MIC is managed on the baseboard** Stereo MIC is managed on the module
JP23	**1+2** 2+3	**Stereo LINE IN is managed on the baseboard** Stereo LINE IN is managed on the module
JP24	**1+2** 2+3	**Stereo LINE IN is managed on the baseboard** Stereo LINE IN is managed on the module
JP25	**1+2** 2+3	**Touch screen is managed on the baseboard** Touch screen is managed on the module
JP26	**1+2** 2+3	**Touch screen is managed on the baseboard** Touch screen is managed on the module
JP27	**1+2** 2+3	**Touch screen is managed on the baseboard** Touch screen is managed on the module
JP28	**1+2** 2+3	**Touch screen is managed on the baseboard** Touch screen is managed on the module
JP29	1+2 **2+3**	Backup voltage is supplied by ext. LICELL **Backup voltage is supplied by onboard Goldcap**
JP30	1+2 3+4 5+6	VCC_BOOT is deep-sleep test voltage VCC_CLK is deep-sleep test voltage VCC_JTAG is deep-sleep test voltage
JP31	1+3,2+4 **3+5,4+6**	Power source is Power Over Ethernet (POE) **Power source is 5 V adapter**
JP32	1+3,2+4 **3+5,4+6**	No power switching, direct supply of VCC_3V3 **Separate supply path**
JP33	1+2,3+4 **Open,Open**	No power switching, direct supply from VCC_3V3 **Separate supply path**

JP34	1+2,3+4 **Open,Open**	No power switching, direct supply from VCC_3V3 **Separate supply path**
JP35	**Open** Closed	**VCC_5V Power Supply is enabled** VCC_5V Power Supply is disabled
JP36	Open **Closed**	VCC_3V3 Power Supply is disabled **VCC_3V3 Power Supply is enabled**
JP37	Open Closed	Chargemode is Single Path Chargemode is Dual Path
JP38	**1+2,3+4** Open,Open	**Power switching, supply from 5 V adapter or POE** No power switching, direct supply from VCC_3V3
JP39	1+2,3+4 **Open,Open**	Power switching active, Battery charge path closed **No power switching, direct supply from VCC_3V3**
JP40	**Open** Closed	**No power switching active, minimum circuit** Power switching active
JP42	1+2 **2+3**	USB VBUS power enable managed on baseboard **USB VBUS power enable managed on module**
JP43	1+2 **2+3**	USB VBUS overcurrent managed on the baseboard **USB VBUS overcurrent managed on the module**
JP44	**open** closed	**USB Host is managed on the module** USB Host is managed on the baseboard
JP45	1+2 **2+3**	USB Host is managed on the baseboard **USB Host is managed on the module**
JP46	1+2 **2+3**	USB Host is managed on the baseboard **USB Host is managed on the module**
JP47	open **closed**	Reset of audio/touch device is not controllable **Reset of audio/touch device is controllable via GPIO**
JP48	open **closed**	IRQ of audio/touch device is not controllable **IRQ of audio/touch device is controllable via GPIO**
JP49	open **closed**	PENDOWN of audio/touch device is not controllable **PENDOWN of audio/touch device is controllable via GPIO**
JP50	open **closed**	SD card write protect is not connected to the module **SD card write protect is connected to the module**
JP602	**Open** Closed	**PC_RW inverted** PC_RW non-inverted
JP604	**Open** Closed	**CF power is manged by x_EXP007** Force enabling VCC_CFL

16 Revision History

Date	Version numbers	Changes in this manual
04-June-2009	Manual L-734e_0 PCM-043 PCB# 1315.2 PMA-005 PCB# 1318.2 PCM-970 PCB# 1280.4	First draft, Preliminary documentation. Describes the phyCORE-i.MX35 with the i.MX35 Mapper and the i.MX Carrier Board.
17-June-2010	Manual L-734e_1 PCM-043 PCB# 1315.4 PMA-005 PCB# 1318.2 PCM-970 PCB# 1280.4	

17 Component Placement Diagram

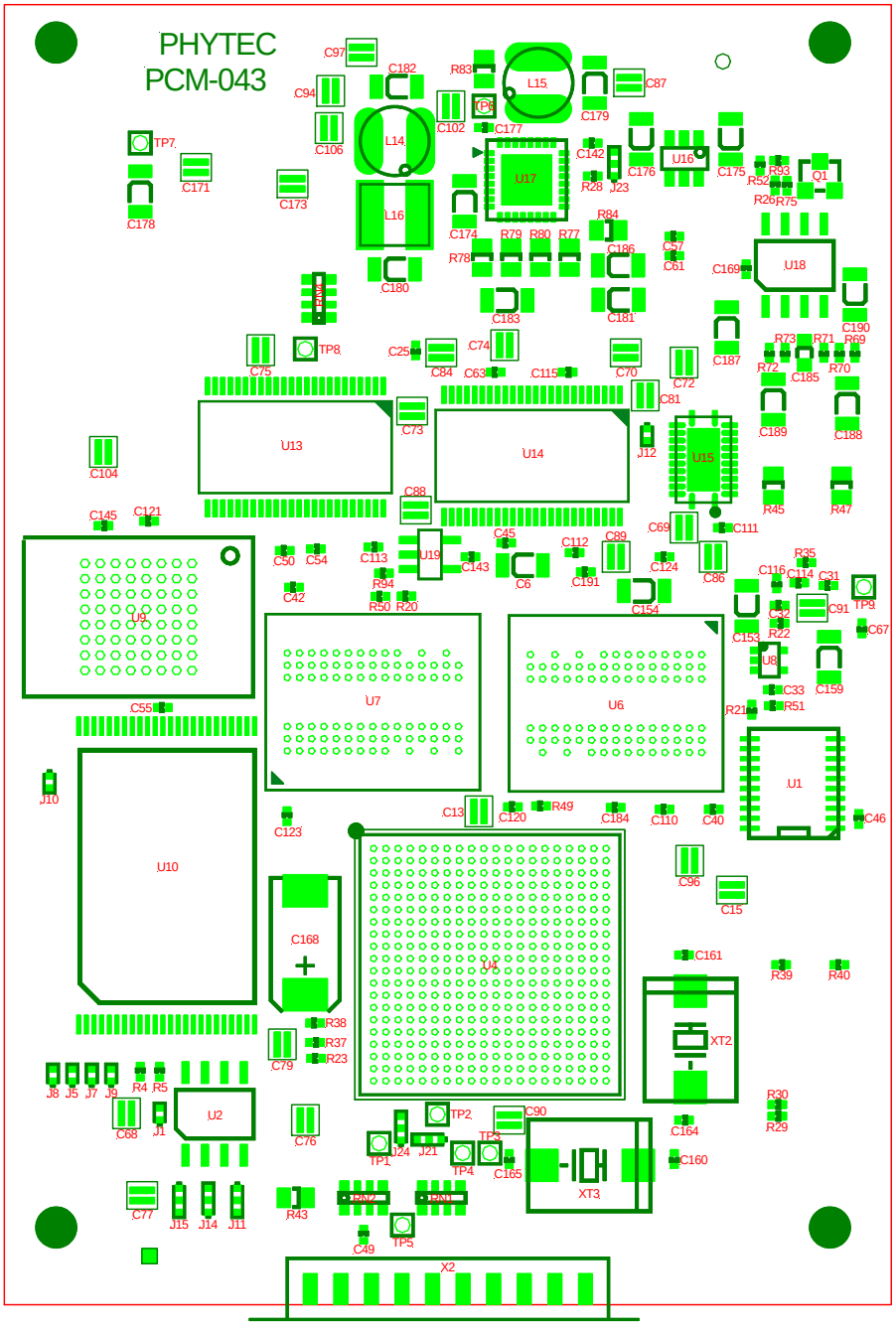

Figure 29: phyCORE-i.MX35 Component Placement (Top View)

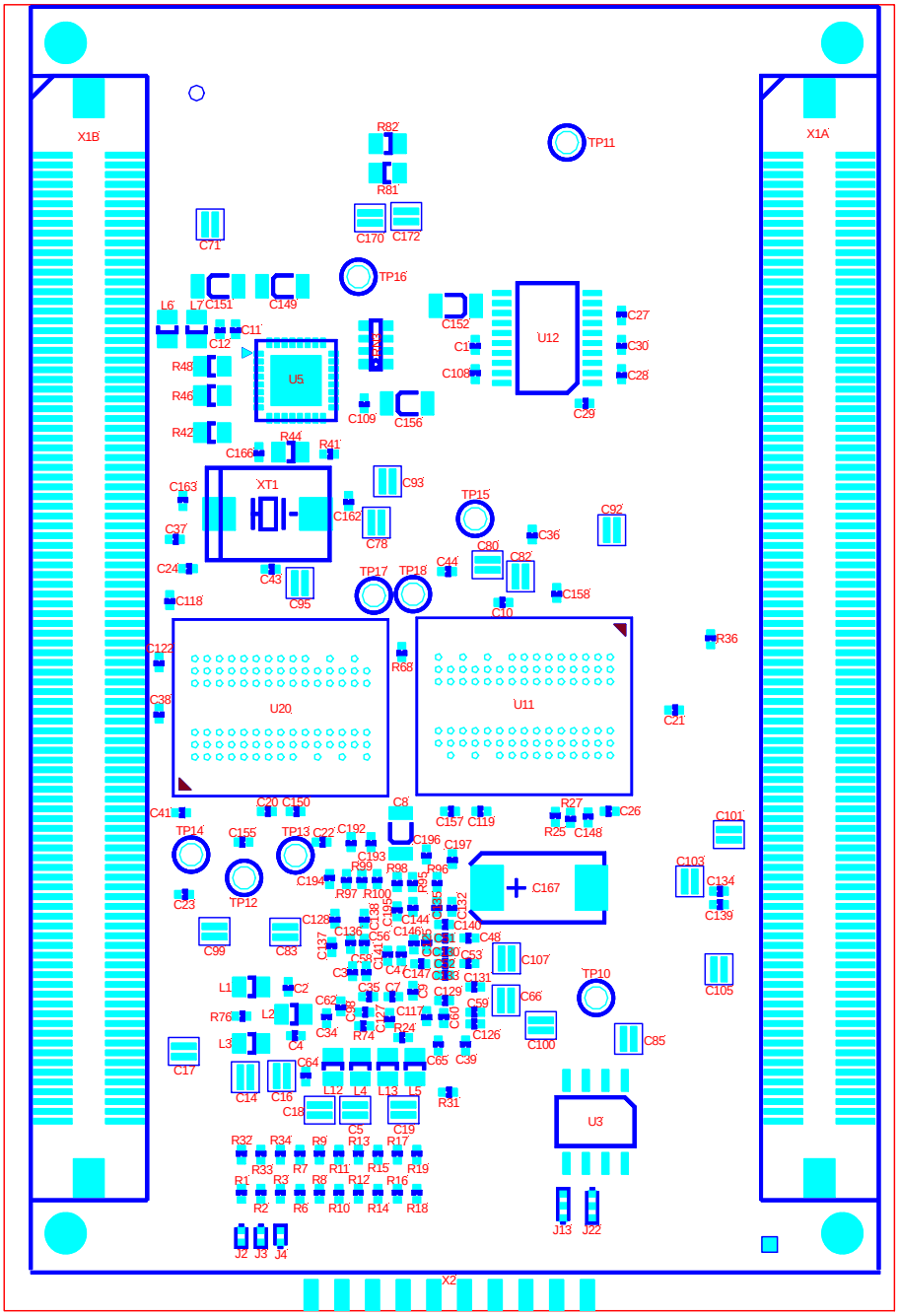

Figure 30: phyCORE-i.MX35 Component Placement (Bottom View)

Index

U

W

X

Document: **phyCORE-i.MX35**
Document number: **L-734e_1**

How would you improve this manual?

Did you find any mistakes in this manual? page

Submitted by:
Customer number:

Name:

Company:

Address:

Return to:

PHYTEC Technologie Holding AG
Postfach 100403
D-55135 Mainz, Germany
Fax : +49 (6131) 9221-33

Published by

PHYTEC

Ordering No. L-734_1
Printed in Germany