A product of a PHYTEC Technology Holding company

phyBOARD®-Segin i.MX 6UL/ULL

Hardware Manual

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Conventions, Abbreviations and Acronyms

This hardware manual describes the PB-02013-XXX Single Board Computer (SBC) in the following referred to as phyBOARD-Segin i.MX 6UL/ULL. The manual specifies the phyBOARD-Segin i.MX 6UL/ULL's design and function. Precise specifications for the NXP® Semiconductor i.MX 6UL/ULL microcontrollers can be found in the NXP® Semiconductor's i.MX 6UL/ULL Data Sheet and Technical Reference Manual.

Conventions

The conventions used in this manual are as follows:
- Signals that are preceded by an "n", "/", or "#"character (e.g.: nRD, /RD, or #RD), or that have a dash on top of the signal name (e.g.: $\overline{\text{RD}}$) are designated as active low signals. That is, their active state is when they are driven low, or are driving low.
- A "0" indicates a logic zero or low-level signal, while a "1" represents a logic one or high-level signal.
- The hex-numbers given for addresses of I^{2}C devices always represent the 7 MSB of the address byte. The correct value of the LSB which depends on the desired command (read (1), or write (0)) must be added to get the complete address byte. E.g. given address in this manual 0x41 => complete address byte = 0x83 to read from the device and 0x82 to write to the device.
- Tables which describe jumper settings show the default position in **bold, blue text.**
- Text in *blue italic* indicates a hyperlink within, or external to the document. Click these links to quickly jump to the applicable URL, part, chapter, table, or figure.
- Text in ***bold italic*** indicates an interaction by the user, which is defined on the screen.
- Text in `Consolas` indicates an input by the user, without a premade text or button to click on.
- Text in *italic* indicates proper names of development tools and corresponding controls (windows, tabs, commands etc.) used within the development tool, no interaction takes place.
- White Text on black background shows the result of any user interaction (command, program execution, etc.)

Abbreviations and Acronyms

Many acronyms and abbreviations are used throughout this manual. Use the table below to navigate unfamiliar terms used in this document.

Abbreviation	Definition
A/V	Audio/Video
BSP	Board Support Package (Software delivered with the Development Kit including an operating system (*Windows*, or *Linux*) pre-installed on the module and Development Tools)
CB	Carrier Board, used in reference to the phyBOARD-Segin i.MX 6UL/ULL Development Kit Carrier Board
DFF	D flip-flop
DSC	Direct Solder Connect
EMB	External memory bus
EMI	Electromagnetic Interference
GPI	General purpose input
GPIO	General purpose input and output
GPO	General purpose output
IRAM	Internal RAM, the internal static RAM on the NXP® Semiconductor i.MX 6UL/ULL microcontroller
J	Solder jumper, these types of jumpers require solder equipment to remove and place
JP	Solderless jumper, these types of jumpers can be removed and placed by hand with no special tools
NC	Not Connected
NM	Not Mounted
NS	Not Specified
PCB	Printed circuit board
PDI	Phytec Display Interface, defined to connect Phytec display adapter boards, or custom adapters
PEB	Phytec Expansion Board
PMIC	Power management IC
PoE	Power over Ethernet
PoP	Package on Package
POR	Power-on reset
RTC	Real-time clock
SBC	Single Board Computer, used in reference to the PBA-CD-10 / phyBOARD-Segin i.MX 6UL/ULL
SMT	Surface mount technology
SOM	System on Module, used in reference to the PCL-063 / phyCORE-i.MX 6UL/ULL module
Sx	User button Sx (e.g. S1, S2) used in reference to the available user buttons, or DIP switches on the CB
Sx_y	Switch y of DIP switch Sx, used in reference to the DIP switch on the carrier board
VSTBY	SOM standby voltage input

Table 1: Abbreviations and Acronyms used in this Manual

	At this icon you might leave the path of this Application Guide.
	This is a warning. It helps you to avoid annoying problems.
	You can find useful supplementary information about the topic.
	At the beginning of each chapter you can find information about the time required to read the following chapter.
	You have successfully completed an important part of this Application Guide.
	You can find information to solve problems.

Note:
The BSP is configured according to the hardware configuration including the expansion board delivered with the kit. Thus some functions of the phyBOARD-Segin i.MX 6UL/ULL might not be available if the corresponding pins and drivers are needed to support an expansion board. If the expansion board is removed, or exchanged the BSP must be exchanged, too.

Preface

As a member of Phytec's phyBOARD® product family the phyBOARD-Segin i.MX 6UL/ULL is one of a series of Phytec System on Modules (SBCs) that offer off-the-shelf solutions for a huge variety of industrial applications. The new phyBOARD® product family consists of a series of extremely compact embedded control engines featuring various processing performance classes. All phyBOARDs are rated for industry, cost optimized and offer long-term availability. The phyBOARD-Segin i.MX 6UL/ULL is one of currently six industrial-grade carrier boards which are suitable for series production and that have been realized in accordance with Phytec's new SBCplus concept. It is an excellent example of this concept.

SBCplus Concept

The SBCplus concept was developed to meet fine differences in customer requirements with little development effort and thus to greatly reduce the time-to-market.

Core of the SBCplus concept is the SBC design library (a kind of construction set) that consists of a great number of function blocks (so-called "building blocks") which are refined constantly. The recombination of these function blocks allows to develop a customer specific SBC within a short time. Thus, Phytec is able to deliver production-ready custom Single Board Computers within a few weeks at very low costs.

The already developed SBCs, such as the phyBOARD-Segin i.MX 6UL/ULL, each represent an intersection of different customer wishes. Because of that all necessary interfaces are already available on the standard versions, thus, allowing to integrate them in a large number of applications without modification. For any necessary detail adjustment extension connectors are available to enable adding of a wide variety of functions.

Cost-optimized with Half-Hole Technology

At the heart of the phyBOARD-Segin i.MX 6UL/ULL is the phyCORE-i.MX 6UL/ULL System on Module (SOM). As with other SBCs of the phyBOARD® family the SOM can be directly soldered onto the carrier board PCB for routing of signals from the SOM to applicable I/O interfaces. This Half-Hole Technology of the SOM eliminates costly PCB to PCB connectors, thereby further reducing overall system costs, and making the phyBOARDs ideally suited for deployment into a wide range of cost-optimized and robust industrial applications.

Customized Expandability from Phytec

Common interface signals route to standard connector interfaces on the carrier board such as Ethernet, CAN, RS-232, and audio. Due to the easily modifiable phyBOARD design approach (see "*SBCplus concept*"), these plug-and-play interfaces can be readily adapted in customer-specific variants according to end system requirements.

Some signals from the processor populating the SOM also extend to the expansion, and A/V connectors of the phyBOARD-Segin i.MX 6UL/ULL. This provides for customized expandability according to end user requirements. Thus expandability is made easy by available plug-and-play expansion modules from Phytec.

- HDMI and LVDS/Parallel Displays
- Power Supply, with broad voltage range
- Industrial I/O (including WLAN)
- Home-Control Board (WiFi, KNX/EIB, I/O)
- M2M Board (GPS, GSM, I/O's)
- Debug Adapter

The default orientation of the expansion bus connectors is parallel and on the top side of the carrier board PCB. However, in custom configurations the connectors can be mounted on the PCB's underside. Connectors in perpendicular orientation can also populate the top or underside of the PCB. This enables maximum flexibility for orientation of expansion modules on the phyBOARD-Segin i.MX 6UL/ULL, as well as integration of the system into a variety of end application physical envelopes and form factors.

Easy Integration of Display und Touch
The phyBOARD and its expansion modules enable easy connection of parallel or LVDS based displays, as well as resistive or capacitive touch screens.

OEM Implementation
Implementation of an OEM-able SBC subassembly as the "core" of your embedded design allows you to focus on hardware peripherals and firmware without expending resources to "re-invent" microcontroller circuitry. Furthermore, much of the value of the phyBOARD® SBC lies in its layout and test.

Software Support
Production-ready Board Support Packages (BSPs) and Design Services for our hardware will further reduce your development time and risk and allow you to focus on your product expertise.

Ordering Information

Ordering numbers:
phyBOARD-Segin i.MX 6UL/ULL Development Kit: **KPB-02013-xxx**
phyBOARD-Segin i.MX 6UL/ULL SBC: **PB-02013-xxx**

Product Specific Information and Technical Support

In order to receive product specific information on changes and updates in the best way also in the future, we recommend to register at

http://www.phytec.de/de/support/registrierung.html or
http://www.phytec.eu/europe/support/registration.html

For technical support and additional information concerning your product, please visit the download section of our web site which provides product specific information, such as errata sheets, application notes, FAQs, etc.

http://www.phytec.de/produkt/single-board-computer/phyboard-segin-download/ or
http://www.phytec.eu/europe/support/faq/faq-phyBOARD-Segin-i.MX6.html

Other Products and Development Support

Aside of the new phyBOARD® familiy, Phytec supports a variety of 8-/16- and 32-bit controllers in two ways:

(1)   as the basis for Rapid Development Kits which serve as a reference and evaluation platform

(2)   as insert-ready, fully functional OEM modules, which can be embedded directly into the user's peripheral hardware design.

Take advantage of Phytec products to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks. With this new innovative full system solution you will be able to bring your new ideas to market in the most timely and cost-efficient manner.

For more information go to:

http://www.phytec.de/de/leistungen/entwicklungsunterstuetzung.html or
http://www.phytec.eu/europe/oem-integration/evaluation-start-up.html

Declaration of Electro Magnetic Conformity of the Phytec phyBOARD-Segin i.MX 6UL/ULL

CE

Phytec Single Board Computers (henceforth products) are designed for installation in electrical appliances, or as part of custom applications, or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution!
Phytec products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, Phytec products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

Phytec products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Implementation of Phytec products into target devices, as well as user modifications and extensions of Phytec products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

Product Change Management and information in this manual on parts populated on the SOM / SBC

When buying a Phytec SOM / SBC, you will, in addition to our HW and SW offerings, receive a free obsolescence maintenance service for the HW we provide.

Our PCM (Product Change Management) Team of developers, is continuously processing, all incoming PCN's (Product Change Notifications) from vendors and distributors concerning parts which are being used in our products.

Possible impacts to the functionality of our products, due to changes of functionality or obsolesce of a certain part, are being evaluated in order to take the right masseurs in purchasing or within our HW/SW design.

Our general philosophy here is: **We never discontinue a product as long as there is demand for it.**

Therefore we have established a set of methods to fulfill our philosophy:

Avoiding strategies

- Avoid changes by evaluating long-livety of parts during design in phase.
- Ensure availability of equivalent second source parts.
- Stay in close contact with part vendors to be aware of roadmap strategies.

Change management in case of functional changes

- Avoid impacts on product functionality by choosing equivalent replacement parts.
- Avoid impacts on product functionality by compensating changes through HW redesign or backward compatible SW maintenance.
- Provide early change notifications concerning functional relevant changes of our products.

Change management in rare event of an obsolete and non replaceable part

- Ensure long term availability by stocking parts through last time buy management according to product forecasts.
- Offer long term frame contract to customers.

Therefore we refrain from providing detailed part specific information within this manual, which can be subject to continuous changes, due to part maintenance for our products.

In order to receive reliable, up to date and detailed information concerning parts used for our product, please contact our support team through the contact information given within this manual.

1 Introduction

1.1 Hardware Overview

The phyBOARD-Segin i.MX 6UL/ULL for phyCORE-i.MX 6UL/ULL modules is a low-cost, feature-rich software development platform supporting the NXP® Semiconductor i.MX 6UL/ULL microcontroller. Moreover, due to the numerous standard interfaces the phyBOARD-Segin i.MX 6UL/ULL can serve as bedrock for your application. At the core of the phyBOARD-Segin i.MX 6UL/ULL is the PCL-063/phyCORE-i.MX 6UL/ULL System On Module (SOM), containing the processor, DRAM, NAND Flash, power regulation, supervision, transceivers, and other core functions required to support the i.MX 6UL/ULL processor. Surrounding the SOM is the PBA-CD-10/ phyBOARD-Segin i.MX 6UL/ULL carrier board, adding power input, buttons, connectors, signal breakout, and Ethernet connectivity amongst other peripherals.

The phyCORE-i.MX 6UL/ULL (PCL-063) is a connector-less, BGA style System On Module (SOM) in a direct solder form factor. Unlike traditional Phytec SOM products that support high density connectors, the PCL-063 SOM is directly soldered down to the phyBOARD-Segin i.MX 6UL/ULL using Half-Hole Technology. This solution offers an ultra-low cost Single Board Computer for the i.MX 6UL/ULL processor, while maintaining most of the advantages of the SOM concept.

Adding the phyCORE-i.MX 6UL/ULL SOM into your own design is as simple as ordering the connectored version (PCL-063) and making use of our phyCORE Carrier Board reference schematics.

1.1.1 Features of the phyBOARD-Segin i.MX 6UL/ULL

The phyBOARD-Segin i.MX 6UL/ULL supports the following features :

- Developed in accordance with Phytec's new SBCplus concept (*Preface*)
- Phytec's phyCORE-i.MX 6UL/ULL SOM with plated half-hole connection, featuring a single ARM Cortex-A7 core operating at speeds up to 696 MHz
- Pico ITX standard dimensions (100 mm × 72 mm)
- Boot from SD card or NAND Flash
- Two different power supply options (5 V via 3.5 mm combicon, or 12 V – 24 V through external power module)
- Two RJ45 jacks for 10/100 Mbps Ethernet
- One USB host interface brought out to an upright USB Standard-A connector
- One USB OTG interface available at an USB Micro-AB connector at the back side, or at the expansion connector
- One Secure Digital / Multi Media Memory Card interface brought out to a Micro-SD connector at the back side
- CAN interface at 2×5 pin header 2.54 mm

- Audio codec with Stereo Line In and Line Out (3x2 pin header 2.54 mm) and Mono Speaker (2-pole Molex)
- One parallel camera interface compatible to Phytec phyCAM-P camera standard with I^2C for camera control
- RS-232 or RS-485 transceiver supporting UART5 incl. handshake signals with data rates of up to 1 Mbps (2×5 pin header 2.54 mm)
- Reset-Button
- CPU ONOFF-Button
- Audio/Video (A/V) connectors including a touch screen interface
- Expansion connector with different interfaces
- External RTC
- Backup supply for RTC via external 2-pole pin header or with Gold cap (lasts approx. 11½ days)

1.1.2 Block Diagram
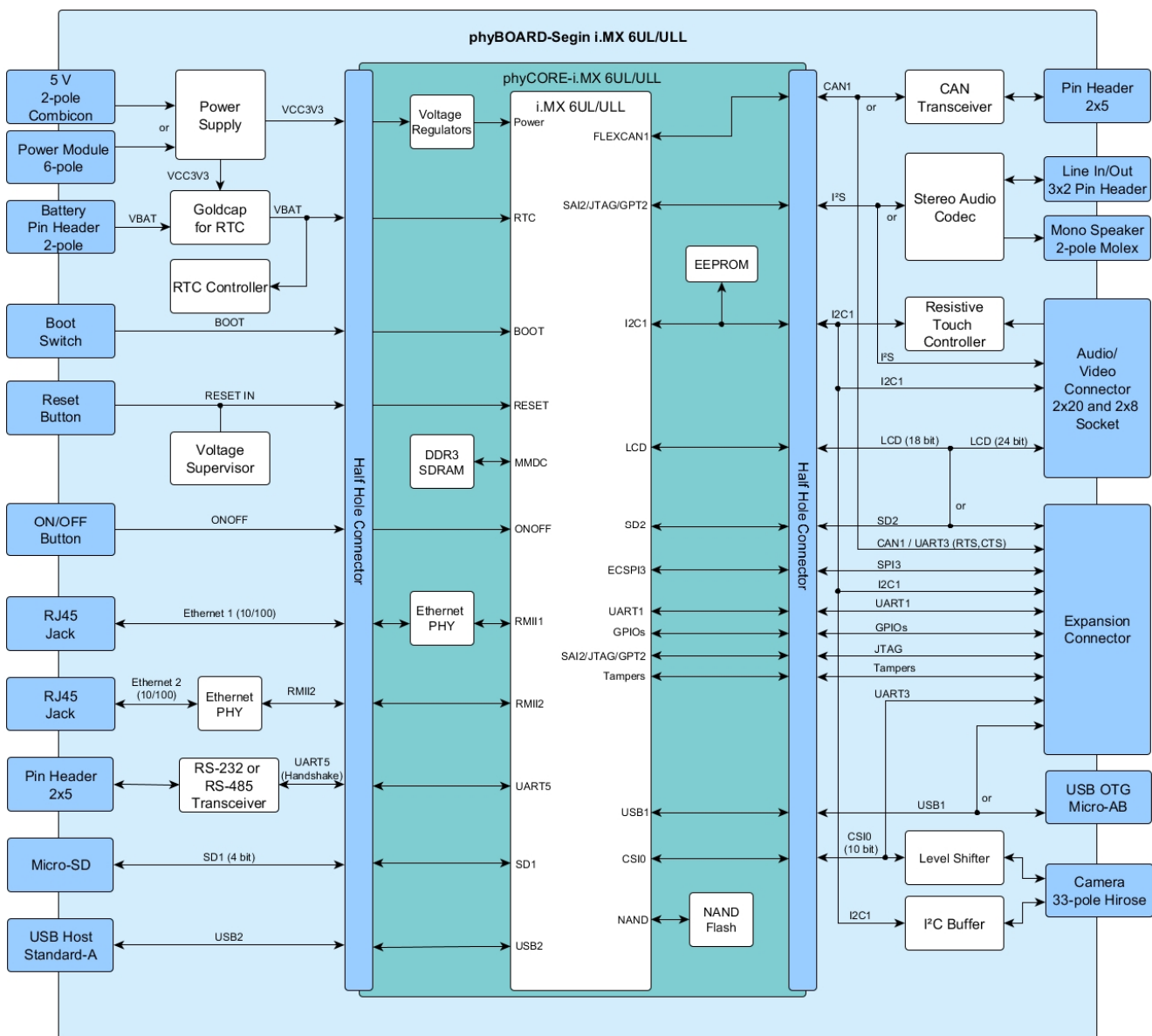
Figure 1:   Block Diagram of the phyBOARD-Segin i.MX 6UL/ULL

1.1.3 View of the phyBOARD-Segin i.MX 6UL/ULL
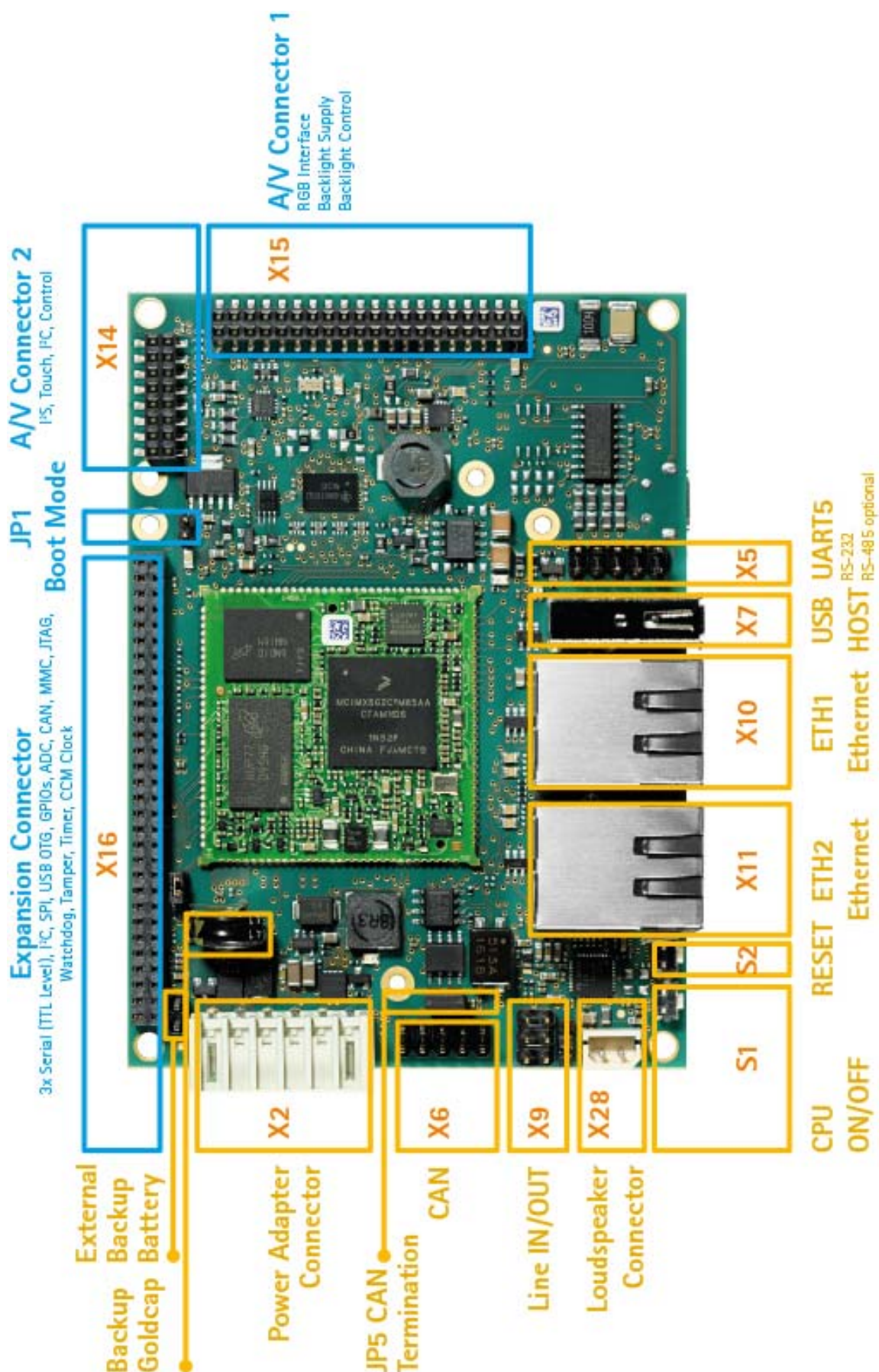
Figure 2:   View of the phyBOARD-Segin i.MX 6UL/ULL (top)
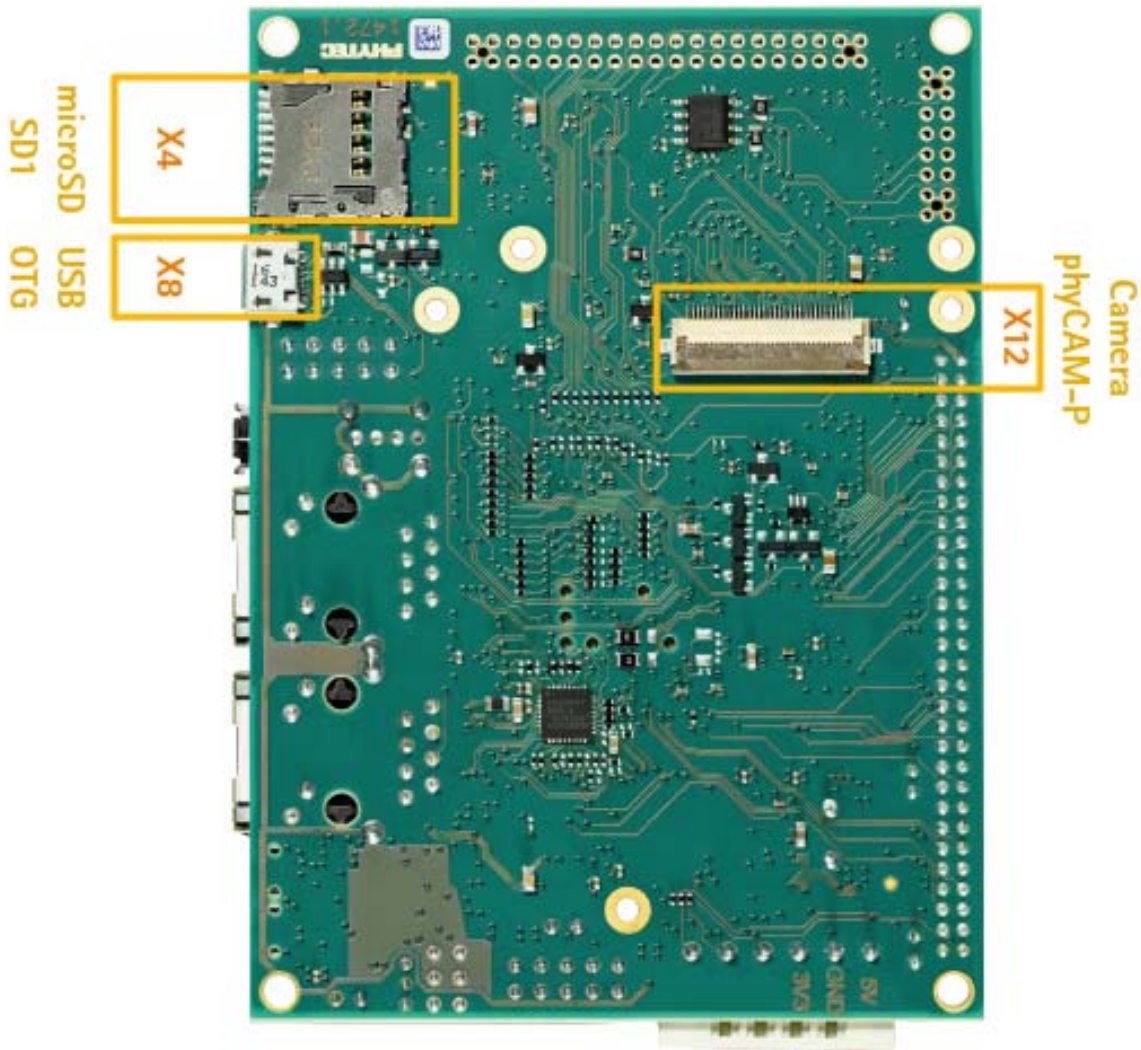
Figure 3: View of the phyBOARD-Segin i.MX 6UL/ULL (bottom)

2 Accessing the phyBOARD-Segin i.MX 6UL/ULL Features

Phytec phyBOARD-Segin i.MX 6UL/ULL is fully equipped with all mechanical and electrical components necessary for the speedy and secure start-up.

2.1 Overview of the phyBOARD-Segin i.MX 6UL/ULL Peripherals

The phyBOARD-Segin i.MX 6UL/ULL is depicted in *Figure 2*. It features many different interfaces and is equipped with the components as listed in *Table 2* to *Table 5*. For a more detailed description of each peripheral refer to the appropriate chapter listed in the applicable table. *Figure 2* and *Figure 3* highlight the location of each peripheral for easy identification.

2.1.1 Connectors and Pin Header

Table 2 lists all available connectors on the phyBOARD-Segin i.MX 6UL/ULL. *Figure 2* and *Figure 3* highlight the location of each connector for easy identification.

Reference Designator	Description	Section
X2	Power supply 5 V only (via 6-pole WAGO male header, or 2-pole Phoenix Contact MINI COMBICON base strip)	*2.2.1.1*
X3	Connector for external Backup Battery (1×2 pin header, 2.54 mm pitch)	*2.2.1.3*
X4	Secure Digital / Multi Media Card (Micro-slot)	*2.2.7*
X5	RS-232 with RTS and CTS, or RS-485 (UART5 2×5 pin header, 2.54 mm pitch)	*2.2.2*
X6	CAN connector (2×5 pin header, 2.54 mm pitch)	*2.2.6*
X7	USB host connector (USB 2.0 Standard-A)	*2.2.4*
X8	USB On-The-Go connector (USB Micro-AB)	
X9	Stereo Line Out and Line In connector (2x3 pin header, 2.54 mm pitch)	*2.2.5*
X10	Ethernet 1 connector (RJ45 with speed and link LED)	*2.2.3*
X11	Ethernet 2 connector (RJ45 with speed and link LED)	
X12	phyCAM-P camera connector (33-pin Hirose FFC-connector, 0.5 mm pitch)	*2.2.8*
X14	A/V connector #1 (2×20 dual entry connector 2 mm pitch)	*2.2.12*, *3.2.5*
X15	A/V connector #2 (2×8 dual entry connector 2 mm pitch)	
X16	Expansion connector (2×30 socket connector 2 mm pitch)	*2.2.13*, *3.2.6*
X28	Mono Speaker output (2-pole Molex SPOX 2.5 mm pitch)	*2.2.5*

Table 2:   phyBOARD-Segin i.MX 6UL/ULL Connectors and Pin Headers

	Ensure that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

2.1.2 LEDs

The phyBOARD-Segin i.MX 6UL/ULL is populated with three LEDs to indicate the status of the USB VBUS voltages, as well as of the power supply voltage.

Figure 2 shows the location of the LEDs. Their function is listed in the table below:

LED	Color	Description	Section
D8	Red	3.3 V voltage generation on the phyBOARD	*2.2.1.2*
D11	Green	Indicates presence of VBUS at the USB host interface (X7)	*2.2.4*
D12	Green	Indicates presence of VBUS at the USB OTG interface (X8)	

Table 3:   phyBOARD-Segin i.MX 6UL/ULL LEDs Descriptions

2.1.3 Buttons

The phyBOARD-Segin i.MX 6UL/ULL is populated with two push buttons, one to reset the phyBOARD and another to power on and power off the NXP® Semiconductor i.MX 6UL/ULL CPU.

Figure 2 shows the location of the switches. Their function is listed in the table below:

Switch	Description	Section
S1	i.MX 6UL/ULL ONOFF (Button) input	*2.2.10*
S2	Reset button	*2.2.11*

Table 4:   phyBOARD-Segin i.MX 6UL/ULL Buttons Description

2.1.4 Jumpers

The phyBOARD-Segin i.MX 6UL/ULL comes pre-configured with four removable jumpers (JP) and several solder jumpers (J). The jumpers allow flexible configuring of a limited number of features for development purposes to the user.

	Due to the small footprint of the solder jumpers (J) we do not recommend manual jumper modifications. This might also render the warranty invalid. Because of that only the removable jumpers are described in this section. For information on the solder jumpers see *section3.2* and contact our sales team if you need jumper configurations different from the default configuration.

The functions of the removable jumpers on the phyBOARD-Segin i.MX 6UL/ULL are shown in *Table 5*. More detailed information can be found in the appropriate section.

Figure 2 shows the location of jumper JP1 and JP5, while the location of jumpers JP2 and JP7 are shown below.
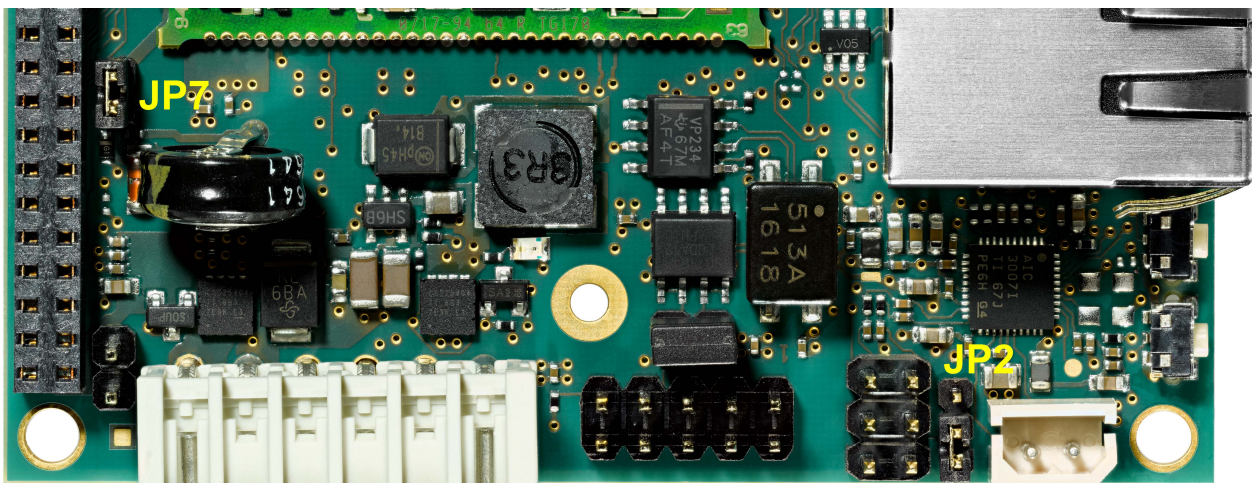
Figure 4:   Jumpers JP2 and JP7

Jumper	Description	Section
JP1	Boot Selection	*2.2.9*
JP2	JTAG Mode Selection	*2.2.5.1*, *3.2.6.1*
JP5	CAN Termination Selection	*2.2.6*
JP7	System Backup Voltage Selection	*2.2.1.3*

Table 5:   phyBOARD-Segin i.MX 6UL/ULL Jumper Description

	Detailed descriptions of the assembled connectors, jumpers and switches can be found in the following chapters.

2.2 Functional Components on the phyBOARD-Segin i.MX 6UL/ULL

This section describes the functional components of the phyBOARD-Segin i.MX 6UL/ULL. Each subsection details a particular connector/interface and associated jumpers for configuring that interface.

2.2.1 Power Supply

 Do not change modules or jumper settings while the phyBOARD is supplied with power!

2.2.1.1 Power Connectors (X2)

The phyBOARD-Segin i.MX 6UL/ULL is available with two different power supply connectors. Depending on your order you will find one of the following connectors on your SBC:

1. a 2-pole Phoenix Contact MINI COMBICON base strip 3.5 mm connector (X2) suitable for a single 5 V supply voltage, or
2. a 6-pole WAGO male header (X2) to attach the Power Module for phyBOARDs (PEB-POW-01) which provides connectivity for 12 V – 24 V

The required current load capacity for all power supply solutions depends on the specific configuration of the phyCORE mounted on the phyBOARD-Segin i.MX 6UL/ULL, the particular interfaces enabled while executing software, as well as whether an optional expansion board is connected to the carrier board.

Phoenix MINI COMBICON base strip   or   WAGO male header 6-pole

Figure 5:   Power Supply Connectors(X2), Backup Voltage Connector (X3)

2.2.1.1.1   Phoenix Contact 2-pole MINI COMBICON Base Strip (X2)

The permissible input voltage is +5 V DC if your SBC is equipped with a 2-pole Phoenix Contact MINI COMBICON base strip. A 5 V adapter with a minimum supply of 1.5 A is recommended to supply the board via the 2-pole base strip.

Figure 5 and the following table show the pin assignment.

Pin	Signal	Description
1	VCC5V	+5 V power supply
2	GND	Ground

Table 6:   Pin Assignment of the 2-pole Phoenix Contact MINI COMBICON Base Strip at X2

2.2.1.1.2   WAGO 6-pole Male Header (X2)

If a WAGO 6-pole male header is mounted on your board (*Figure 2* and *Figure 5*) your board is prepared to connect to a phyBOARD Power Module (PEB-POW-01), or a custom power supply circuitry. The ordering number of the mating connector from WAGO is:
EAN 4045454120610.

Use of the 6-pole connector has the following advantages:

* Higher and wider operate range of the input voltage
* External scaling potential to optimize the electrical output current, by use of customized power modules which match the requirements
* 5 V, 3.3 V and backlight power supply

Pin assignment of the 6–pole WAGO connector:

Pin	Signal	Description
1	VCC5V	+5 V power supply
2	GND	Ground
3	VCC3V3_PMOD	+3.3 V power supply
4	VCC_BL	Backlight power supply (input voltage of power module) [1]
5	PMOD_PWRGOOD	Power good signal (connected to reset nRESET_IN)
6	nPMOD_PWRFAIL	Power fail signal

Table 7:   Pin Assignment of the 6-pole WAGO Connector at X2

1:    The voltage level depends on the connected power module and the voltage attached, and is thus not specified here.

A detailed description of the Power Module for phyBOARDs including information on the minimum supply current can be found in the Application Guide for phyBOARD Expansion Boards (L-793e).

2.2.1.2 Power LED D8

The red LED D8 next to power connector X2 (*Figure 2*) indicates the presence of the 3.3 V supply voltage generated from the 5 V input voltage.
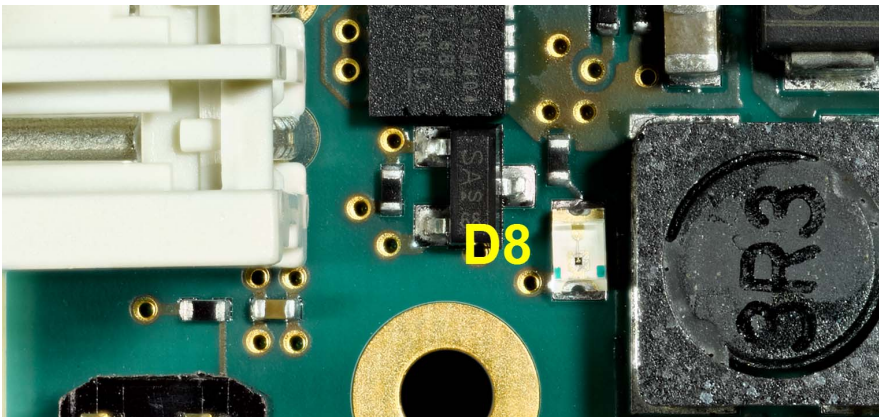
Figure 6:   Power Supply LED D8

2.2.1.3 Backup Voltage, RTC and X3

The phyBOARD-Segin i.MX 6UL/ULL features an external RTC at U2 in addition to the internal RTC of i.MX 6UL/ULL processor. They are used for real-time or time-driven applications. To backup the RTCs a Goldcap (C1) (*Figure 2*) is placed on the phyBOARD. Alternatively the 2-pole pin header X3 can be used to connect an external battery (max. 3.6 V) to VCC_BACKUP to feed in the backup voltage.

Figure 5 and the following table show the pin assignment of X3.

Pin	Signal	Description
1	VCC_BACKUP	Backup battery voltage
2	GND	Ground

Table 8:   Pinout of the 2-pole Pin Header X3

The backup voltage source (either Gold cap at C1, or external battery via X3) supplies the external RTC at U2.

Closing jumper JP7 connects the backup voltage source also to the backup voltage domain VDD_SNVS of the i.MX 6UL/ULL which supplies the RTC and some critical registers when the primary system power, VCC5V, is removed. The backup supply for only the RTC at U2 (jumper JP7 open) lasts approximately 11½ days.

2.2.2 UART Connectivity (X16 and X5)

The phyCORE-i.MX 6UL\ULL provides up to 3 high speed universal asynchronous interfaces. On the phyBOARD TTL level signals of UART1 (the standard console) and UART3[2] are routed to expansion connector X16. UART5 is available at pin header connector X5 at RS-232 level, or optionally at RS-485 level[3].

	The Evaluation Board (PEB-EVAL-01) delivered with the kit plugs into the expansion connector and allows easy use of the standard console (UART1) which is required for debugging. Please find additional information on the Evaluation Board in Application Guide for phyBOARD Expansion Boards (L-793e).

Further information on the expansion connector can be found in *section 3.2.6.*

Pin header connector X5 is located next to the USB host connector (*Figure 2)* and provides the UART5 signals of the i.MX 6UL/ULL at RS-232, or RS-485 level. The serial interface is intended to be used as data terminal equipment (DTE) and allows for a 5-wire connection including the signals RTS and CTS for hardware flow control. *Table 9* shows the signal mapping of the RS-232 and RS-485 level signals at connector X5.
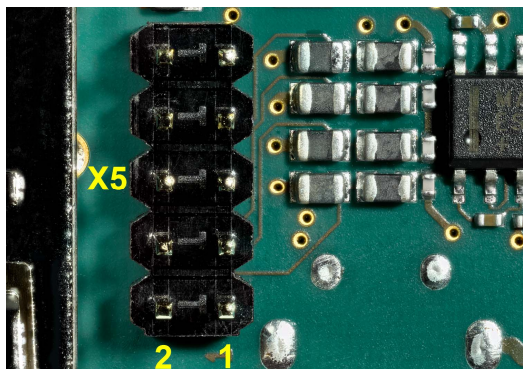
Figure 7:   *RS-232 or RS-485 Interface Connector X5*

Pin	Signal	Pin	Signal
1	NC	2	NC
3	X_UART5_RXD_RS232	4	X_UART5_RTS_RS232
5	X_UART5_TXD_RS232	6	X_UART5_CTS_RS232
7	X_UART5_RS485_A[3]	8	X_UART5_RS485_B[3]
9	GND	10	NC

Table 9:   *Pin Assignment of RS-232 /RS-485 Interface Connector X5*

2:   Usually UART3 is not available, as the signals are routed to the phyCAM-P interface via jumpers J3 and J4. If UART3 is needed at expansion connector X16 the jumpers as well as the BSP must be changed.
3:   The standard kit comes with an RS-232 transceiver installed, if you need an RS-485 interface at X5 instead, please contact our sales team.

An adapter cable is included in the phyBOARD-Segin i.MX 6UL/ULL Kit to facilitate the use of the UART5 interface. The following figure shows the signal mapping of the adapter.

Pin 2:	RxD-RS232
Pin 7:	RTS-RS232
Pin 3:	TxD-RS232
Pin 8:	CTS-RS232
Pin 4:	A-RS485[3]
Pin 9:	B-RS485[3]
Pin 5:	GND
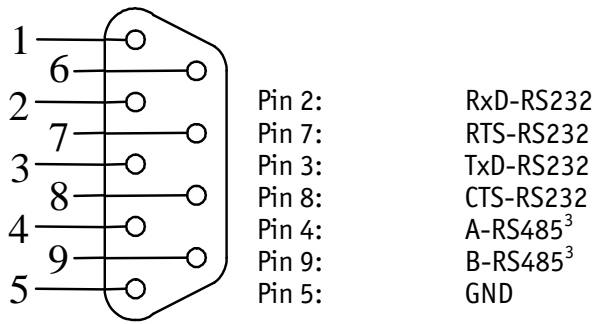
Figure 8:   RS-232 / RS-485 Connector Signal Mapping

2.2.3 Ethernet Connectivity (X10 and X11)

The Ethernet interfaces of the phyBOARD-Segin i.MX 6UL/ULL are accessible at two RJ45 connectors X10 (Ethernet 1) and X11 (Ethernet 2).

Figure 9:   Ethernet Interfaces at Connectors X10 and X11

Ethernet 1 is directly brought out from the SOM's Ethernet interface ENET1, whereas Ethernet 2 is made available by a an Ethernet PHY at U3 on the phyBOARD. The Ethernet PHY is connected to the SOM's RMII interface ENET2.

Both Ethernet interfaces are configured as 10/100Base-T networks. The LEDs for LINK (green) and SPEED (yellow) indication are integrated in the connector. Both Ethernet transceivers support HP Auto-MDIX, eliminating the need for the consideration of a direct connect LAN cable, or a cross-over path cable. They detect the TX and RX pins of the connected device and automatically configure the PHY TX and RX pins accordingly.

2.2.3.1 MAC Address

In a computer network such as a local area network (LAN), the MAC (Media Access Control) address is a unique computer hardware number. For a connection to the Internet, a table is used to convert the assigned IP number to the hardware's MAC address.

In order to guarantee that the MAC address is unique, all addresses are managed in a central location. Phytec has acquired a pool of MAC addresses. The MAC address of the phyBOARD-Segin i.MX 6UL/ULL is located on the bar code sticker attached to the module. This number is a 12-digit HEX value.

2.2.4 USB Connectivity (X7 and X8)

The phyBOARD-Segin i.MX 6UL/ULL provides one USB host and one USB OTG interface.

USB1 is accessible at connector X8 (USB Micro-AB) located at the back side of the phyBOARD. It is configured as USB OTG. USB OTG devices are capable to initiate a session, control the connection and exchange host and peripheral roles between each other. This interface is compliant with USB revision 2.0.

USB2 is accessible on the top of the phyBOARD at connector X7 (USB Standard-A) and is configured as USB host.
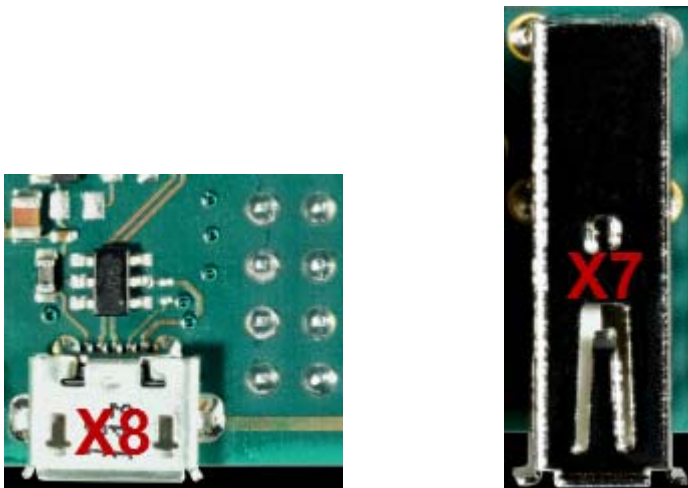
Figure 10:   USB Interfaces Connectors X8 and X7

LED D12 displays the status of USB_OTG1_VBUS and LED D11 indicates the status of X_USB_OTG2_VBUS (*Figure 11*).
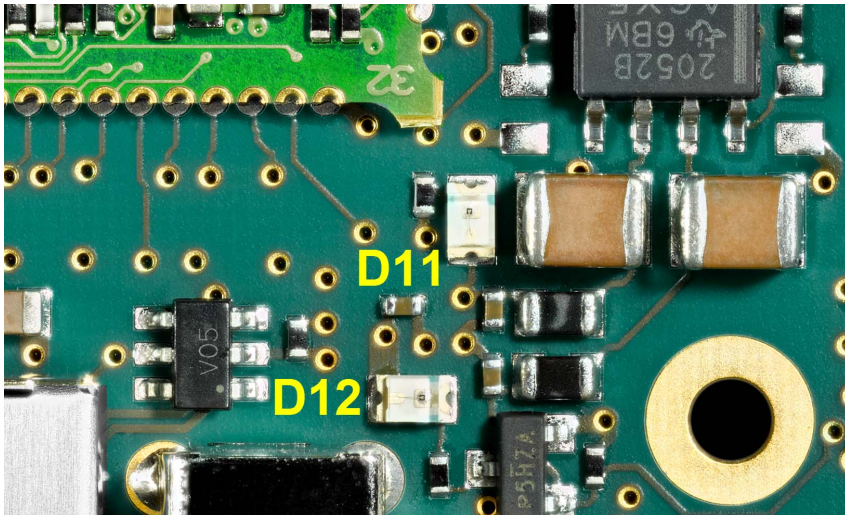
Figure 11:   USB Host and OTG LEDs

Two jumpers and a resistor allow to configure the USB1 interface according to your needs. Please refer to *section 3.2.6.3* for more information.

2.2.5 Audio Interface (X28 and X9)

The audio interface provides a method of exploring i.MX 6UL/ULL's audio capabilities. The phyBOARD-Segin i.MX 6UL/ULL is populated with an audio codec at U8. The audio codec is connected to the i.MX 6UL/ULL's SAI interface to support stereo line input and stereo line output at connector X9. In addition to that the phyBOARD-Segin i.MX 6UL/ULL has one direct mono speaker output (1 W) at Molex connector X28.
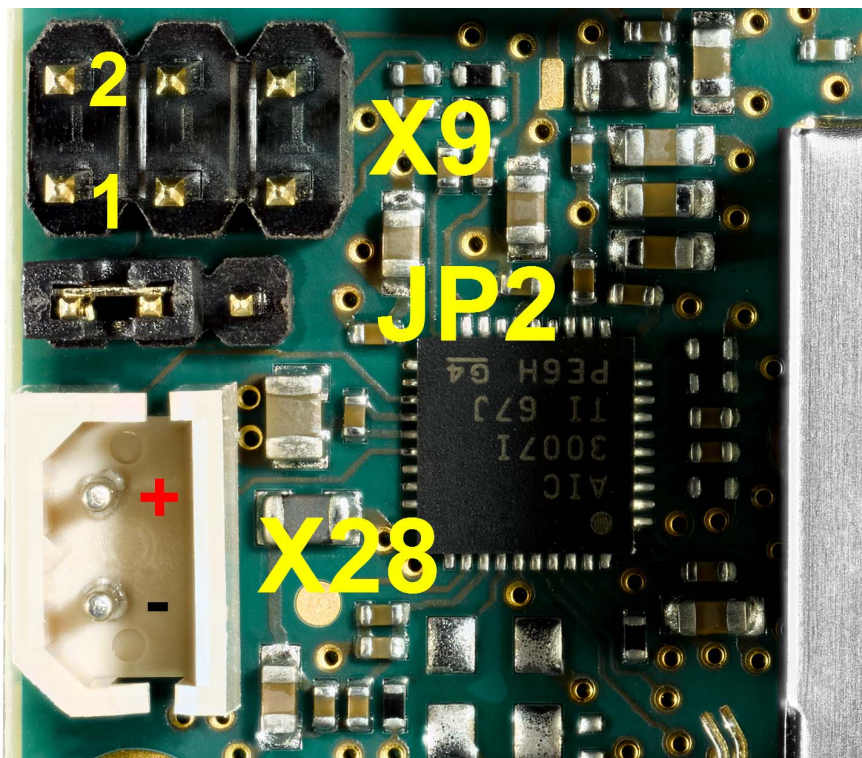
Figure 12:   Audio Interfaces at Connectors (X28 and X9)

Pin	Signal	Pin	Signal
1	LINE_IN_L	2	LINE_IN_R
3	AGND	4	AGND
5	LINE_OUT_L	6	LINE_OUT_R

Table 10:   Pin Assignment of Audio Connector X9

Pin	Signal	Description
1	SPOP	Class-D positive differential output
2	SPOM	Class-D negative differential output

Table 11:   Pin Assignment of Audio Connector X28

The audio codec can be configured via I²C interface I2C1 at address 0x18.

For additional audio applications the SAI interface of the i.MX 6UL/ULL including the signals X_JTAG_TDI/SAI2_BCLK, X_JTAG_TDO/SAI2_SYNC, X_JTAG_TCK/SAI2_RXD and X_JTAG_nTRST/SAI2_TXD are routed to A/V connector X15 (please refer to *section 3.2.5* for additional information on the A/V connector).

Please refer to the audio codec's reference manual for additional information regarding the special interface specification.

2.2.5.1 Disabling the Audio Codec

Jumper JP2 allows disabling the audio codec. This is necessary if the JTAG interface at expansion connector X16 is required during development (*3.2.6.1*)

If the audio codec is to be used in normal operation ensure that jumper JP2 is set to 1+2 which connects the audio codec's reset input to X_nRESET_OUT.

The location of JP2 is shown in *Figure 23.*

Mode Selection	Description
Audio reset signal (JP2 = 1+2)	Audio codec normal operation
JTAG mode (JP2 = 2+3)	Audio codec disabled, JTAG interface can be used

Table 12:   Audio Codec Disable Jumper JP2[4]

4:     Default settings are in **bold blue** text

2.2.6 CAN Connectivity (X6, JP5)

The Controller Area Network (CAN) bus offers a low-bandwidth, prioritized message fieldbus for serial communication between microcontrollers. It efficiently supports distributed real time control with a high level of security. The Flexible Controller Area Network (FLEXCAN) module of the iMX 6UL/ULL is a full implementation of the CAN protocol specification version 2.0B. It supports standard and extended message frames and supports bitrates up to 1 Mbit/s.

Note:
The CAN interface is not available on the processor type -G0 and -Y0.

The first interface (FLEXCAN1) of the Flexible Controller Area Network is accessible at connector X6 (2×5 pin header, 2.54 mm pitch).

Jumper JP5 can be installed to add a 120 Ohm termination resistor across the CAN data lines if needed.
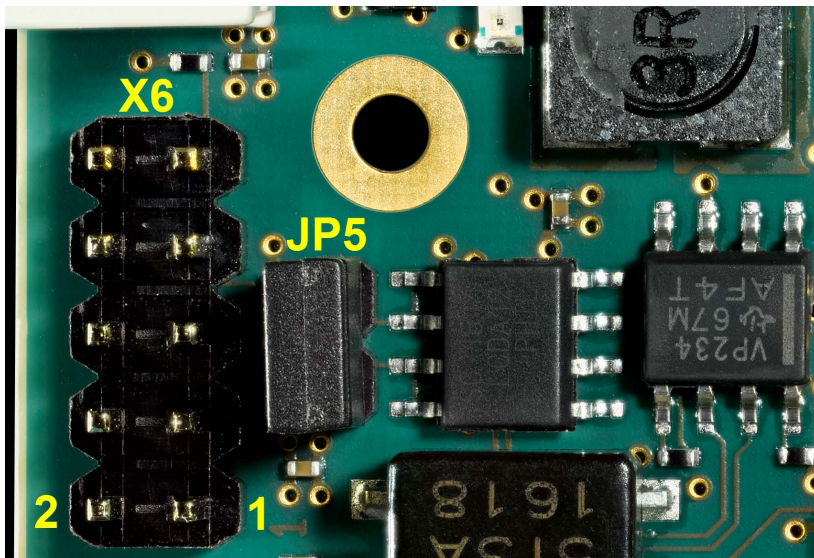
Figure 13:   Components supporting the CAN Interface(X6, JP5)

Table 13 below shows the signal mapping of the CAN1 signals at connector X6.

Pin	Signal	Pin	Signal
1	NC	2	GND
3	X_CANL	4	X_CANH
5	GND	6	NC
7	NC	8	NC
9	Shield	10	NC

Table 13:   Pin Assignment of CAN Connector X6

An adapter cable is included in the phyBOARD-Segin i.MX 6UL/ULL Kit to facilitate the use of the CAN interface. The following figure shows the signal mapping of the adapter.

Pin 6:	GND
Pin 2:	X_CANL
Pin 7:	X_CANH
Pin 3:	GND
Pin 5:	Shield
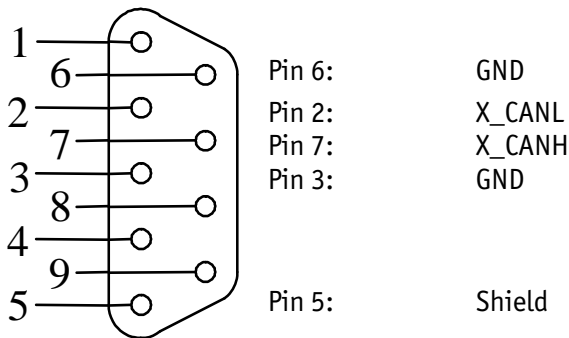
Figure 14:   CAN Connector Signal Mapping

As an alternative option the TTL level signals of FLEXCAN1 can be also routed to expansion connector X16, and, depending on the muxing options, a second CAN interface (FLEXCAN2) is available at the expansion connector, too (*3.2.6.1.2*).

2.2.7 Secure Digital Memory Card/MultiMedia Card (X4)

Figure 15:   SD/MM Card Interface at Connector X4 (back side)

The phyBOARD-Segin i.MX 6UL/ULL provides a standard microSDHC card slot at X4 for connection to MMC/SD interface cards. It allows easy and convenient connection to peripheral devices such as SD- and MMC cards. Power to the SD interface is supplied by inserting the appropriate card into the MMC/SD connector, which features card detection, a lock mechanism and a smooth extraction function by Push-in/Push-out of card.

Insertable jumper JP1 allows to toggle between NAND boot and boot from SD card. In order to boot from SD card, JP1 must be set to change the boot configuration (*section 2.2.9*).

2.2.8 Camera Connectivity (X12)

The phyCORE module on the phyBOARD-Segin i.MX 6UL/ULL offers one interfaces to connect digital cameras[5]. The signals of the parallel CMOS Sensor Interface (CSI) are available as 10-bit parallel camera interface together with an I^2C interface to allow for direct connection of CMOS camera modules.

Generally, the parallel port can be expanded on the carrier board in three ways:
1. according to the phyCAM-P camera interface standard
2. according to the as phyCAM-S+ camera interface standard
3. as interface for customer parallel cameras

On the phyBOARD-Segin i.MX 6UL/ULL the 10-bit parallel CMOS Serial Interface is brought out as phyCAM-P camera interface at connector X12 (*Figure 17*). Information on the phyCAM-P standard and the other possibilities can be found in the phyCAM-manual (L-748).
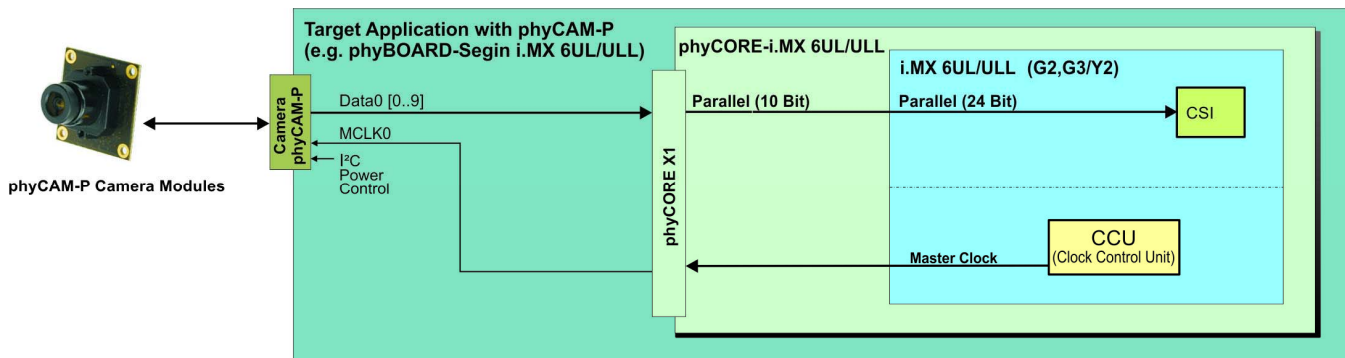
Figure 16:   phyCAM-P Camera Interface on the phyBOARD-Segin i.MX 6UL/ULL

Figure 17:   Camera Interface (phyCAM-P) at Connector X12

5:    Only the i.MX 6UL/ULL microcontrollers version Y2, G2 and G3 are equipped with one parallel CMOS Sensor Interface (CSI) to process the signals from the parallel camera interface.

The table below shows the pinout of connector X12.

Pin #	Signal Name	Description
1,2,32,33	VCC_CAM	Power Supply
3	VSR_VCCCAM	Power Voltage Set
4	CAM_CTRL2	Control Signal 2
5	CAM_MCLK	Camera Master Clock
6,8,11,14,17,20,23,26,30	GND	Ground
7	CAM_PCLK	Camera Pixel Clock
9	CAM_DD0	Camera Signal 0
10	CAM_DD1	Camera Signal 1
12	CAM_DD2	Camera Signal 2
13	CAM_DD3	Camera Signal 3
15	CAM_DD4	Camera Signal 4
16	CAM_DD5	Camera Signal 5
18	CAM_DD6	Camera Signal 6
19	CAM_DD7	Camera Signal 7
21	CAM_DD8	Camera Signal 8
22	CAM_DD9	Camera Signal 9
24	CAM_LV	Camera HSYNC Signal
25	CAM_FV	Camera VSYNC Signal
27	CAM_CTRL1	Control signal 1
28	CAM_I2C_SCL	I^2C clock Signal
29	CAM_I2C_SDA	I^2C data Signal
31	nCAM_RST	Camera reset signal

Table 14:   Phytec Camera Connector X12

2.2.9 Boot Mode (JP1)

The pyhBOARD-Segin i.MX 6UL/ULL has two defined boot sequence which can be selected by configuring jumper JP1.
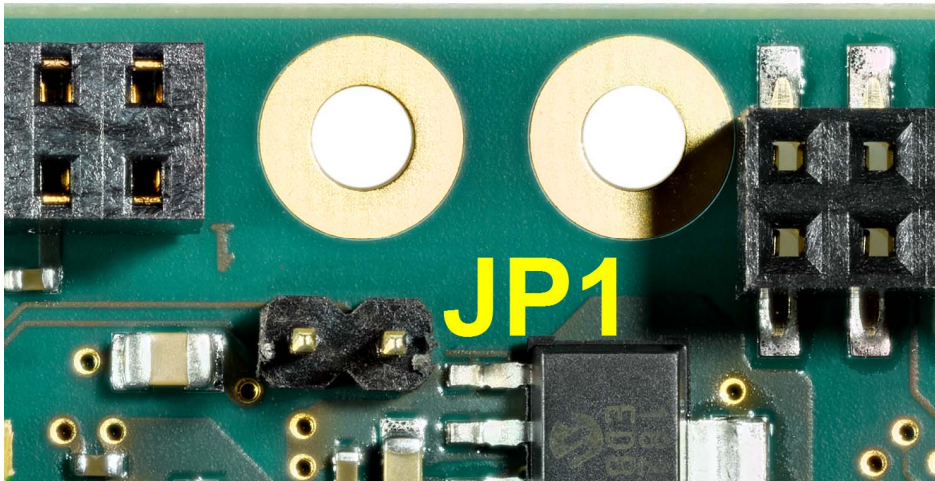
Figure 18:   Boot Mode Selection Jumper JP1

Boot Mode	Description
Boot mode 1 (JP1 = open)	Boot from NAND
Boot mode 2 (JP1 = closed)	Boot from SD/MMC 1

Table 15:   Boot Jumper Configuration JP1

2.2.10 CPU ON/OFF Button (S1)

The phyBOARD-Segin i.MX 6UL/ULL is equipped with a CPU ON/OFF button at S1. Pressing this button will toggle the X_ONOFF signal (pin X1-99) of the phyCORE SOM low, causing the i.MX 6UL/ULL CPU to power off. Pressing S1 for about 5 seconds turns off the phyBOARD. Please refer to the i.MX 6UL/ULL Reference Manual for more information on the ONOFF (Button) input.
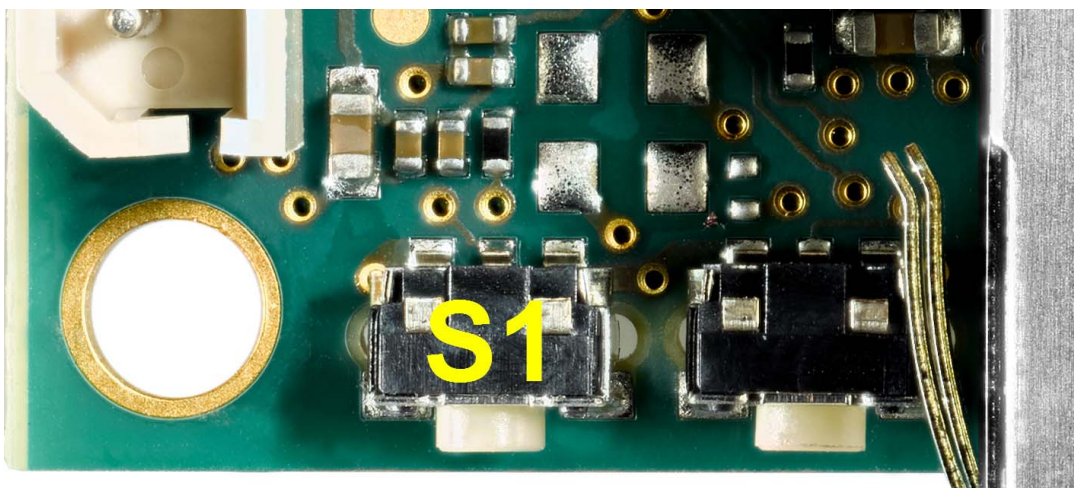
Figure 19:   CPU ON/OFF Button S1

2.2.11   System Reset Button (S2)

The phyBOARD-Segin i.MX 6UL/ULL is equipped with a system reset button at S2. Pressing this button will toggle the X_nRESET_IN pin (X1-100) of the phyCORE SOM low, causing the module to reset. Additionally, the reset signal X_nRESET_OUT is generated on the module (X1-98) to also reset the peripherals on the carrier board.
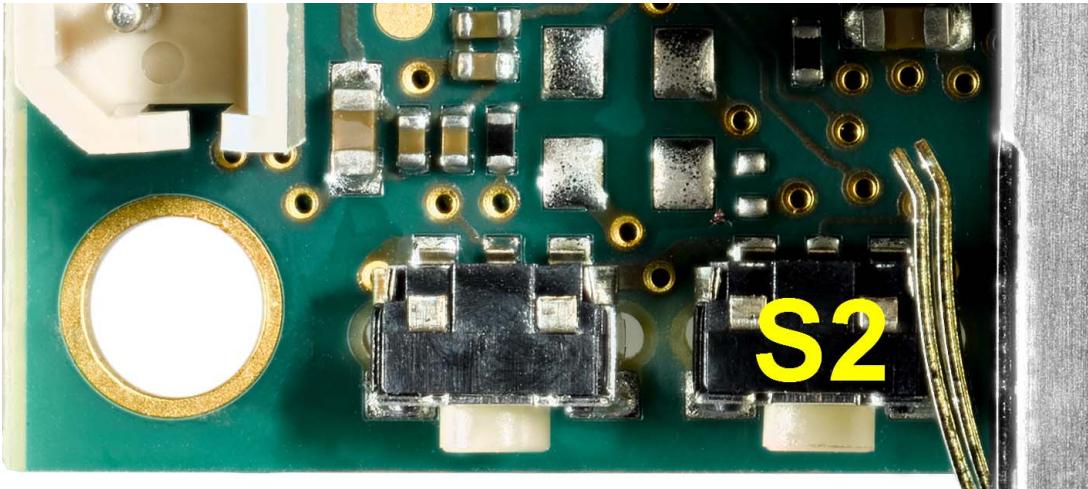
Figure 20:   System Reset Button S2

2.2.12   Audio/Video connectors (X14 and X15)

The Audio/Video (A/V) connectors X14 and X15 provide an easy way to add typical A/V functions and features to the phyBOARD-Segin i.MX 6UL/ULL. Standard interfaces such as parallel display, I^2S and I^2C as well as different supply voltages are available at the two A/V female dual entry connectors. Special feature of these connectors are their connectivity from the bottom or the top of the PCB.

For further information of the A/V connectors see *chapter 3.2.5*. Information on the expansion boards available for the A/V Connectors can be found in the Application Guide for phyBOARD Expansion Boards (L-793e).

2.2.13   Expansion connector (X16)

Expansion connector X16 provides an easy way to add other functions and features to the phyBOARD-Segin i.MX 6UL/ULL. Standard interfaces such as JTAG, UART, MMC, SPI and I^2C as well as different supply voltages and some GPIOs are available at the expansion female connector.

For further information of the expansion connector and the pinout see *chapter 3.2.6*. Information on the expansion boards available for the expansion connector can be found in the Application Guide for phyBOARD Expansion Boards (L-793e).

3   System Level Customizing

3.1 About this Section

This section addresses advanced developers who want to design custom expansion boards, or display adapters. It includes detailed information on the different interfaces and features of the phyBOARD-Segin i.MX 6UL/ULL at a system level.

3.2 System Level Hardware Information

3.2.1 Differences in SOM Pinout

To support all features of the phyBOARD-Segin i.MX 6UL/ULL the BSP provided assigns functions different from what is described in the pinout table (chapter 2) of the phyCORE-i.MX 6UL/ULL hardware manual to some pins of the phyCORE-AM335x R2. *Table 16* lists all pins with functions different from what is described in the SOM's pinout table.

> **Note:**
> The information given in the "TYPE" column is from the SOM's perspective.

Pin#	Signal	Type	SL	Description
44	X_LCD_D18	I/O	3.3 V	DISP data 18 is multiplexed for uSDHC2 command on expansion connector X16
45	X_LCD_D19	I/O	3.3 V	DISP data 19 is multiplexed for uSDHC2 clock on expansion connector X16
46	X_LCD_D20	I/O	3.3 V	DISP data 20 is multiplexed for uSDHC2 data 0 on expansion connector X16
47	X_LCD_D21	I/O	3.3 V	DISP data 21 is multiplexed for uSDHC2 data 1 on expansion connector X16
48	X_LCD_D22	I/O	3.3 V	DISP data 22 is multiplexed for uSDHC2 data 2 on expansion connector X16
49	X_LCD_D23	I/O	3.3 V	DISP data 23 is multiplexed for uSDHC2 data 3 on expansion connector X16
78	X_GPIO1_3	I	3.3 V	ADC input 3 available on expansion connector X16
87	X_GPIO5_1	I	3.3 V	External RTC interrupt available on expansion connector X16
88	X_GPIO5_0	I	3.3 V	Tamper pin on expansion connector X16
95	X_GPIO5_5	I	3.3 V	Interrupt for AV adapter
96	X_GPIO1_1	O	3.3 V	Watchdog signal available on expansion connector X16

Table 16:   Specifically used Pins on the phyCORE-Connector

3.2.2 Soldering Jumpers

Numerous jumpers and 0 Ohm resistors allow configuring the phyBOARD according to your needs.

	Due to the small footprint of the jumpers we do not recommend manual jumper modifications. This might also render the warranty invalid. Please contact our sales team if you need one of the configurations described below.

The following table lists all jumpers and resistors, and describes their function.

Jumper / Resistor	Description	Section
J1, J2	Rerouting the CAN interface to expansion connector X16	*3.2.6.1*
J3 – J4	Rerouting the UART3 interface to expansion connector X16	*3.2.6.2.3*
J5 – J10	Adding LCD interface data lines D18 to D23 to the parallel LCD interface on A/V connector X14	*3.2.5.1.1*
J11	Selecting the reset signal at pin 8 of A/V connector X15	*3.2.5.1.2*
J13, J14	Rerouting the USB OTG1 interface to expansion connector X16	*3.2.6.3*
R34	Configuring the operation mode for the USB OTG interface	*3.2.6.3.1*
J17	Connecting AGND and GND via a star point jumper	
J18	Changing the I^2C address of the touchscreen controller ABA_U1	*3.2.3*
J19, J20	Configuring the phyCAM-P control signals X_CAM_CTRL1 and X_CAM_CTRL2	*3.2.4.1*
J21	Disabling the phyCAM-P bus transceiver output	*3.2.4.2*
J22	Selecting phyCAM-P reset input signal nCAM_RST	*3.2.4.3*

Table 17:   Soldering Jumpers on the phyBOARD-Segin i.MX 6UL/ULL

3.2.3 I²C Connectivity

The I2C1 interface of the i.MX 6UL/ULL is available at different connectors on the phyBOARD-Segin i.MX 6UL/ULL. The following table provides a list of the connectors and pins with I²C connectivity.

Connector	Location
Expansion connector X16	pin 11 (I2C1_SDA), pin 13 (I2C1_SCL)
A/V connector X15	pin 16 (I2C1_SDA), pin 15 (I2C1_SCL)

Table 18:   I2C1 Connectivity

To avoid any conflicts when connecting external I²C devices to the phyBOARD-Segin i.MX 6UL/ULL the addresses of the on-board I²C devices must be considered. *Table 19* lists the addresses already in use. The table shows only the default address.

Board	Prod. No.	Device	Address used (7 MSB)
I2C1			
phyCORE-i.MX 6UL/ULL	PCL–063	EEPROM	0x52, 0x5A
phyBOARD-Segin i.MX 6UL/ULL	PBA-CD-10	Touch controller	0x44
		Stereo Audio Codec	0x18
		RTC	0x68
		phyCAM-P	0x45, 0x48, 0x5D
AV-Adapter HDMI	PEB-AV-01	HDMI Core	0x70
		CEC Core	0x34
AV-Adapter Display	PEB-AV-02	GPIO Expander	0x41
Evaluation Board	PEB-EVAL-01	EEPROM	0x56
M2M Board	PEB-C-01	GPIO Expander	0x20
		GPIO Expander	0x21
		GPIO Expander	0x22

Table 19:   I²C Addresses in Use

3.2.4 phyCAM-P Interface Configuration

Numerous jumpers allow configuring the phyCAM-P interfaces according to your needs.

3.2.4.1 Configuring the CAM_CTRL Signals J19, J20

The different phyCAM-P camera modules offer various additional features such as I^2C address selection, strobe output, or trigger input to name a few. These are available via the CAM_CTRLx I/O pins. Jumpers J19 and J20 allow configuring the CAM_CTRLx I/Os according to the phyCAM-P camera module connected to X12.

The following configurations are possibel:

		Description
J19	1+2	CAM_CTRL1 connected to VCC_CAM
	2+3	**CAM_CTRL1 connected to GND**
	2+4	CAM_CTRL1connected to the phyCAM-P bus transceiver
J20	1+2	CAM_CTRL2 connected to VCC_CAM
	2+3	CAM_CTRL2 connected to GND
	2+4	**CAM_CTRL2connected to the phyCAM-P bus transceiver**

Table 20:   CAM_CTRLx Signal Configuration J19, J20[6]

For more information on possible configurations with the CAM_CTRLx signals refer also to the documentation delivered with the camera module (*L-748d*).

3.2.4.2 Disabling the phyCAM-P Bus Transceiver J21

Jumper J21 allows disabling the phyCAM-P bus transceiver at U6. Closing J21 at 2+3 places both output ports of the transceiver into high-impedance mode.

J21	Description
1+2	**phyCAM-P bus transceiver at U6 enabled**
2+3	output ports of phyCAM-P bus transceiver in high-impedance mode

Table 21:   Disabling the phyCAM-P Bus Transceiver J21[6]

3.2.4.3 Configuring the Reset Signal J22

The reset signal nCAM_RST at the X12 can be configured with J22. In the default configuration (J22 closed at 1+2) nCAM_RST is connected with the system reset signal X_nRESET_OUT.

6:      Default settings are in **bold blue** text

3.2.5 Audio/Video Connectors (X14 and X15)

Audio/Video (A/V) connectors X14 and X15 provide an easy way to add typical A/V functions and features to the phyBOARD-Segin i.MX 6UL/ULL. Standard interfaces such as parallel display, I^{2}S and I^{2}C as well as different supply voltages are available at the two A/V female dual entry connectors. Special feature of these connectors are their connectivity from the bottom or the top. The pinout of the A/V connectors is shown in *Table 22* and *Table 23*.

The A/V connector is intended for use with phyBOARD Expansion Boards[7], and to add specific audio/video connectivity with custom expansion boards.
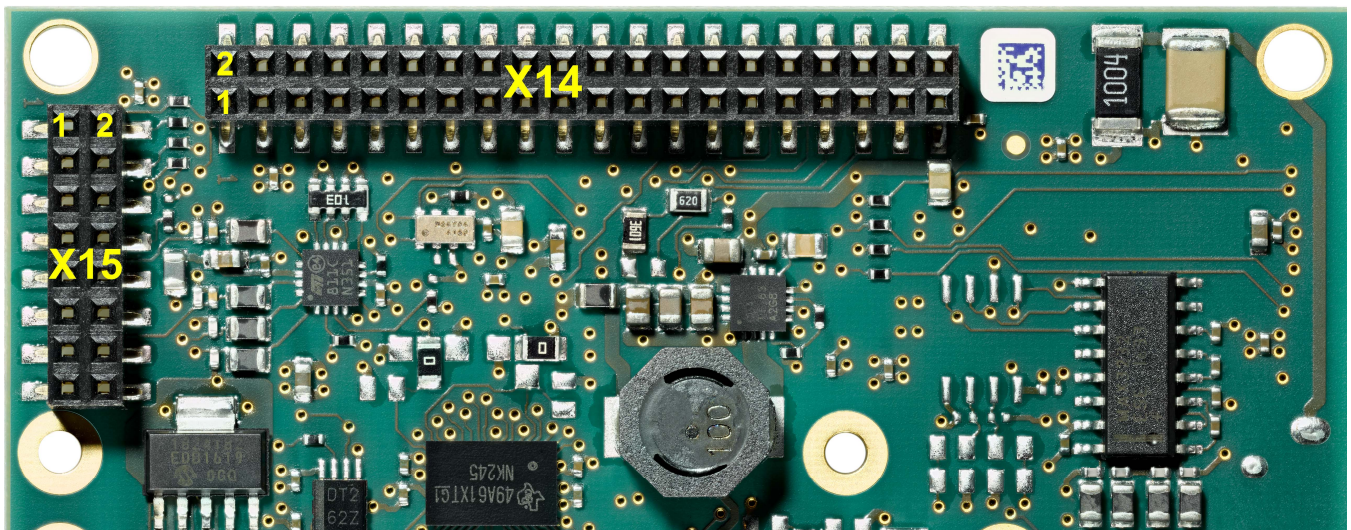
Figure 21:   Audio/Video Connectors (X14 and X15)

A/V connector X15 makes all signals for display connectivity available, while X14 provides signals for audio and touch screen connectivity, as well as an I^{2}C bus and additional control signals.

7:    Please find additional information on phyBOARD Expansion Boards in the corresponding application guide (L-793e).

Pin #	Signal Name	Type	SL	Description
1	GND	-	-	Ground
2	X_LCD_D22_AV	OUT	3.3V	LCD data 22[8]
3	X_LCD_D23_AV	OUT	3.3 V	LCD data 23[8]
4	X_LCD_D12	OUT	3.3 V	LCD data 12
5	X_LCD_D13	OUT	3.3 V	LCD data 13
6	GND	-	-	Ground
7	X_LCD_D14	OUT	3.3 V	LCD data 14
8	X_LCD_D15	OUT	3.3 V	LCD data 15
9	X_LCD_D16	OUT	3.3 V	LCD data 16
10	X_LCD_D17	OUT	3.3 V	LCD data 17
11	GND	-	-	Ground
12	X_LCD_D20_AV	OUT	3.3 V	LCD data 20[8]
13	X_LCD_D21_AV	OUT	3.3 V	LCD data 21[8]
14	X_LCD_D6	OUT	3.3 V	LCD data 6
15	X_LCD_D7	OUT	3.3 V	LCD data 7
16	GND	-	-	Ground
17	X_LCD_D8	OUT	3.3 V	LCD data 8
18	X_LCD_D9	OUT	3.3 V	LCD data 9
19	X_LCD_D10	OUT	3.3 V	LCD data 10
20	X_LCD_D11	OUT	3.3 V	LCD data 11
21	GND	-	-	Ground
22	X_LCD_D18_AV	OUT	3.3 V	LCD data 18[8]
23	X_LCD_D19_AV	OUT	3.3 V	LCD data 19[8]
24	X_LCD_D0	OUT	3.3 V	LCD data 00
25	X_LCD_D1	OUT	3.3 V	LCD data 01
26	GND	-	-	Ground
27	X_LCD_D2	OUT	3.3 V	LCD data 02
28	X_LCD_D3	OUT	3.3 V	LCD data 03
29	X_LCD_D4	OUT	3.3 V	LCD data 04
30	X_LCD_D5	OUT	3.3 V	LCD data 05
31	GND	-	-	Ground
32	X_LCD_CLK	OUT	3.3 V	LCD pixel clock
33	X_LCD_ENABLE	OUT	3.3 V	LCD enable

Table 22:   Phytec A/V Connector X14

8: In the default configuration of the phyBOARD-Segin i.MX 6UL/ULL the corresponding controller outputs of these signals are muxed as SD card interface signals SD2 and are routed to expansion connector X16 via jumpers J5 to J10. Hence the standard configuration of the module provides only an LCD display interface with 18-bit bus width at A/V connector X14.

Pin #	Signal Name	Type	SL	Description
34	X_LCD_HSYNC	OUT	3.3 V	LCD horizontal synchronization
35	X_LCD_VSYNC	OUT	3.3 V	LCD vertical synchronization
36	GND	-	-	Ground
37	GND	-	-	Ground
38	X_GPIO1_4/PWM3	OUT	3.3 V	Pulse width modulation
39	VCC_BL	OUT	NS[9]	Backlight power supply
40	VCC5V	OUT	5.0 V	5.0 V power supply

Table 22:   Phytec A/V Connector X14 (continued)

Caution!

Please consider that the LCD data signals shown in Table 22 are boot configuration pins which must not be driven by any device on the baseboard during reset, to avoid accidental change of the boot configuration. Please refer to *section 6 "System Configuration and Booting"* in the phyCORE-i.MX 6UL/ULL hardware manual, or to the i.MX 6UL/ULL Reference Manual for more information about the boot configuration.

Pin #	Signal Name	Type	SL	Description	
1	X_SAI2_BCLK	OUT	3.3 V	SAI2 transmit bit clock	
2	X_SAI2_SYNC	OUT	3.3 V	SAI2 transmit frame sync.	
3	X_SAI2_RXD	IN	3.3 V	SAI2 receive data	
4	X_SAI2_TXD	OUT	3.3 V	SAI2 transmit data	
5	X_AV_INT	I/O	3.3 V	A/V interrupt; GPIO5_5[10]	
6	X_GPIO1_18	OUT	3.3 V	LCD control; GPIO1_18	
7	GND	-	-	Ground	
8	X_nRESET_OUT	OUT	3.3 V	Reset	(J11 1+2)
	X_LCD_RESET	OUT	3.3 V	Reset LCD	(**J11 2+3**)
9	TS_X+	IN	1.8 V	Touch X+	
10	TS_X-	IN	1.8 V	Touch X-	
11	TS_Y+	IN	1.8 V	Touch Y+	
12	TS_Y-	IN	1.8 V	Touch Y-	
13	VCC3V3	OUT	3.3 V	3.3 V power supply	
14	GND	-	-	Ground	
15	X_I2C1_SCL	I/O	3.3 V	I2C1 clock	
16	X_I2C1_SDA	I/O	3.3 V	I2C1 data	

Table 23:   Phytec A/V connector X15

9:    VCC_BL comes directly from pin 4 of power connector X2. Because of that the voltage level depends on the connected power module and the voltage attached, and is thus not specified here.

10:   **Caution!** The GPIO5 interface (GPIO5_0 to GPIO5_9) is multiplexed with the tamper detection inputs. Hence, these GPIOs can not be used as GPIO if the phyCORE-i.MX 6UL/ULL is equipped with the i.MX 6UL/ULL version G3.

3.2.5.1 Parallel LCD Interafce

A/V connectors X14 and X15 provide a parallel LCD display interface with up to 24 bit and control signals. The locations of the signals are shown in *Table 22* and *Table 23*.

3.2.5.1.1 Enabeling Data Lines D18 to D23

Jumpers J5 and J10 allow to route data lines D18 to D23 of the phyCORE-i.MX 6UL/ULL's parallel LCD interface to A/V expansion connector X14 to enable implementing a 24-bit LCD interface on a custom A/V expansion board. The following table shows the possible configurations.

J5 to J10	Description
1+2	LCD data lines D18 to D23 routed to A/V connector X14
2+3	**Signals are routed as uSDHC2 interface to expansion connector X16**

Table 24: Routing of the LCD Interface Signals J5 to J10[11]

Note:
Use of data lines D18 to D23 of the i.MX 6UL/ULL's LCD interface at A/V connector X14 requires changing of the BSP.

3.2.5.1.2 LCD Reset Selection

Pin 8 of A/V connector X15 provides a reset signal to allow resetting peripheral devices on a custom A/V expansion board.

Jumper J11 connects either the i.MX 6UL/ULL's LCD_RESET signal, or the system reset signal X_nRESET_OUT to pin 8 of X15. The following table shows the available configurations.

J11	Description
1+2	X_nRESET_OUT connected to X15 pin 8
2+3	**X_LCD_RESET connected to X15 pin 8**

Table 25: LCD Reset Selection J11[11]

3.2.5.2 Brightness

The PWM signal at pin 38 allows changing the brightness of the display attached to the A/V connector.

11: Default settings are in **bold blue** text

3.2.5.3 I^{2}C Connectivity

Please refer to *section 3.2.3* for complete information on the I^{2}C connectivity.

3.2.5.4 Audio I^{2}S

Audio support on the module is done via the I^{2}S interface and controlled via I^{2}C.

On the phyBOARD-Segin i.MX 6UL/ULL the audio codec's registers can be accessed via the I2C1 interface at address 0x18 (7-bit MSB addressing).

3.2.5.5 User programmable GPIOs

Two pins of the A/V connector X15 are dedicated as GPIO (*Table 23*). These signals are also available/used on the corresponding expansion boards, e.g. PEB-AV-02. For more information please look at the Expansion Boards Application Guide (L-793e).

The BSP delivered with the phyBOARD-Segin i.MX 6UL/ULL supports the GPIOs according to the configuration done in correspondence to the expansion board installed on delivery. Thus the GPIOs might not be available if they are needed to support functions of the expansion board. In order to apply the GPIOs for other purposes after removal of the expansion board the BSP must be exchanged, too.

With the appropriate BSP / BSP configuration the GPIOs (GPIO5_5 and GPIO1_18) are available as input by default.

The following table lists all GPIOs, their location, their number and their default usage.

Pin #	GPIO Name	Default Usage	Comment
5	GPIO5_5	IN	Can be used as A/V connector interrupt
6	GPIO1_18	I/O	

Table 26:   GPIOs available at A/V Connector X15

Caution!
The GPIO5 interface (GPIO5_0 to GPIO5_9) is multiplexed with the tamper detection inputs. Hence, GPIO5_5 is not available if the phyCORE-i.MX 6UL/ULL is equipped with the i.MX 6UL/ULL version G3.

3.2.6 Expansion Connector (X16)

Expansion connector X16 provides an easy way to add other functions and features to the phyBOARD-Segin i.MX 6UL/ULL. Standard interfaces such as UART, SPI and I^{2}C as well as different supply voltages and some GPIOs are available at the expansion female connector.

The expansion connector is intended for use with phyBOARD Expansion Boards[12], and to add specific functions with custom expansion boards.

Figure 22:   Expansion Connector (X16)

The pinout of the expansion connector is shown in the following table.

Pin #	Signal Name	Type	SL	Description
1	VCC3V3	OUT	3.3 V	3.3 V power supply
2	VCC5V	OUT	5.0 V	5.0 V power supply
3	VCC1V8	OUT	1.8 V	1.8 V power supply
4	GND	-	-	Ground
5	X_UART2_TX/SPI3_SS0	OUT	3.3 V	ECSPI3 chip select 0
6	X_UART2_nCTS/SPI3_MOSI	OUT	3.3 V	ECSPI3 master output/slave input
7	X_UART2_RTS_B/SPI3_MISO	IN	3.3 V	ECSPI3 master input/slave output
8	X_UART2_RX/SPI3_CLK	OUT	3.3 V	ECSPI3 clock output
9	GND	-	-	Ground
10	X_UART1_RX	IN	3.3 V	UART 1receive data (standard debug interface)
11	X_I2C1_SDA	I/0	3.3 V	I2C 1 data
12	X_UART1_TX	OUT	3.3 V	UART 1 transmit data (standard debug interface)
13	X_I2C1_SCL	I/0	3.3 V	I2C 1 clock
14	GND	-	-	Ground
15	X_JTAG_TMS/SAI2_MCLK	IN	3.3 V	JTAG chain test mode select signal[13]

Table 27:   Phytec Expansion Connector X16

12:   Please find additional information on phyBOARD Expansion Boards in the corresponding application guide (L-793e).
13:   The standard kit comes with the I^{2}S interface available at A/V connector X15. Because of that the JTAG signals which are muxed with the I^{2}S signals are not available at expansion connector X16. Use of the JTAG interface at X16 requires changing of the pin muxing and additional software development.

Pin #	Signal Name	Type	SL	Description
16	X_nJTAG_TRST/SAI2_TXD	IN	3.3 V	JTAG chain test reset[13]
17	X_JTAG_TDI/SAI2_BCLK	IN	3.3 V	JTAG chain test data input[13]
18	X_JTAG_TDO/SAI2_SYNC	OUT	3.3 V	JTAG chain test data output[13]
19	GND	-	-	Ground
20	X_JTAG_TCK/SAI2_RXD	IN	3.3 V	JTAG chain test clock signal[13]
21	X_USB_DP_EXP	I/O	DIFF	USB host data +[14, 15]
22	X_USB_DM_EXP	I/O	DIFF	USB host data -[14, 15]
23	X_nRESET_OUT	OUT	3.3 V	Reset
24	GND	-	-	Ground
25	X_LCD_D18/SD2_CMD	I/O	3.3 V	SD/MMC command
26	X_LCD_D20/SD2_D0	I/O	3.3 V	SD/MMC data 0
27	X_LCD_D19/SD2_CLK	I/O	3.3 V	SD/MMC clock
28	X_LCD_D21/SD2_D1	I/O	3.3 V	SD/MMC data 1
29	GND	-	-	Ground
30	X_LCD_D22/SD2_D2	I/O	3.3 V	SD/MMC data 2
31	X_UART3_RX_EXP	IN	3.3 V	UART3 receive
32	X_LCD_D23/SD2_D3	I/O	3.3 V	SD/MMC data 3
33	X_UART3_TX_EXP	OUT	3.3 V	UART3 transmit
34	GND	-	-	Ground
35	X_JTAG_MOD/SPDIF_TX	I/O	3.3 V	Sony/Philips Digital Interface[13]
36	X_GPIO1_1/nWDOG1_B	I/O	3.3 V	Watchdog (low active)
37	X_BOOT_MODE0	IN	3.3 V	Boot mode 0
38	X_SNVS_TAMPER0	I/O	3.3 V	Tamper detection
39	X_BOOT_MODE1	IN	3.3 V	Boot mode 1
40	X_RTC_nINT	OUT	3.3 V	External RTC interrupt output
41	GND	-	-	Ground
42	X_GPIO5_9	I/O	3.3 V	Power fail signal[16]
43	X_nRESET_IN	IN	3.3 V	Reset input
44	X_GPIO1_3/ADC_IN3	IN	3.3 V	ADC input
45	X_SNVS_PMIC_ON_REQ			Internal PMIC power on request
46	GND	-	-	Ground
47	X_UART3_nCTS/CAN1_TX_EXP		3.3 V	CAN 1 transmit data

Table 27:   Phytec Expansion Connector X16 (continued)

14: J13 and J14 need to be set to 2+3 to route the USB OTG1 interface to the expansion connector (*3.2.6.3*).
15: **Caution!** There is no protective circuit for the USB interfaces brought out at the expansion connector (X16).
16: **Caution!** It could be used as power fail signal for PEB-POW-01 adapter, just if the resistor R22 is mounted.

Pin #	Signal Name	Type	SL	Description
48	X_UART3_nRTS/CAN1_RX_EXP		3.3 V	CAN1 receive data
49	X_CCM_CLK1_P	IN	DIFF	CCM clock positive
50	X_CCM_CLK1_N	IN	DIFF	CCM clock negative
51	GND	-	-	Ground
52	X_ONOFF	IN	3.3 V	CPU ON/OFF
53	X_OTG1_ID	IN	3.3 V	USB OTG1 identification pin
54	X_USB_OTG1_VBUS	OUT	5.0 V	USB OTG1 bus voltage
55	X_nUSB_OTG1_CHD	OUT	3.3 V	USB OTG1 charger enable
56	GND	-	-	Ground
57	VCC_BL	OUT	NS	Backlight power supply[17]
58	X_PMIC_STBY_REQ	OUT	3.3 V	Internal PMIC standby request
59	GND	-	-	Ground
60	VCC5V	IN	5.0 V	5 V input supply voltage

Table 27:   Phytec Expansion Connector X16 (continued)

3.2.6.1 CAN Connectivity

3.2.6.1.1 FLEXCAN1

Jumpers J1 and J2 allow to route the TTL level signals of the i.MX 6UL/ULL's FLEXCAN1 interface to pins 47 (FLEXCAN1_TX) and 48 (FLEXCAN1_RX) of expansion connector X16. This enables implementing a CAN interface on a custom expansion board[18]. The following table shows the possible configurations.

J1, J2	Description
1+2	CAN interface signals are available at expansion connector X16 at TTL level
2+3	**CAN interface signals connected to CAN transceiver at AAV_U1**

Table 28:   Routing of the CAN Interface SignalsJ1, J2[19]

Note:
The CAN signals are multiplexed with the for hardware flow control signals (RTS, CTS) of UART3. Hence changing jumpers J1 and J2 to 1+2 also allows setting up a UART interface with hardware flow control on a custom expansion board.20

17: VCC_BL connects directly to pin 4 of power connector X2. Because of that the voltage level depends on the connected power module and the voltage attached, and is thus not specified here.

18: The standard kit comes with the CAN transceiver installed at AAV_U1. Please contact our sales team, if you need the FLEXCAN1 interface at expansion connector X16.

19: Default settings are in **bold blue** text.

20: Use of UART3 at expansion connector X16 requires changing of the pin muxing and additional software development.

3.2.6.1.2 FLEXCAN2

The second CAN interface (FLEXCAN2) of the i.MX 6UL/ULL is multiplexed with the hardware flow control signals of UART2 which are available at expansion connector pins 6 and 7. FLEXCAN2_RX is available at pin 7 and FLEXCAN2_TX at pin 6.

Use of FLEXCAN2 at X16 requires changing of the pin muxing and additional software development.

3.2.6.2 UART Interfaces

Up to three UART interfaces (UART1 to UART3) are available at expansion connector X16. On the phyCORE-i.MX 6UL/ULL the ports of UART2 and UART3 are used for other interfaces. To use UART2 and UART 3 on the phyBOARD-Segin i.MX 6UL/ULL's expansion connector changing of the pin muxing and additional software development is required.

3.2.6.2.1 UART1

The signals of UART1 are directly routed from the phyCORE-i.MX 6UL/ULL to pins 10 (UART1_RX) and 12 (UART1_TX) of expansion connector X16.

3.2.6.2.2 UART2

The i.MX 6UL/ULL's UART2 signals are used for the SPI interface at expansion connector X16. Changing of the pin muxing and additional software development allows using UART2 at expansion connector X16. UART2 provides hardware flow control. The locations of the UART2 signals are shown in *Table 27.*

3.2.6.2.3 UART3

Jumpers J3 and J4 allow to route the TTL level signals of the phyCORE-i.MX 6's UART3 interface to pins 31 (UART3_RX) and 33 (UART3_TX) of expansion connector X16 to enable implementing a serial interface on a custom expansion board if the camera interface is not needed[21]. The following table shows the possible configurations.

J3, J4	Description
1+2	UART3 interface signals (TX, RX) are available at expansion connector X16 at TTL level
2+3	**Signals are routed as CSI data lines D0 and D1 to the transceiver at U6 and are used to build up the phyCAM-P camera interface**

Table 29:   Routing of the UART3 Interface Signals J3, J4[22]

21: The standard kit comes with the phyCAM-P interface enabled. Please contact our sales team, if you need the UART3 interface at expansion connector X16.

22: Default settings are in **bold blue** text

3.2.6.3 USB OTG Interface

The USB OTG interface of the phYBOARD-i.MX 6UL/ULL can be routed to expansion connector X16 [23]. Jumpers J13 and J14 route the USB data signals to pins 21 (USB_DP) and 22 (USB_DM) of expansion connector X16. The signals OTG1_ID (pin 53), nUSB_OTG1_CHD (pin 53) and USB_OTG1_VBUS (pin 54) are connected permanently to the expansion connector.

The following table shows the possible configurations of jumpers J13 and J14.

J13, J14	Description
1+2	**USB1 interface signals (DM, DP) are routed to USB connector X8**
2+3	USB1 interface available at expansion connector X16

Table 30:   Routing of the USB OTG Interface Signals J13, J14[24]

Note:
Use of UART3 at expansion connector X16 requires changing of the BSP and renders the phyCAM-P camera interface at X12 unusable.

3.2.6.3.1 Configuring the OTG Operating Mode (R34)

Resistor R34 configures the OTG operating mode with the OTG1_ID signal. By default this resistor is not mounted, which leaves the ID pin floating, and thus configuring the interface as USB OTG. Mounting a 10 kΩ resistor connects the OTG1_ID pin to GND and configures the OTG interface as USB host.

Typically the configuration of a connecting device as host or slave is done automatically via the USB cable. However, given the limited number of OTG enabled devices in the embedded market, this resistor is provided to either simulate an OTG cable, or force the OTG interface into host mode when OTG operation is not required.

23: **Caution!** There is no protective circuit for the USB interfaces brought out at the expansion connector X16.
24: Default settings are in **bold blue** text

3.2.6.4 JTAG Interface

The phyBOARD-Segin i.MX 6UL/ULL provides a JTAG interface. The signals for the JTAG interface share the controller pins with the audio interface of the i.MX 6UL/ULL. In the default configuration the audio interface is brought out at the phyCORE-Connector. Because of that the pin muxing must be changed if the JTAG interface is required during development. The locations of the JTAG signals at expansion connector X16 are shown in *Table 27.*

Caution!
To avoid disturbances at the JTAG interface the audio codec must be disabled. This can be done with jumper JP2. Closing Jumper JP2 at 2+3 connects the reset input of the audio codec to GND which holds the audio codec in reset state.

Figure 23:   Audio Codec Disable Jumper JP2

Mode Selection	Description
Audio reset signal (JP2 = 1+2)	Audio codec normal operation
JTAG mode (JP2 = 2+3)	Audio codec disabled, JTAG interface can be used

Table 31:   Audio Codec Disable Jumper JP2[25]

3.2.6.4.1 I^{2}C Connectivity

Please refer to *section 3.2.3.*

25:   Default settings are in **bold blue** text

4   Revision History

Date	Version #	Changes in this manual
26.07.2017	Manual L-820e_1	First edition. Describes the phyCORE-i.MX 6UL/ULL SOM (PCB 1468.2) with phyBOARD-Segin i.MX 6UL/ULL-Carrier Board (PCB 1472.1)

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