# 3. phyCORE-i.MX6UL


- 1.
- 2.
- 3.
- 4.
- 5.I2C
- 6.USB
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- 8.
- 9.EMMC
- 10.LCD
- 11.
- 12.


## 1.

- phyCORE-i.MX6UL(L-827e_2)
- phyBOARD-Segin i.MX6UL(L-802e_1)
- 
  - PCL-063
  - PCB1468
  - PBA-CD-10 phyBOARD-Segin
  - PCB1472
- phyCORE-i.MX6UL(L-827e_2) Figure 12
- phyCORE-i.MX6UL(L-827e_2) Table 4
- /phyCORE-i.MX6UL(L-827e_2) Figure 4&13
- phyCORE i.MX6ul CPU
- Altium Designer
  - 
  - 
- 
  - 
  - 
  - phyCORE-i.MX6UL(L-827e_2) Figure 2&3
- dxf/step 3D
  - 3D Step
  - dxf
- Segin
  - 
  - 
  - dxf
  - 3D step
- SMT Soldering Instruction for the phyCORE-i.MX6UL/ULL(LAN-077e.A1)

## 2.

4.4

imx6ul3.3V

| | |
|---|---|
| X_nRESET_OUT | 98 |

IO

## 3.

4.5

| | | |
|---|---|---|
| X_nRESET_OUT | 98 | |
| X_nRESET_IN | 100 | 200ms |

## 4.

imx6ul

Boot_mode

| | | |
|---|---|---|
| X_BOOT_MODE0 | 104 | 10k |
| X_BOOT_MODE1 | 103 | 4.7k |

SD

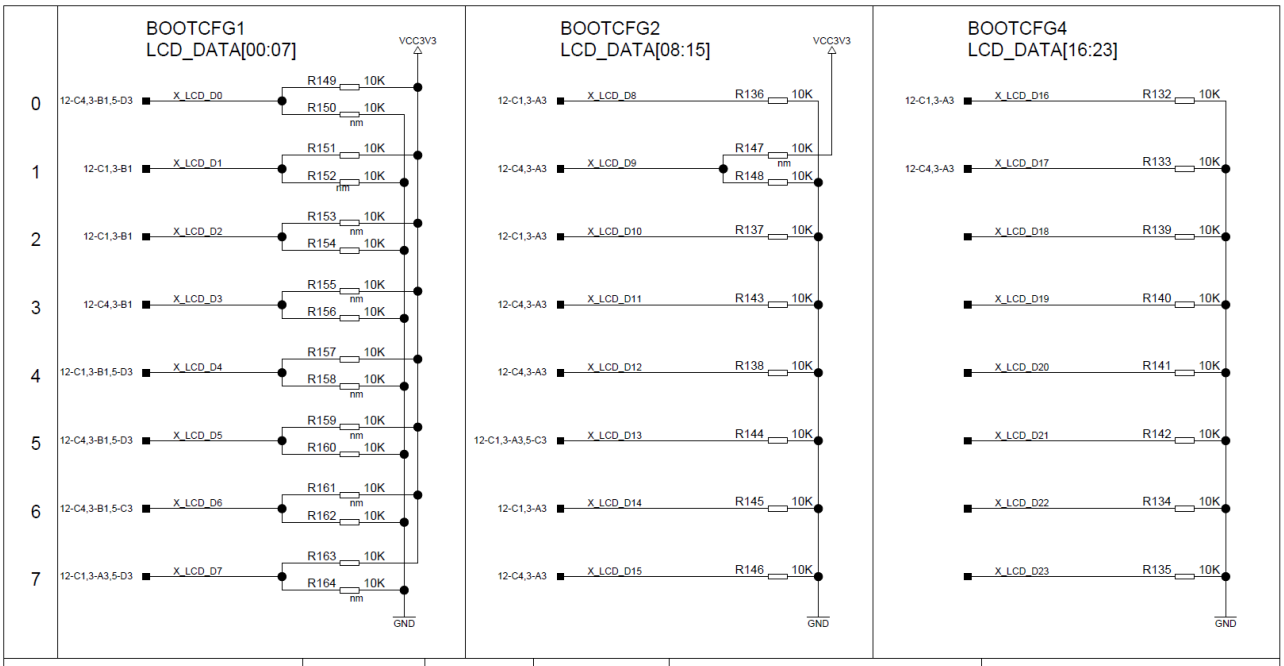
| | | SD(usdhc1) | 128MB/256MB NAND | 512MB/1GB NAND | emmc(usdhc2) |
|---|---|---|---|---|---|
| X_LCD_D[7:0] | BCFG1[7:0] | 0100,0010 | 1001,0010 | 1001,0011 | 0110,0000 |
| X_LCD_D[15:8] | BCFG2[7:0] | 0010,0000 | 0000,0000 | 0000,0000 | 0100,1000 |
| X_LCD_D[23:16] | BCFG4[7:0] | 0000,0000 | 0000,0000 | 0000,0000 | 0000,0000 |

2410kio

resetIO

/ Examples on boot pin isolation

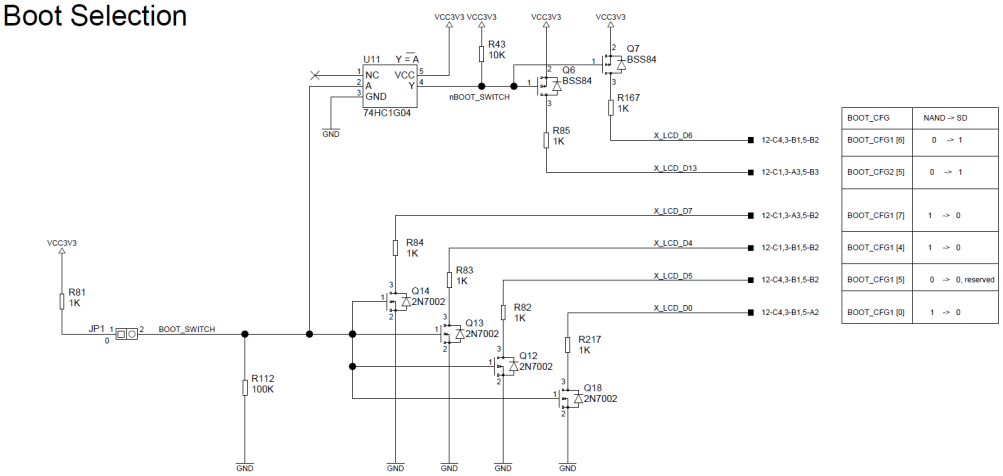
Segin




| Description | BOOTCFG1[7:0] XX0X00XX | BOOTCFG2[7:0] 00X00000 | BOOTCFG4[7:0] 00000000 | mounted | not mounted |
|---|---|---|---|---|---|
| NAND 1Gbit (128MByte) (64 pages per block, 4 address bytes) | 10010010 | 00000000 | 00000000 | R148, R150, R151, R154, R156, R157, R160, R162, R163 | R147, R149, R152, R153, R155, R158, R159, R161, R164 |
| NAND 4Gbit (512MByte) (64 pages per block, 5 address bytes) | 10010011 | 00000000 | 00000000 | R148, R149, R151, R154, R156, R157, R160, R162, R163 | R147, R149, R151, R153, R155, R158, R159, R161, R164 |
| SD Card | 01000010 | 00100000 | 00000000 | | |

IONANDSD

Boot Selection




| BOOT_CFG | NAND -> SD |
|---|---|
| BOOT_CFG1 [6] | 0 -> 1 |
| BOOT_CFG2 [5] | 0 -> 1 |
| BOOT_CFG1 [7] | 1 -> 0 |
| BOOT_CFG1 [4] | 1 -> 0 |
| BOOT_CFG1 [5] | 0 -> 0, reserved |
| BOOT_CFG1 [0] | 1 -> 0 |

## 5.I2C

eeprom

| | |
|---|---|
| X_I2C1_SCL | 60 |
| X_I2C1_SDA | 61 |

1k

## 6.USB

Hardware Development Guide for the i.MX 6UltraLite Applications Processor

USBVBUSUSB5VUSB Phy

OTG

VBUS1uF

## 7.

UART1

| | |
|---|---|
| X_UART1_RX | 105 |
| X_UART1_TX | 107 |

## 8.

phy KSZ8081RNBIAdesign checklist

LED

| | | | | |
|---|---|---|---|---|
| | | **reset** | | |

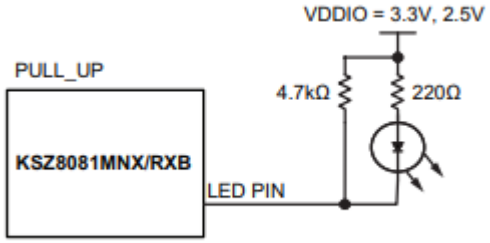
| | | | | |
|---|---|---|---|---|
| X_ETH1_LED0 | 17 | | 4.7k |  |
| X_ETH1_LED1 | 16 | | 4.7k | |

**FIGURE 4-1: TRANSMIT AND RECEIVE CHANNEL CONNECTIONS**

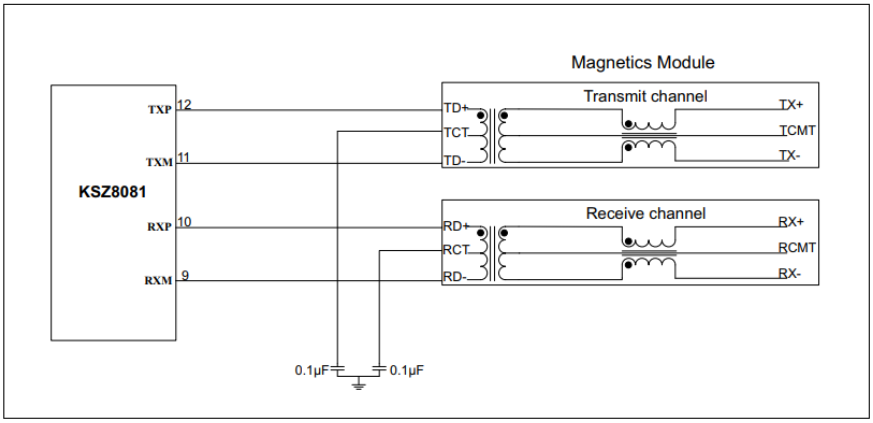



**FIGURE 7-16: TYPICAL MAGNETIC INTERFACE CIRCUIT**

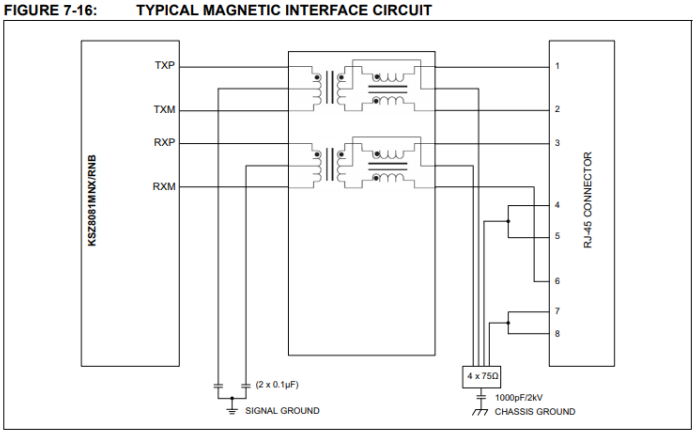



Table 7-13 lists recommended magnetic characteristics.

## 9.EMMC

- NANDEMMCSD2
  - cpu
  - SDIOSD/TFSDIOWIFI
-

| | BOOTCFG1[7:0]<br>XXXXXXXX | BOOTCFG2[7:0]<br>0XX0X000 | BOOTCFG4[7:0]<br>00000000 |
|---|---|---|---|
| NAND 1Gb (64 pages per block, 4 address bytes) | 10010010 | 00000000 | 00000000 |
| NAND 2/4Gb (64 pages per block, 5 address bytes) | 10010011 | 00000000 | 00000000 |
| SD-Card (usdhc1 interface) | 01000010 | 00100000 | 00000000 |
| eMMC (usdhc2 interface) | 01100000 | 01001000 | 00000000 |

## 10.LCD

LCDimx6ulTable 61

**Table 61. LCD Signal Parameters**

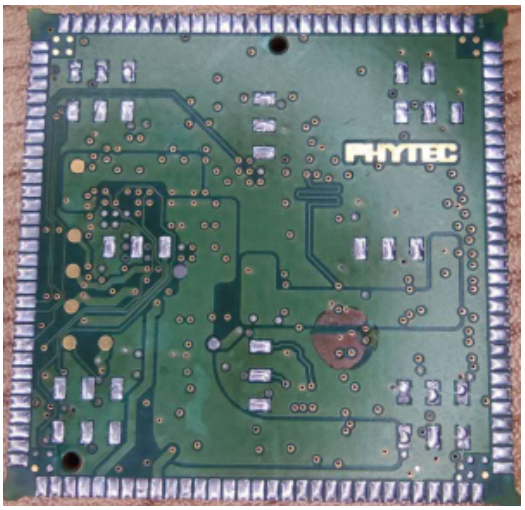
| Pin name | 8-bit DOTCLK LCD IF | 16-bit DOTCLK LCD IF | 18-bit DOTCLK LCD IF | 24-bit DOTCLK LCD IF | 8-bit DVI LCD IF |
|---|---|---|---|---|---|
| LCD_RS | — | — | — | — | CCIR_CLK |
| LCD_VSYNC* (Two options) | LCD_VSYNC | LCD_VSYNC | LCD_VSYNC | LCD_VSYNC | — |
| LCD_HSYNC | LCD_HSYNC | LCD_HSYNC | LCD_HSYNC | LCD_HSYNC | — |
| LCD_DOTCLK | LCD_DOTCLK | LCD_DOTCLK | LCD_DOTCLK | LCD_DOTCLK | — |
| LCD_ENABLE | LCD_ENABLE | LCD_ENABLE | LCD_ENABLE | LCD_ENABLE | — |
| LCD_D23 | — | — | — | R[7] | — |
| LCD_D22 | — | — | — | R[6] | — |
| LCD_D21 | — | — | — | R[5] | — |
| LCD_D20 | — | — | — | R[4] | — |
| LCD_D19 | — | — | — | R[3] | — |
| LCD_D18 | — | — | — | R[2] | — |
| LCD_D17 | — | — | R[5] | R[1] | — |
| LCD_D16 | — | — | R[4] | R[0] | — |
| LCD_D15 / VSYNC* | — | R[4] | R[3] | G[7] | — |
| LCD_D14 / HSYNC** | — | R[3] | R[2] | G[6] | — |
| LCD_D13 / LCD_DOTCLK ** | — | R21] | R[1] | G[5] | — |

**Table 61. LCD Signal Parameters (continued)**

| | | | | | |
|---|---|---|---|---|---|
| LCD_D12 / ENABLE** | — | R[1] | R[0] | G[4] | — |
| LCD_D11 | — | R[0] | G[5] | G[3] | — |
| LCD_D10 | — | G[5] | G[4] | G[2] | — |
| LCD_D9 | — | G[4] | G[3] | G[1] | — |
| LCD_D8 | — | G[3] | G[2] | G[0] | — |
| LCD_D8 | — | G[3] | G[2] | G[0] | — |
| LCD_D7 | R[2] | G[2] | G[1] | B[7] | Y/C[7] |
| LCD_D6 | R[1] | G[1] | G[0] | B[6] | Y/C[6] |
| LCD_D5 | R[0] | G[0] | B[5] | B[5] | Y/C[5] |
| LCD_D4 | G[2] | B[4] | B[4] | B[4] | Y/C[4] |
| LCD_D3 | G[1] | B[3] | B[3] | B[3] | Y/C[3] |
| LCD_D2 | G[0] | B[2] | B[2] | B[2] | Y/C[2] |
| LCD_D1 | B[1] | B[1] | B[1] | B[1] | Y/C[1] |
| LCD_D0 | B[0] | B[0] | B[0] | B[0] | Y/C[0] |
| LCD_RESET | LCD_RESET | LCD_RESET | LCD_RESET | LCD_RESET | — |
| LCD_BUSY / LCD_VSYNC | LCD_BUSY (or optional LCD_VSYNC) | LCD_BUSY (or optional LCD_VSYNC) | LCD_BUSY (or optional LCD_VSYNC) | LCD_BUSY (or optional LCD_VSYNC) | — |

LCD85MHz1366x768@60Hz

## 11.




## 12.

| | | |
|---|---|---|
| X_PMIC_STBY_REQ | 102 | |
| X_SNVS_PMIC_ON_REQ | 101 | |
| X_ONOFF | 99 | |