

How To Use SPIDEV on phyFLEX-i.MX6 Yocto BSP

The following will provide instructions for exercising SPI0 (ECSPI3) and SPI1 (ECSPI5) on the phyFLEX-i.MX6 RDK using release PD15.3.0. This example is a loopback test and will set up the phyFLEX-i.MX6 RDK by connecting SPI1_MOSI to SPI1_MISO at the X30 header, as well as SPI0 on the pin header X53.

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Booting the BSP

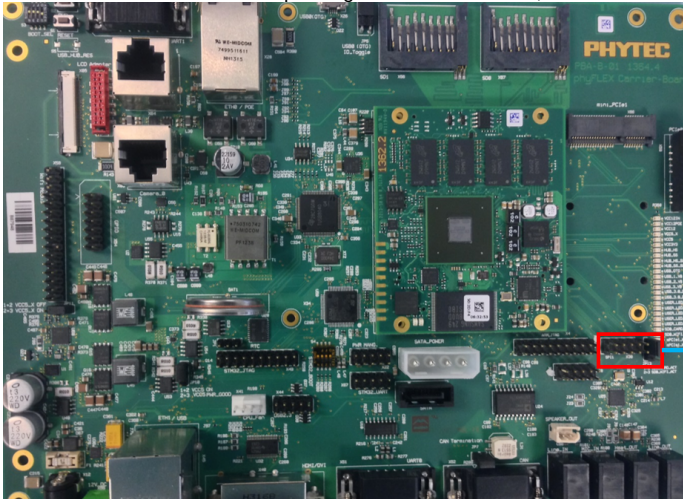
1. Create an sd card using the [.sdcard image](#) from PHYTEC DE FTP. This image contains a device tree file with ecspi3 and ecspi5 configured for spidev.

```
sudo dd if=phytec-headless-image-phyflex-imx6-2.sdcard of=/dev/sd<your device> bs=1M conv=fsync
```

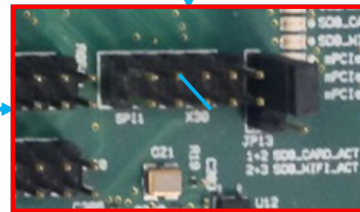
2. Copy the [SPITest application](#) to the root filesystem of the SD card

```
sudo cp SPITest /media/<user>/83d62e12-ea57-4557-85e7-ee67e229887a/home/root/; sync
```

3. Set the boot switch to boot from SD.
4. Connect SPI3 MOSI and MISO pins together on header X53, and SPI5 MISO and MOSI on X30.



Connect pins X30-6 (SPI1_MISO) and X30-7 (SPI1_MOSI)



5. Boot the board fully into Linux and check the available SPI devices:

```
root@phyflex-imx6-2:~# ls -l /dev/spidev*
crw----- 1 root root 153, 0 Aug 30 20:37 /dev/spidev2.1      #
Corresponds with ECSPi3 chip select 1
crw----- 1 root root 153, 1 Aug 30 20:37 /dev/spidev2.2      #
Corresponds with ECSPi3 chip select 2
crw----- 1 root root 153, 2 Aug 30 20:37 /dev/spidev4.0      #
Corresponds with ECSPi5 chip select 0
crw----- 1 root root 153, 3 Aug 30 20:37 /dev/spidev4.1      #
Corresponds with ECSPi5 chip select 1
```

6. Run the SPITest application for SPI3 cs1. The test can be run by passing any of the spidev devices.

```

root@phyflex-imx6-2:~# chmod +x SPITest

root@phyflex-imx6-2:~# ./SPITest -D /dev/spidev2.1
spi mode: 0
bits per word: 8
max speed: 500000 Hz (500 KHz)

FF FF FF FF FF FF
40 00 00 00 00 95
FF FF FF FF FF FF
FF FF FF FF FF FF
FF FF FF FF FF FF
DE AD BE EF BA AD
F0 0D

```



If SPI communication is not functioning properly, only "FF"s will be transmitted.

Device Tree Configuration

In the case of this BSP, ecspi3 and ecspi5 are already configured for spidev. The following instructions describe how to clone the kernel source and show how SPIDEV was enabled in the device tree.

Note that although the kernel source is available in the Yocto BSP build directory, it is recommended to clone the kernel source separately from the Yocto build when doing kernel development. To do so:

1. Clone linux-mainline repo from [git.phytec.de](https://git.phytec.de/linux-mainline):

```
git clone git://git.phytec.de/linux-mainline
```

2. Create a branch based on release tag v4.1.18-phy4, which corresponds with PD15.3.0 BSP.

```
git checkout -b <development branch name> v4.1.18-phy4
```

3. The device tree corresponding to phyflex-imx6-2 is imx6q-phytec-pbab01.dts. This file includes several dtsti files, corresponding to the processor, SOM, carrier board, and compatible modules. Note that if you are working with a different machine and are unsure which device tree corresponds with it, check "KERNEL_DEVICE_TREE" in the [machine configuration](#) of the Yocto build.

The SOM dtsti file, imx6qdl-phytec-pfla02.dtsi, configures the pinmuxing for the ECSPi3 signals. The SOM dtsti only configures the SPI Flash chip for ECSPi3 in this file.

```

&iomuxc {
    pinctrl-names = "default";
    pinctrl-0 = <&pinctrl_hog>;

    imx6q-phytec-pfla02 {

...
        pinctrl_ecspi3: ecspi3grp {
            fsl,pins = <
                MX6QDL_PAD_DISP0_DAT0__ECSPI3_SCLK      0x100b1
                MX6QDL_PAD_DISP0_DAT2__ECSPI3_MISO      0x100b1
                MX6QDL_PAD_DISP0_DAT1__ECSPI3_MOSI      0x100b1
                MX6QDL_PAD_DISP0_DAT3__GPIO4_I024      0x80000000
                MX6QDL_PAD_DISP0_DAT4__GPIO4_I025      0x80000000
                MX6QDL_PAD_DISP0_DAT5__GPIO4_I026      0x80000000
            >;
        };

...

/* SPI0 on module */
&ecspi3 {
    pinctrl-names = "default";
    pinctrl-0 = <&pinctrl_ecspi3>;
    status = "okay";
    fsl,spi-num-chipselects = <3>;
    cs-gpios = <&gpio4 24 GPIO_ACTIVE_HIGH
        &gpio4 25 GPIO_ACTIVE_HIGH
        &gpio4 26 GPIO_ACTIVE_HIGH>;

    flash@@ {
        compatible = "m25p80";
        spi-max-frequency = <20000000>;
        reg = <0>;

        #address-cells = <1>;
        #size-cells = <1>;

...

```

Then the carrier board dtsi, imx6qdl-phytec-pbab01.dtsi, configures ecspi cs1 and cs2 for spidev:

```

&ecspi3 {
    spi@1 {
        compatible = "spidev";
        spi-max-frequency = <57600000>;
        reg = <1>;
    };

    spi@2 {
        compatible = "spidev";
        spi-max-frequency = <57600000>;
        reg = <2>;
    };
};

```