How-to: Configure the phyCORE-i.MX7 SoM pinout with the "Pins" tool

This how-to will demonstrate how to use NXP's "Pins" tool to configure the phyCORE-i.MX7 SoM pinout.

Getting Started

NXP provides a tool, called "Pins", that is used to configure the processors pin functions. This can be a very useful tool for implementing a custom peripheral set for your application.

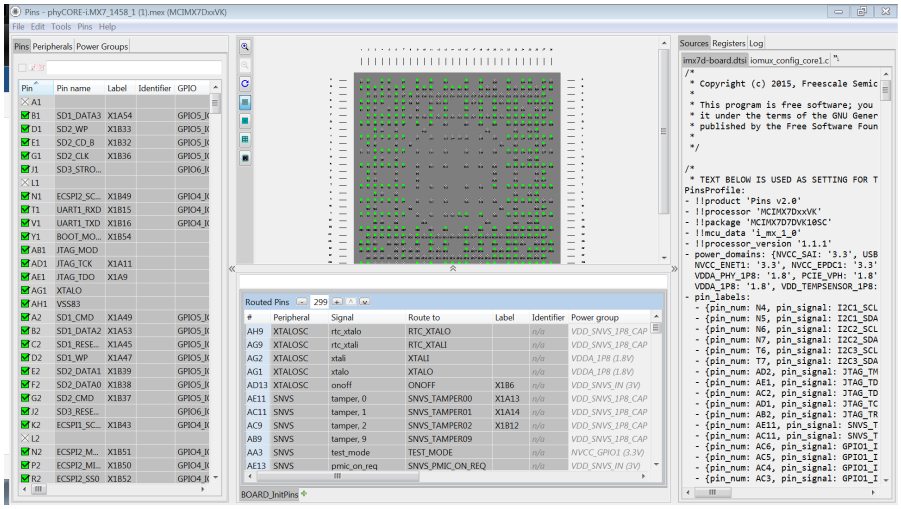
To get started, download the Pins application here:

> http://www.nxp.com/products/software-and-tools/software-development-tools/processor-expert-and-embedded-components/software-suites/pins-tool-for-i.mx-application-processors:PINS-TOOL-IMX

Also, download the standard phyCORE-i.MX7 SoM configuration here:

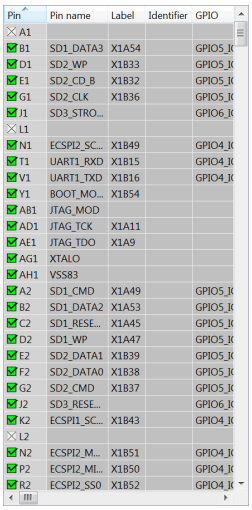
> https://develop.phytec.com/download/attachments/34113565/phyCORE-i.MX7_1458_1.mex?api=v2

Open the "phyCORE-i.MX7_1458_1.mex" file using Pins (see below). This shows the standard configuration for the SoM:



Customizing for your application

If you need to customize the SoM pinout, the Pins tool is a great tool to figure out what is possible. Keep in mind that this tool is for the processor and not every processor pin is available on the SoM connector. With that in mind, note that the "Label" column in the picture below indicates the processor pins location on the SoM connector. For example, UART1_RXD is configured on processor pin T1, which is connected to the SoM connector at X1 B15. Likewise, UART1_TXD is configured on processor pin V1, which is connected to the SoM connector at X1 B16.



Pin	Pin name	Label	Identifier	GPIO
A1				
B1	SD1_DATA3	X1A54		GPIO5_I(
D1	SD2_WP	X1B33		GPIO5_I(
E1	SD2_CD_B	X1B32		GPIO5_I(
G1	SD2_CLK	X1B36		GPIO5_I(
J1	SD3_STRO...			GPIO6_I(
L1				
N1	ECSPI2_SC...	X1B49		GPIO4_I(
T1	UART1_RXD	X1B15		GPIO4_I(
V1	UART1_TXD	X1B16		GPIO4_I(
Y1	BOOT_MO...	X1B54		
AB1	JTAG_MOD			
AD1	JTAG_TCK	X1A11		
AE1	JTAG_TDO	X1A9		
AG1	XTALO			
AH1	VSS83			
A2	SD1_CMD	X1A49		GPIO5_I(
B2	SD1_DATA2	X1A53		GPIO5_I(
C2	SD1_RESE...	X1A45		GPIO5_I(
D2	SD1_WP	X1A47		GPIO5_I(
E2	SD2_DATA1	X1B39		GPIO5_I(
F2	SD2_DATA0	X1B38		GPIO5_I(
G2	SD2_CMD	X1B37		GPIO5_I(
J2	SD3_RESE...			GPIO6_I(
K2	ECSPI1_SC...	X1B43		GPIO4_I(
L2				
N2	ECSPI2_M...	X1B51		GPIO4_I(
P2	ECSPI2_MI...	X1B50		GPIO4_I(
R2	ECSPI2_SS0	X1B52		GPIO4_I(