Application Note: Boot i.MX7 without pressing the power button

- Summary
- Default Behavior
- Modifying to power on without a button press

Summary

The phyCORE-i.MX7 System on Module (SoM) by default requires a power button to be pressed in order to boot the device. This application note will explain the default behavior in depth and provide a solution for changing the behavior of the SoM so that a button press is not required to boot the device.

Default Behavior

The i.MX 7 Processor supports various power modes including:

- OFF Mode
- Secure Non-Volatile Storage (SNVS) Mode
- Low Power State Retention (LPSR) Mode
- RUN Mode
- Low Power Mode

This application note will focus on 'OFF', 'RUN', and 'SNVS' mode. The below snapshot (Figure 5-11 and Table 13) was taken from NXP's i.MX7Dual Applications Processor Reference Manual, Rev. 0.1, 08-2016. Please refer to this manual for additional details on the available modes.

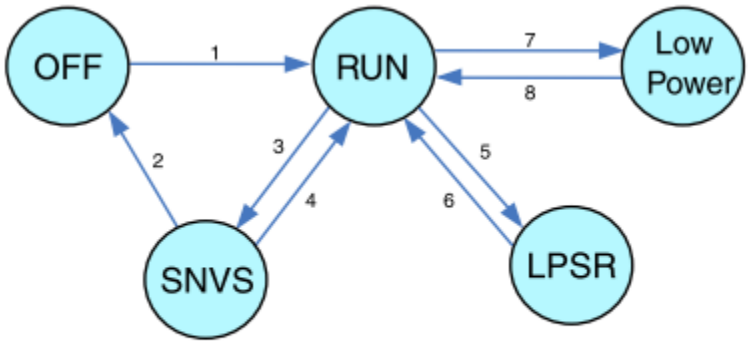

Figure 5-11. i.MX7Dual Power Modes

Table 13. Power Mode Transition

Transition	From	To	Condition
1	OFF	RUN	VDD_SVNS_IN supply present.
2	SNVS	OFF	VDD_SNVS_IN supply removal.
3	RUN	SNVS	ONOFF long press, or SW.
4	SNVS	RUN	ONOFF press, or RTC, or tamper event.
5	RUN	LPSR	SW.
6	LPSR	RUN	ONOFF press, or RTC, or tamper event, or GPIO event.
7	RUN	Low Power	SW (CPU execute WFI)
8	Low Power	RUN	RTC, tamper event, IRQ.

In addition to 'RUN' and 'OFF' modes, the phyCORE-i.MX7 SoM has been designed to support the low power Secure Non-Volatile Storage (SNVS) mode. When in this mode, a portion of the i.MX 7 chip is in a low power state where only RTC and tamper detection logic is active.

SNVS mode requires VDD_SNVS_IN to be present. The phyCORE-i.MX7 SoM is configured such that the VDD_SNVS_IN rail is always supplied. When power is applied, VDD_SNVS_IN is sourced from 'VIN' (tied to VCC_SOM). Likewise, when power is removed, VDD_SNVS_IN is sourced from 'LICELL' coin cell supply (tied to VBAT). As long as there is a valid voltage present from either power applied or there is a charged battery attached, the i.MX 7 will not transition from 'RUN' to 'OFF' mode. Instead it will transition from 'RUN' to 'SNVS' mode. The transition from 'RUN' to 'SNVS' (step 3 in the above Figure) can be triggered by the following:

- Software controlled power off - For example, safe shut down of the system using the 'poweroff' command in Linux.
- Long ONOFF signal press - phyCORE-i.MX7 SoM signal X_MX7_ONOFF is connected to a button on the phyBOARD-Zeta. If this button is held it will trigger a move between power states.

To then boot the board and bring the i.MX 7 from 'SNVS' to 'RUN', this can be triggered by the following actions:

- ONOFF signal press - With the phyCORE-i.MX7 SoM signal X_MX7_ONOFF is connected to a button on the phyBOARD-Zeta. This button must be pressed to boot the board.
- RTC event
- Tamper event

Due to VDD_SNVS_IN always being present, a button press will always be required to boot the system.

Modifying to power on without a button press

If your use case requires the board to boot up without a button press, the VDD_SNVS_IN supply will need to be removed to transition the i.MX 7 from 'RUN' mode to 'OFF' mode. Currently when power is removed, VDD_SNVS_IN is sourced from 'LICELL' coin cell supply (tied to VBAT). As long as there is a charged battery supplying the VBAT rail, VDD_SNVS_IN will be supplied and the board will remain in 'SNVS' mode. One solution is to not supply VDD_SNVS_IN when power is cut from the system. This can be done by removing the connection between VBAT and the i.MX 7.

Please note that this solution will require the SoM to be power cycled in order to boot the device (which forces an automatic 'OFF' to 'RUN' transition). If you are using software or an ONOFF long press to turn off the i.MX 7 and VCC_SOM is still supplied, the board will still transition into the 'SNVS' mode until the VCC_SOM supply is removed. In that case, a button press or RTC/tamper event will be required to transition into 'RUN' mode from 'SNVS'.

Below are a couple options to disconnect VBAT from the i.MX 7:

1. No external battery. Do not supply the VBAT rail on your carrier board design.

   ⚠ Discrete RTC functionality will be lost.

2. Depopulate R172 on the phyCORE-i.MX7 SoM. This will disconnect VBAT from the LICELL pin, while still allowing it to supply the discrete RTC.

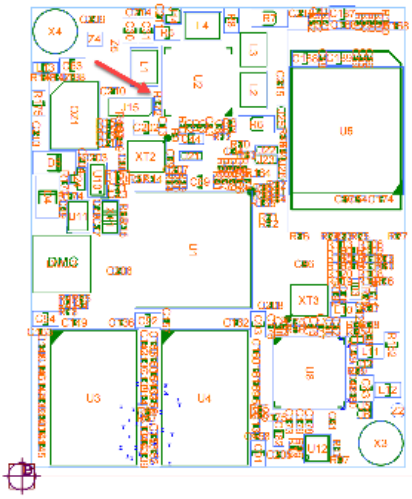

Figure 1: Component placement of R172 on the phyCORE-i.MX7 SOM