phyCORE-i.MX6 / Configuration for display

LCD/LCD display timings in device tree

/ RGB

imx6 datasheet

4.11.10.4 IPU Display Interface Signal Mapping

The IPU supports a number of display output video formats. Table 64 defines the mapping of the Display Interface Pins used during various supported video interface formats.

Table 64. Video Signal Cross-Reference

I.MX 6Dual/6Quad	LCD							Comment[1,2]
Port Name (x = 0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[3]	16-bit YCrCb	20-bit YCrCb	
IPUx_DISPx_DAT00	DAT[0]	B[0]	B[0]	B[0]	Y/C[0]	C[0]	C[0]	—
IPUx_DISPx_DAT01	DAT[1]	B[1]	B[1]	B[1]	Y/C[1]	C[1]	C[1]	—
IPUx_DISPx_DAT02	DAT[2]	B[2]	B[2]	B[2]	Y/C[2]	C[2]	C[2]	—
IPUx_DISPx_DAT03	DAT[3]	B[3]	B[3]	B[3]	Y/C[3]	C[3]	C[3]	—
IPUx_DISPx_DAT04	DAT[4]	B[4]	B[4]	B[4]	Y/C[4]	C[4]	C[4]	—
IPUx_DISPx_DAT05	DAT[5]	G[0]	B[5]	B[5]	Y/C[5]	C[5]	C[5]	—
IPUx_DISPx_DAT06	DAT[6]	G[1]	G[0]	B[6]	Y/C[6]	C[6]	C[6]	—

PD16.1.0 DRDY/DV or DE Data Enable

imx6qdl-phytec-mira-peb-av-02.dtsi

```
diff --git a/arch/arm/boot/dts/imx6qdl-phytec-mira-peb-av-02.dtsi b/arch/arm/boot/dts/imx6qdl-phytec-mira-peb-
av-02.dtsi
index 95e450c..66662d1 100644
--- a/arch/arm/boot/dts/imx6qdl-phytec-mira-peb-av-02.dtsi
+++ b/arch/arm/boot/dts/imx6qdl-phytec-mira-peb-av-02.dtsi
@@ -151,7 +151,7 @@
                                MX6QDL_PAD_DI0_PIN2__IPU1_DI0_PIN02        0x10
                                MX6QDL_PAD_DI0_PIN3__IPU1_DI0_PIN03        0x10

-                               MX6QDL_PAD_DI0_PIN15__IPU1_DI0_PIN15  0x1b080
+                               MX6QDL_PAD_DI0_PIN15__IPU1_DI0_PIN15  0x1b0b0

                                MX6QDL_PAD_DISP0_DAT0__IPU1_DISP0_DATA00   0x10
                                MX6QDL_PAD_DISP0_DAT1__IPU1_DISP0_DATA01   0x10
```

LVDS

imx6LVDS

imx6lvds37MHz

dts imx6q-phytec-mira-rdk-nand.dts

```
&clks {
     assigned-clocks = <&clks IMX6QDL_CLK_LDB_DI0_SEL>,
               <&clks IMX6QDL_CLK_LDB_DI1_SEL>;
     assigned-clock-parents = <&clks IMX6QDL_CLK_PLL5_VIDEO_DIV>,
               <&clks IMX6QDL_CLK_PLL5_VIDEO_DIV>;
};
```

LVDS

https://github.com/torvalds/linux/commit/b8a559feffb2210344bb11cedc1103311ac41de5#diff-343c12e7de8f2207eccb97b7b30c5022R407

```
&ldb {
        fsl,dual-channel;
        status = "okay";

         lvds-channel@0 {
                fsl,data-mapping = "spwg";
                fsl,data-width = <18>;
                status = "okay";

                 display-timings {
                        native-mode = <&timing0>;
                        timing0: hsd100pxn1 {
                                clock-frequency = <65000000>;
                                hactive = <1024>;
                                vactive = <768>;
                                hback-porch = <220>;
                                hfront-porch = <40>;
                                vback-porch = <21>;
                                vfront-porch = <7>;
                                hsync-len = <60>;
                                vsync-len = <10>;
                        };
                };
        };
};
```

lvdsclock-frequency32.5MHz

56MLVDS

fsl, dual-channel https://github.com/torvalds/linux/blob/df0cc57e/Documentation/devicetree/bindings/display/imx/ldb.txt#L40